Low-temperature preparation of GaN-SiO_2 interfaces with low defect density. I. Two-step remote plasma-assisted oxidation-deposition process

Choelhwyi Bae and Gerald Lucovsky[a)]
Departments of Physics, Materials Science and Engineering, and Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina 27695-8202

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In previous studies, device-quality Si-SiO_2 interfaces and dielectric bulk films (SiO_2) were prepared using a two-step process: (i) remote plasma-assisted oxidation (RPAO) to form a superficially interfacial oxide (~0.6 nm) and (ii) remote plasma-enhanced chemical vapor deposition (RPECVD) to deposit the oxide film. The same approach has been applied to the GaN-SiO_2 system. Without an RPAO step, subcutaneous oxidation of GaN takes place during RPECVD deposition of SiO_2, and on-line Auger electron spectroscopy indicates a ~0.7-nm subcutaneous oxide. The quality of the interface and dielectric layer with/without RPAO process has been investigated by fabricated GaN metal-oxide-semiconductor capacitors. Compared to single-step SiO_2 deposition, significantly reduced defect state densities are obtained at the GaN-SiO_2 interface by independent control of GaN-GaO_x interface formation by RPAO and SiO_2 deposition by RPECVD. © *2004 American Vacuum Society.* [DOI: 10.1116/1.1807396]

I. INTRODUCTION

GaN has emerged as an important material for optoelectronic and high-temperature/high-power/high-frequency device applications. As such, GaN-dielectric insulators for gate dielectrics[1] and surface passivation layers[2] have become important issues in device processing. Studies of GaN metal-insulator-semiconductor (MIS) systems have focused on reducing fixed-oxide charge and interface-trapped charge. For *n*-type GaN MIS systems, interface state density (D_{it}) in the range of low-to-mid 10^{11} cm^{-2} eV^{-1} has been obtained without *in situ* native oxide removal and thin intermediate layer (or sacrificial layer) preparation.[1] These results are remarkably different from the other compound semiconductors, where surface passivation has been an important issue to avoid thin native oxide formation between deposited oxide and substrate. Considering the deep depletion without severe Fermi-level pinning, and the low D_{it} of *n*-type GaN MIS systems, the native oxide of GaN is exempt from the critically undesirable factors such as multiple-type oxides, thermodynamic instability, metallic residue, and smaller band gap than that of the semiconductor. In the cases of GaAs metal-oxide-semiconductor (MOS) systems, improved surface passivation was initially obtained by removal of As_2O_3 and subsequent formation of a few monolayers of Ga_2O_3 film or $(Ga_2O_3)_{1-x}(Gd_2O_3)_x$.[3–5]

The main difference of GaN from other III-V semiconductors, such as GaAs and GaP, is the volatility of N oxide species, e.g., NO and N_2O. This suggests that a thin native oxide of GaN can be used to control the semiconductor-deposited dielectric interface. The purpose of our present work is to investigate how a controlled superficially thin native oxide of GaN can improve the quality of the interface and dielectric layer of the GaN MOS system. For the oxide film deposition by a plasma-assisted process, *ex situ* wet chemical and *in situ* removal of the air-grown native oxide does not guarantee that there is no interfacial oxide because the presence of oxidant and excitation very often leads to the growth of an oxide on the substrate surface. When SiO_2 thin films were deposited on Si, Ge, GaAs, and CdTe using remote plasma-enhanced chemical vapor deposition (RPECVD), the substrates were slightly consumed by plasma-activated species that diffused though the deposited oxide layer and oxidized the underlying substrate.[6–8] These parasitic reactions, or subcutaneous oxidation, during oxide film deposition by the RPECVD process degrade the electrical characteristics of the interface. To prevent the subcutaneous oxidation of the GaAs and Ge, a thin sacrificial Si layer was deposited before the deposition of the SiO_2 thin film.[6–8] To prepare a device-quality Si-SiO_2 interface and dielectric bulk film (SiO_2), the superficially thin oxide layer (~0.6 nm) is formed on the silicon substrate by a remote plasma-assisted oxidation (RPAO) process, and the remainder of the oxide layer is deposited by a RPECVD process.[9] After formation of ~0.6 nm of oxide in ~15 s, the oxidation rate slows down to ~0.3–0.4 nm/min. Therefore, during plasma-enhanced deposition at rates of ~2.5–5 nm/min, plasma-activated O species are consumed faster by deposition reactions with SiH_4 than by continued oxidation at the buried Si-SiO_2 interface.[10] The same RPAO-RPECVD process has been applied to SiC,[11] Ge,[12] and GaN[13] and has yielded a semiconductor-dielectric interface with reduced net oxide charges compared with the direct deposition of SiO_2 film on a semiconductor substrate.

On the other hand, the low D_{it} of GaN MIS systems also contributed to the possible underestimation of the actual D_{it}. In a wide-band-gap semiconductor, the Terman method at

[a)]Author to whom correspondence should be addressed; electronic mail: gerry_lucovsky@ncsu.edu

room temperature can lead to gross underestimation of D_{it} because interface states more than ~0.6 eV above the valence (or below the conduction) band edge cannot follow changes in dc bias at room temperature.[14] Therefore, high-temperature or photoassisted capacitance-voltage (C-V) measurements have been suggested to estimate D_{it} over a significant portion of the wide band gap. The present work suggests another introduced error in the estimation of D_{it} using the Terman method due to the wide band gap of GaN. The Terman method relies on a high-frequency C-V measurement at a sufficiently high frequency that interface traps are assumed not to respond, but they respond to the slowly varying dc gate voltage and cause the C-V curve to "stretch out" along the gate voltage axis as interface trap occupancy changes with gate bias.[15,16] In the estimation of D_{it} using the Terman method, it is well known that doping concentration should be known exactly to compare the difference between the measured and calculated C-V curves. However, doping concentration for calculated C-V curves has been selected until a close fit of C-V curves was obtained over the entire voltage range because the C-V characteristics of GaN MOS capacitors showed deep depletion instead of inversion. Then, the C-V curve "stretch" associated with uniformly distributed D_{it} could be misinterpreted as an increased doping concentration, and can lead to the underestimation of D_{it}. The high-low frequency method or conductance method, which does not require a theoretical curve to compare with the measured curve, can be considered to reduce the uncertainty associated with doping concentration in C-V characterizations of the GaN MOS system. However, due to high series resistance (R_s) and system noise, a quasistatic or low (below 100 Hz) frequency C-V curve has not been reported, and the conductance method has been used on occasion for GaN MOS analysis. In addition, there are side contact effects on the capacitance properties[17] for the MOS system using thin epitaxial layers grown on insulating substrates. For the GaN MOS structures, it is also difficult to properly extract the oxide-fixed charge from the flat-band voltage shift (ΔV_{fb}). The extraction of the fixed charge from ΔV_{fb} has several uncertainties, such as the (i) compensated effect[14] among several types of charge, (ii) uncertain doping concentration of GaN MOS system, which was usually obtained from a close fit of the C-V curve, and (iii) assumption of both the electron affinity of GaN and work function of the Al gate as 4.1 eV.

In this work, the occurrence of subcutaneous oxidation of GaN during plasma-enhanced deposition of SiO_2 films has been studied using Auger electron spectroscopy (AES) measurements. The quality of the interface and dielectric layer with/without RPAO process was investigated by fabricated GaN MOS capacitors.

II. EXPERIMENT

The epitaxial GaN (0001) layer was grown directly on the c plane of sapphire by hydride vapor-phase epitaxy (Technologies Devices International, Inc.). Silicon was used as n-type dopant, and the thickness of the GaN epitaxial layer was 5 μm. The as-grown GaN layer had an electron concentration of $5-10\times10^{17}$ cm^{-3}. As-received 2-in. GaN epiwafers on sapphire were degreased in organic solvents (acetone, methanol), for 20 min in each solvent. After wet-chemical treatments using 1:1:5 $NH_4OH:H_2O_2:H_2O$ solution at ~80 °C and etching in 1:5 $NH_4OH:H_2O$ solution at ~80 °C, the GaN samples were loaded into a multichamber system,[10] which provided a separate remote plasma-assisted process and on-line AES measurement.

To investigate the initial stages of oxidation of the GaN surface, AES measurements using a 3-keV electron beam were performed following each process step. The as-loaded GaN sample was exposed to reactive species from a remote N_2/He discharge at 0.02 Torr to reduce residual contaminants after wet-chemical treatments.[18] Superficially thin GaO_x (~1 nm), with a composition close to Ga_2O_3 or $x\sim1.5$, was formed by the RPAO process at 0.3 Torr using O_2 source,[18] and a thin SiO_2 film was deposited by the RPECVD process at 0.3 Torr.[10] The substrate temperature was 300 °C, and plasma power was 30 W at 13.56 MHz. The experimental procedure was to alternate AES measurements with the SiO_2 deposition for 20 s, i.e., interrupted processing and AES analysis cycles.

For the fabrication of GaN MOS capacitors, SiO_2 films were deposited onto wet-chemical-treated GaN samples with/without RPAO. After gate dielectric insulator deposition, the sample was rapid-thermal annealed at ~900 °C for 30 s in Ar atmosphere. A 300-nm-thick Al layer was evaporated and defined by the conventional lithography process. For GaN MOS capacitors without RPAO, postmetallization annealing (PMA) was performed at 400 °C for 30 min in forming gas (N_2/H_2). The electrical properties of GaN MOS capacitors were investigated using an HP 4284A (precision inductance-capacitance-resistance meter). The area of the device being tested was 4×10^{-4} cm^2.

III. RESULTS AND DISCUSSION

A. Subcutaneous oxidation of GaN during deposition of SiO_2

To demonstrate subcutaneous oxidation of GaN during deposition of SiO_2, two different process sequences, shown in Fig. 1, were used: (a) a direct deposition of SiO_2 on GaN using the RPECVD process and (b) a two-step process, i.e., RPAO process to form a superficially thin RPAO oxide layer (~1.0 nm), or GaO_x with $x\sim1.5$,[18] and deposition of SiO_2 on GaN using the RPECVD process. Figure 2 displays differential AES spectra for (i) the *in situ* N_2/He-plasma-cleaned GaN sample, followed by (ii)–(vi) the SiO_2 deposition on the GaN sample for 20–160 s. After the N_2/He plasma treatment of the GaN surface, residual C and Cl were reduced below AES detection, and the AES peak ratio of O KLL and N KLL was ~0.06 (~0.1 monolayer of oxygen coverage on the GaN surface).[18] Increasing the deposition time of the SiO_2 film, the N KLL (~378 eV) and

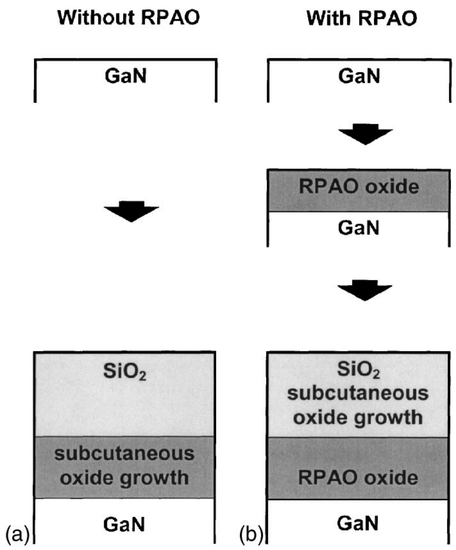

FIG. 1. Two different process sequences were used to demonstrate the presence of subcutaneous oxidation of GaN during deposition of SiO_2: (a) direct deposition of SiO_2 on GaN using RPECVD process and (b) two-step process, i.e., RPAO process to form a superficially thin RPAO oxide layer ($\sim$1.0 nm), or GaO_x with $x \sim 1.5$ and deposition of SiO_2 on GaN using RPECVD process.

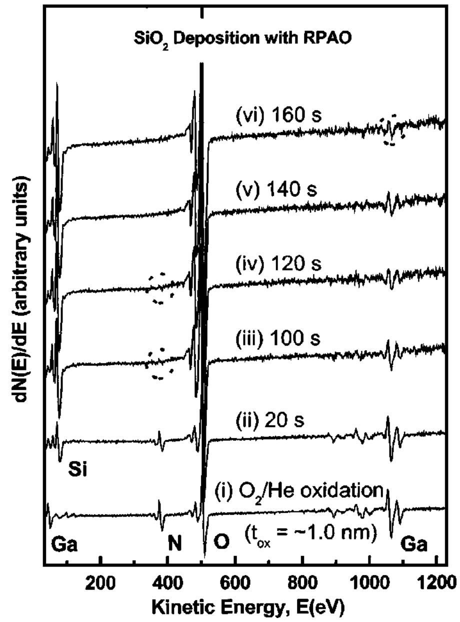

FIG. 3. Differential AES spectra for (i) RPAO process of GaN sample using O_2 source gas followed by (ii)–(vi) SiO_2 deposition on GaN sample for 20–160 s. Initial oxide thickness (t_{ox}) prior to SiO_2 film deposition on GaN sample was $\sim$1.0 nm.

Ga (*LMM*) ($\sim$1061 eV) features mainly associated with Ga–N bonding in the GaN substrate decreased in strength, whereas the O *KLL* ($\sim$506 eV) feature mainly associated with O–Si bonding in the deposited oxide layer increased. Figure 3 displays differential AES spectra for (i) the RPAO process of the GaN sample using O_2 source gas, followed by (ii)–(vi) the SiO_2 deposition on the GaN sample for 20–160 s. Note that the N *KLL* features of both samples in Figs. 2 and 3 disappeared at nearly the same SiO_2 deposition time, 120 s. In addition, the Ga *LMM* features of both samples show similar intensity after the deposition of SiO_2 for 160 s. This indicates that oxide thickness (t_{ox}) of both samples became similar after the deposition of SiO_2 film for 120 s.

Figure 4 shows a comparison of determined t_{ox} of GaN samples shown in Figs. 2 and 3 as a function of SiO_2 deposition time. Assuming the negligible dependence of electron escape depth on oxide overlayer, i.e., GaO_x or SiO_2, oxide thickness (t_{ox}) is obtained from (Ref. 18 and references therein):

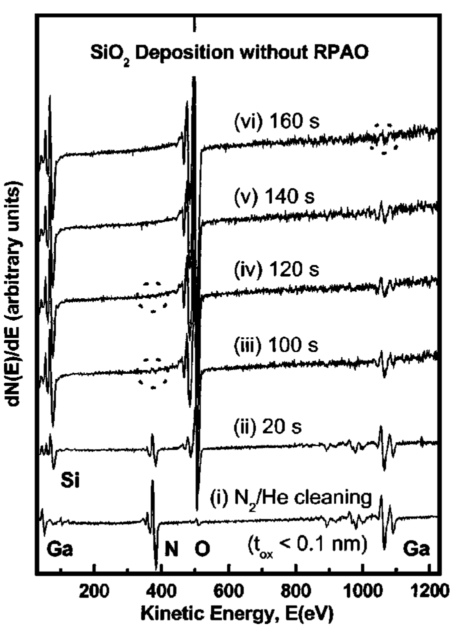

FIG. 2. Differential AES spectra for (i) *in situ* N_2/He-plasma-cleaned GaN sample followed by (ii)–(vi) SiO_2 deposition on GaN sample for 20–160 s. Initial oxide thickness (t_{ox}) prior to SiO_2 film deposition on GaN sample was below 0.1 nm.

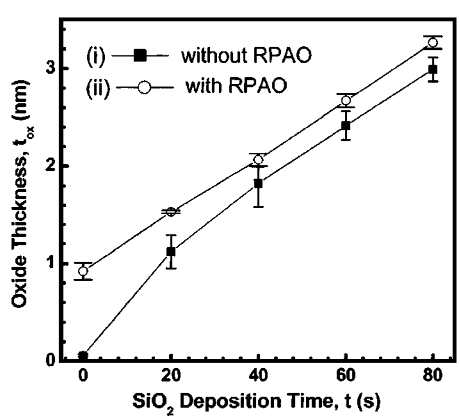

FIG. 4. Comparison of determined oxide thickness (t_{ox}) of both GaN samples, shown in Figs. 2 and 3, as a function of SiO_2 deposition time (t).

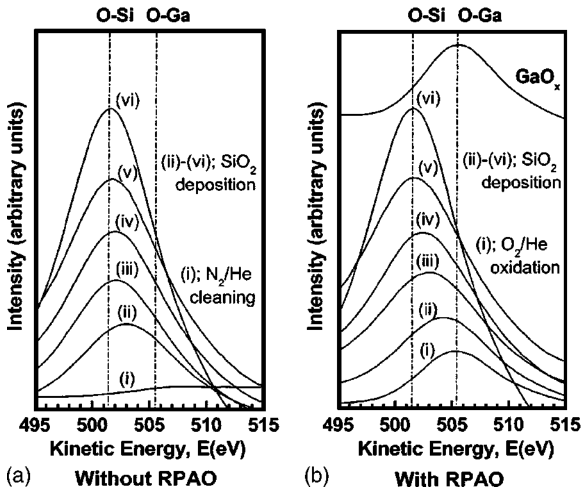

FIG. 5. Peak shift of nondifferentiated AES spectra by the SiO_2 deposition for (ii) 20, (iii) 40, (iv) 60, (v) 80, and (vi) 180 s on GaN samples (a) without RPAO and (b) with RPAO.

$$t_{ox} = \lambda \ln\left(1 + \frac{I^o_N}{I^o_O} \times \frac{I_o}{I_N}\right), \quad (1)$$

where I_N=N *KLL* Auger electron intensity from the GaN substrate, $I^o{}_N$=N *KLL* Auger electron intensity from the clean GaN substrate, I_O=O *KLL* Auger electron intensity from the thin GaO_x layer, $I^o{}_O$=O *KLL* Auger electron intensity from the thick GaO_x layer, and λ=electron escape depth for O and N, ~1 nm.

The difference of t_{ox} between two samples was gradually reduced by increasing SiO_2 deposition time from the initial value of ~1 nm, and saturated to ~0.3 nm. This reduction indicates that ~0.7 nm of GaO_x was formed during the direct SiO_2 deposition on the GaN sample without RPAO due to the subcutaneous oxidation process. The nearly linear SiO_2 deposition rate of the sample with RPAO means that negligible subcutaneous oxidation occurred, and ~1.0 nm of GaO_x using the RPAO process (or several monolayers of a sacrificial Si) can inhibit the subcutaneous oxidation process of GaN during the SiO_2 deposition.

Figure 5 displays the peak shift of nondifferentiated AES spectra by the SiO_2 deposition for (ii) 20, (iii) 40, (iv) 60, (v) 80, and (vi) 180 s on GaN samples (a) without RPAO and (b) with RPAO. The nondifferentiated AES spectrum of a thick GaO_x sample, obtained by remote O_2/He plasma oxidation of the GaN sample for 30 min, is included as a reference in Fig. 5(b). The AES O *KLL* feature at ~505.5 eV of the GaN sample with RPAO, shown in Fig. 5(b), gradually shifts to lower energy as the SiO_2 deposition time increased. This gradual peak shift (~4 eV) of the O *KLL* feature indicates that O-Ga bonds change to O-Si bonds. For the direct deposition of SiO_2 on a cleaned GaN sample without RPAO, shown in Fig. 5(a), the O *KLL* feature after the deposition of SiO_2 for 20 s was located ~1.5 eV higher position than that of thick SiO_2 films (>3 nm) and gradually shifted to lower energy as the SiO_2 deposition time increased. This peak shift

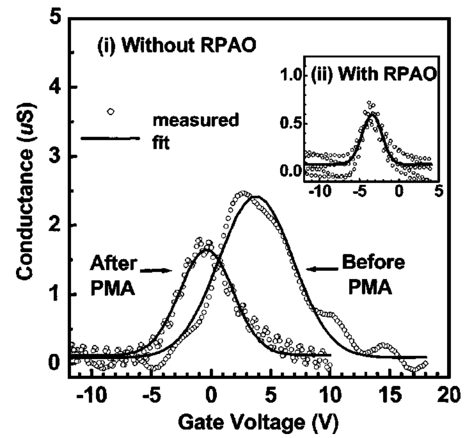

FIG. 6. Conductance-voltage (*G-V*) characteristics of GaN MOS capacitors (i) without RPAO before/after PMA and (ii) with RPAO measured at room temperature and 1 MHz in the dark.

demonstrates that thin GaO_x, or subcutaneous oxide, was formed during the direct SiO_2 deposition on the GaN sample.

B. GaN MOS system with/without RPAO

The quality of the interface and dielectric layer (i) without and (ii) with the RPAO process was compared by the fabricated GaN MOS capacitors. The RPAO process was performed for 30 s to form the RPAO oxide of ~1.0-nm thickness, and the RPECVD process was performed for 12 min to deposit SiO_2 of ~40-nm thickness. Note that both MOS capacitors (i) without RPAO and (ii) with RPAO have an interfacial GaO_x layer below the SiO_2 film because subcutaneous oxide (~0.7 nm) was formed at the sample without RPAO. In this section, we discuss a significant role of (i) subcutaneous oxide and (ii) RPAO oxide in determining the electrical properties of the semiconductor/oxide interface. Compared to the MOS sample with RPAO, the sample without RPAO showed a large ΔV_{fb} to the positive voltage direction and frequency dependence in the depletion region. Postmetallization annealing (PMA) was performed for the sample without RPAO at 400 °C for 30 min in forming gas (N_2/H_2), as well as for all of the samples with the RPAO step.

We measured conductance-voltage (*G-V*) characteristics of GaN MOS capacitors (i) without RPAO before/after PMA and (ii) with RPAO before PMA at room temperature and 1 MHz. Figure 6 displays the measured *G-V* curves that have clear peaks of interface trap reduction. The value of R_s determined from measured capacitance and conductance in accumulation was ~50–70 Ω. This relatively low value of R_s for the GaN MOS system is attributed to thick (~5-μm) GaN epilayer with high doping concentration (~$5-10\times10^{17}$ cm^{-3}). The low and symmetric base line of the *G-V* curve indicates that there are no significant trapping effects and charge injection into the superficially thin RPAO oxide. For the electron-beam-deposited Ga_2O_3 film, where the Ga_2O_3 was used as a bulk oxide of the MOS system,[19,20] interface trap loss is masked by high oxide loss. The conductance peak heights of samples (i) without RPAO before

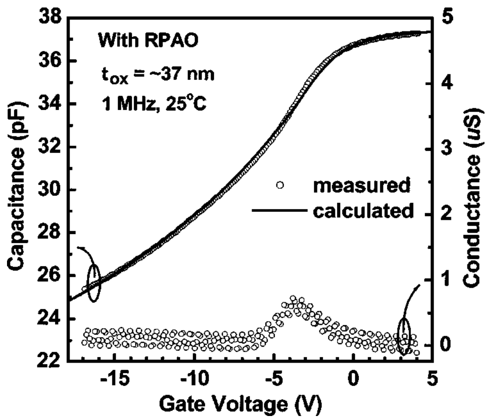

FIG. 7. Calculated and measured *C-V* curve of the GaN capacitor with RPAO at room temperature and 1 MHz. Also shown is the measured conductance.

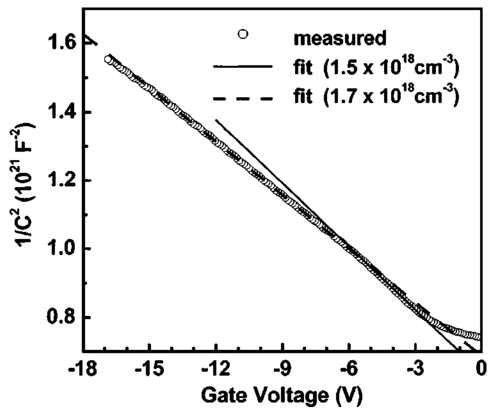

FIG. 8. $1/C^2$ characteristics as a function of gate voltage. Net doping concentration (N_D) obtained from the slope was 1.5×10^{18} and 1.7×10^{18} cm^{-3}.

PMA, (ii) without RPAO after PMA, and (iii) with RPAO before PMA were ~2.4, 1.5, and 0.5 μS, respectively. Because these samples have nearly similar values of R_s and oxide capacitance (C_{ox}), D_{it} of each sample will be approximately proportional to the measured conductance peak heights.

To estimate the distribution of D_{it} using the Terman method, *C-V* curves of each sample were measured at room temperature and 1 MHz. In the evaluation of expressions for theoretical *C-V* curves,[15,16] the same fundamental constants as in a previous paper[21] were used. The relative dielectric constant of GaN is taken as 9.5. The intrinsic carrier concentration (n_i) is 2.0×10^{-10} cm^{-3} for GaN at room temperature. Both the electron affinity of GaN and the work function of the Al gate are assumed as 4.1 eV. Figure 7 shows the measured and calculated *C-V* curves of the GaN MOS capacitor with RPAO. Also shown is the measured conductance. The calculated *C-V* curve was obtained using a net donor concentration (N_D) of 1.7×10^{18} cm^{-3} and fixed oxide charge of 3.5×10^{11} cm^{-2} (or ΔV_{fb} of −0.6 V). These values were determined from a close fit of the measured *C-V* curve over the entire voltage range. The measured *C-V* curve shows a small deviation from the calculated *C-V* curve between −1 and −7 V. Note that this deviation cannot be attributed to interface states because the measured curve is sharpened, rather than stretched. Figure 8 displays the $1/C^2$-*V* characteristics. Two linear lines fit the characteristics, and N_D obtained from the slope increased from the initial value of 1.5×10^{18} cm^{-3} to 1.7×10^{18} cm^{-3}. It is not clear whether this result is caused by the actual change in N_D or by voltage and capacitance changes associated with interface states. Figure 9 shows the distribution of D_{it} by applying the Terman method. The minimum D_{it} was estimated as $\sim1\times10^{11}$ cm^{-2} eV^{-1} at ~0.45 eV below the conduction band edge. For the sample without RPAO before/after PMA, as shown in Fig. 10, there was a reduction of the stretch-out in the measured *C-V* curves. When the measured *C-V* curves were partially fit above ~30 pF, measured curves agreed with calculated curves. N_D was 2.7×10^{18} cm^{-3} for the sample before PMA and 2.0×10^{18} cm^{-3} for the sample after PMA. These results indicate that the *C-V* curve stretch-out along the gate voltage axis, which is associated with interface trap occupancy changes, can sometimes be misinterpreted as an increased value of N_D.

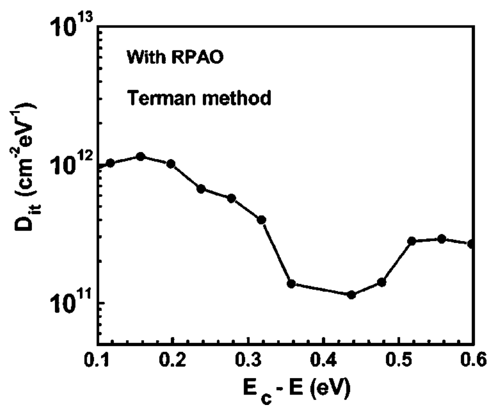

FIG. 9. Distribution of the density of interface state (D_{it}) of GaN MOS capacitor with RPAO using Terman method.

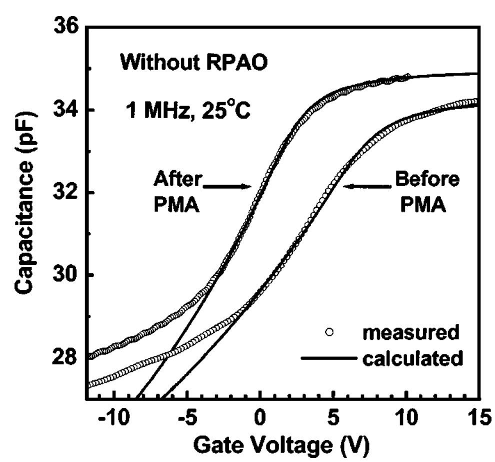

FIG. 10. Calculated and measured *C-V* curve of the GaN capacitors without RPAO before/after PMA at room temperature and 1 MHz.

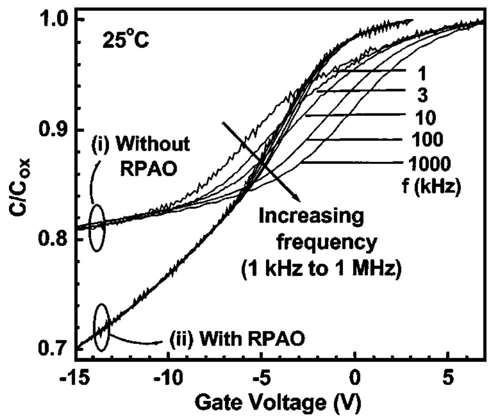

FIG. 11. Frequency dependence (1 kHz to 1 MHz) of the *C-V* characteristics of GaN MOS capacitors (i) without RPAO after PMA and (ii) with RPAO.

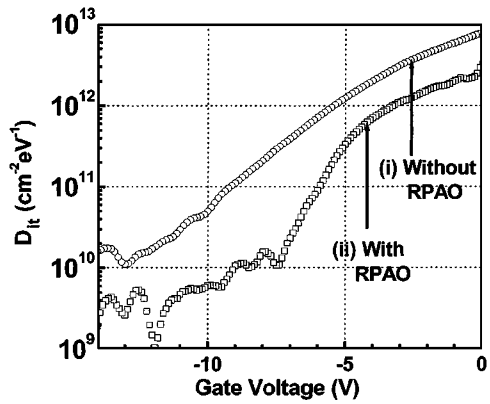

FIG. 12. Density of interface state (D_{it}) of GaN MOS capacitors (i) without RPAO and (ii) with RPAO using the high-low frequency method. The minimum D_{it} was determined at the gate voltage where low and high *C-V* curves showed the maximum capacitance difference (ΔC_{max}). Then, minimum D_{it} of (i) without and (ii) with RPAO was $\sim 4\times 10^{12}$ cm^{-2} eV^{-1} at −2.5 V and $\sim 7\times 10^{11}$ cm^{-2} eV^{-1} at −4.1 V, respectively.

Because the high-low frequency method does not require a theoretical curve to compare with the measured curve, this method can reduce the uncertainty of the extraction of D_{it} associated with doping concentration. In this study, *C-V* curves measured at 1 MHz and 3 kHz were used as high- and low-frequency *C-V* curves, respectively. The actual D_{it} will be higher than the estimated value using this method because the 3-kHz frequency is not sufficiently low that slow interface traps respond. In addition, the gate voltage where low and high *C-V* curves showed the maximum capacitance difference (ΔC_{max}) can be used to estimate the energy level of the traps contributing to D_{it}. The capacitance difference between low and high frequency is due to the electron emission and capture by interface states. If each energy level has the same values of D_{it} and time constant of electron emission, the capacitance difference will be continuously increased with gate bias sweep from accumulation to depletion. In fact, the capacitance difference showed a maximum value and gradually decreased to a negligible value because the time constant for electron emission from interface states increased exponentially with energy from the conduction band edge. Then, a limiting energy where D_{it} can be investigated without underestimation will be obtained at the gate voltage of ΔC_{max}. Figure 11 shows the frequency dependence (1 kHz to 1 MHz) of the *C-V* characteristics of GaN MOS capacitors (i) without RPAO after PMA and (ii) with RPAO. The gate voltage was swept from positive to negative voltage at room temperature. Figure 12 shows the distribution of D_{it} as a function of gate voltage calculated from[15,16]

$$D_{it} = \frac{C_{ox}}{q}\left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}}\right), \qquad (2)$$

where C_{lf} is the capacitance measured at low frequency (or 3 kHz) and C_{hf} is the capacitance measured at high frequency (or 1 MHz). The minimum value of D_{it} was determined at the gate voltage where low and high *C-V* curves showed ΔC_{max}. For the *C-V* curves measured at 1 MHz, shown in Fig. 11, the values of C/C_{ox} at the voltage of ΔC_{max} were $\sim$0.88–0.89. This small difference in the values of C/C_{ox} indicates that the minimum D_{it} was determined at the similar energy level. The minimum value of D_{it} (i) without the RPAO was $\sim 4\times 10^{12}$ cm^{-2} eV^{-1} at −2.5 V, and (ii) with RPAO was $\sim 7\times 10^{11}$ cm^{-2} eV^{-1} at −4.1 V. Figure 13 shows the distribution of D_{it} over the band-gap energy near the conduction band edge using the Terman method and the high-low frequency method. When the extracted values of D_{it} were compared at $\sim$0.3 eV, where ΔC_{max} was observed, D_{it} using the Terman method is $\sim$2 times smaller than that using the high-low frequency method. Note that the calculated curve without D_{it} was obtained using N_D from a close fit of the *C-V* curve, and the actual energy level for minimum D_{it} was located at a level deeper than $\sim$0.3 eV.

The conductance method was also used to clarify the estimated D_{it} using the high-low frequency method. Figures 14 and 15 show the parallel conductance loss (G_p/ω) versus angular frequency (ω) curves at selected gate voltages. Assuming negligible series resistance, G_p/ω was obtained from[16]

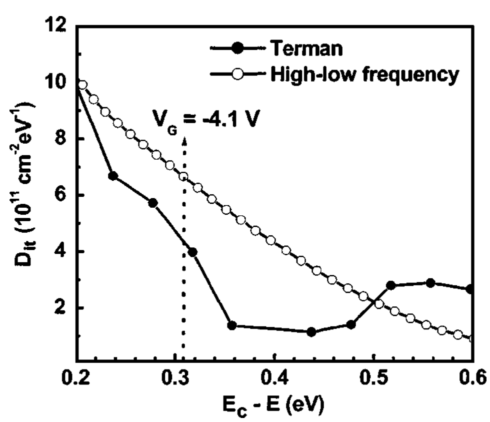

FIG. 13. Distribution of the density of interface state (D_{it}) of GaN MOS capacitor with RPAO using the Terman method and the high-low frequency method.

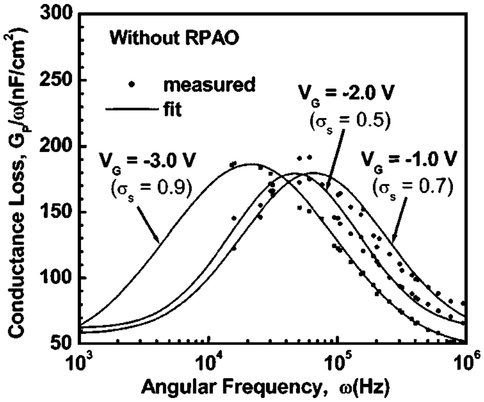

FIG. 14. Parallel conductance loss (G_p/ω) vs angular frequency (ω) curves measured at 25 °C for GaN MOS capacitor without RPAO after PMA. The graphically determined standard deviation of band bending (σ_s) was 0.5–0.9 (in the unit of kT/q).

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{\mathrm{ox}}^2}{{G_m}^2 + \omega^2 (C_{\mathrm{ox}} - C_m)^2}, \tag{3}$$

where G_m is the measured conductance and C_m is the measured capacitance. From the graphically determined standard deviation of band bending (σ_s) and universal function (f_D) as a function of σ_s, D_{it} of each sample was calculated from[16]

$$D_{\mathrm{it}} = \left(\frac{G_p}{\omega}\right)_{f_p} [q f_D(\sigma_s)]^{-1}, \tag{4}$$

where f_p is the frequency corresponding to the peak value of G_p/ω. The determined values of f_D were about 0.34–0.38 for the sample without RPAO and 0.24–0.26 for the sample with RPAO. Figure 16 shows D_{it} from the conductance measurements in Figs. 14 and 15, along with D_{it} from the high-low frequency method in Fig. 12. Both methods indicate well that D_{it} of (i) without RPAO after PMA is ~5 times larger compared to that of (ii) with RPAO. Therefore, it is clear that the two-step (RPAO-RPECVD) process can effectively reduce D_{it} of the GaN MOS system.

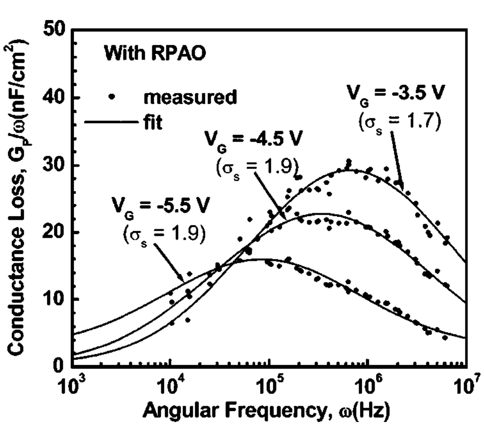

FIG. 15. Parallel conductance loss (G_p/ω) vs angular frequency (ω) curves measured at 25 °C for GaN MOS capacitor with RPAO. The graphically determined standard deviation of band bending (σ_s) was 1.7–1.9 (in the unit of kT/q).

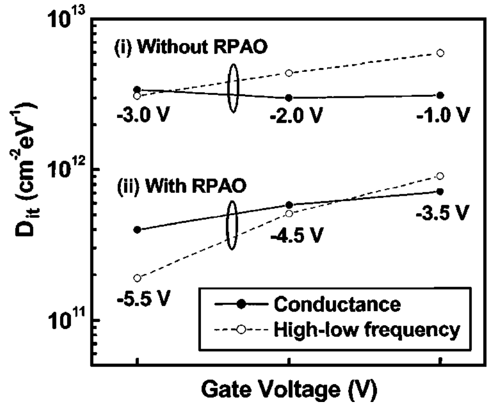

FIG. 16. Density of interface state (D_{it}) of GaN MOS capacitors (i) without RPAO after PMA and (ii) with RPAO using the conductance method and the high-low frequency method.

C. High-temperature and photo-assisted *C-V* measurements

The high-temperature *C-V* method[22–24] and photoassisted *C-V* method[21,22,25] have been used to estimate D_{it} over a significant portion of the wide band gap. The GaN MOS sample with RPAO was investigated using these two methods.

Figure 17 shows the *C-V* characteristics measured at 25°–200 °C in the dark. Also shown is the change in polarization charge (ΔQ) (Ref. 23) by increasing temperature. As reported by Matocha, Chow, and Coutmann,[23] our *C-V* curves also showed a positive shift with increasing temperature. They reported that their large positive shift (~2 V) was caused by the pyroelectric polarization of GaN because the change in the semiconductor bulk potential (E_c-E_f) and interface trap charge (Q_{it}) with increasing temperature make ΔV_{fb} (below 0.1 V) negligible in the negative-voltage direction. For the capacitor with RPAO, shown in Fig. 17, calculated ΔV_{fb} from the change in E_c-E_f was about −0.06 V with increasing temperature from 25° to 200 °C. The determined pyroelectric charge coefficient was ~4.9×10^9 q/cm^2 K. As shown in Fig. 17, however, *C-V* curves

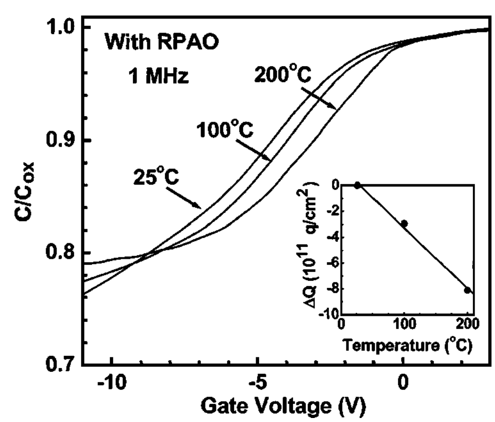

FIG. 17. *C-V* characteristics of GaN MOS capacitors with RPAO measured at 25°–200 °C in the dark. Also shown is the change in polarization charge (ΔQ) by increasing temperature Ref. 23.

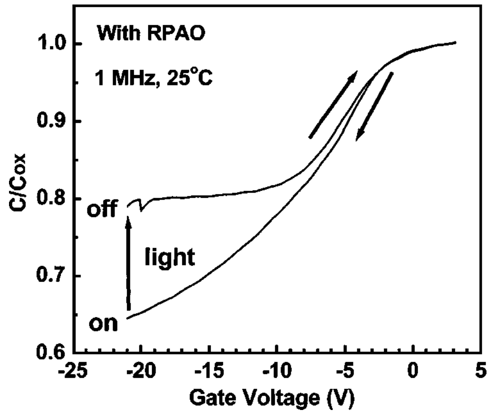

FIG. 18. Photoassisted *C-V* characteristics of GaN MOS capacitors measured at room temperature and 1 MHz.

were stretched along the voltage axis and flatten with increasing temperature. This indicates that electron-capture/emission-associated interface traps increased at high temperature and were not negligible in the measured positive shift of V_{fb}.

Figure 18 shows the photoassisted *C-V* characteristics measured at room temperature. The sweep rate of gate bias was 100 mV/s. From N_D of 1.7×10^{18} cm^{-3}, the threshold voltage was determined as about −18 V. The bias first swept from accumulation (+3 V) to deep depletion (−21 V) in the dark. While the bias remained at −21 V, the sample was illuminated by ultraviolet lamp (365 nm) until the measured capacitance saturated. After the capacitance saturated, the lamp was turned off and the bias was swept back to accumulation in the dark. Due to the higher photosaturated capacitance (~31 pF) than the expected inversion capacitance (~25 pF), "interface state ledge"[14,26,27] was not observed, and photoinduced hysteresis (ΔV_p) was obtained within the limited voltage range. Tungsten-bulb or microscope illumination can produce the same value of photosaturated capacitance with a reduced ΔV_p. The discrepancy between photosaturated capacitance and the expected inversion capacitance was also reported,[21,22] and was attributed to the small minority-carrier recombination rate, rather than to charge transfer from interface states.[22] In this study, the photosaturated capacitance was quite similar to the saturated capacitance measured at 200 °C, as well as that of MOS samples without RPAO.

Details of high-temperature *C-V* and photoassisted *C-V* will be discussed in a separate paper. It would be interesting to investigate the high-temperature *C-V* characteristics of nonpolar (or Ga- and N-terminated surface) GaN MOS structures as well as the photoassisted *C-V* characteristics by varying the gate-voltage sweep rate, and this will be presented in a separate paper.

IV. CONCLUSION

A low-temperature RPAO process for interface formation and passivation has been extended from Si and SiC to GaN. The process provides the control of ultra-thin interfacial layers that passivate the GaN substrate, preventing a parasitic or subcutaneous oxidation of the substrate during plasma deposition of SiO$_2$. Without the RPAO step, subcutaneous oxidation of GaN occurs during RPECVD deposition of SiO$_2$, and on-line AES indicates a ~0.7-nm subcutaneous oxide. A two-step process (RPAO-RPECVD) has been shown to result in significantly reduced interfacial trapping compared to a single-step SiO$_2$ deposition that does not include the RPAO step. The high-low frequency method and conductance method indicate that D_{it} of a GaN MOS sample without RPAO is ~5 times larger than that of the sample with RPAO. Improved GaN-dielectric interface properties will be obtained by changing the O$_2$/He plasma oxidation time to minimize RPAO oxide thickness as a superficially thin (~0.6–1.0-nm) oxide, followed by a remote plasma-assisted interface nitridation step that introduces approximately one monolayer of nitrogen atoms at the GaN-gallium oxide interface. Also, a post-oxide-deposition anneal and forming-gas anneal need to be investigated to obtain optimized processing conditions.

The remote plasma processing can be extended to the following applications: (i) the gate dielectric insulator of a GaN MOS field-effect transistor, (ii) the passivation layer of an AlGaN/GaN high-electron-mobility transistor (HEMT), and (iii) the intermediating layer prior to the RPAO process of other III-V materials such as GaAs and GaP. For the AlGaN/GaN HEMT, the RPAO oxide will be a mixture of Al$_2$O$_3$ and Ga$_2$O$_3$ because the RPAO process will be performed on AlGaN. For the GaAs and GaP devices, sacrificial GaN layers are formed prior to the RPAO process because the key of this study is the volatility of N-oxide species, e.g., NO and N$_2$O. The nonvolatility of As and P oxides means that the RPAO process cannot be applied directly to GaAs or GaP.

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