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LOW TEMPERATURE SILICON OXIDE AND FLUORINATED SILICON OXIDE FILMS PREPARED BY PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION USING DISILANE AS SILICON PRECURSOR

A Dissertation

Submitted to the Graduate Faculty of the
Louisiana State University and
Agricultural and Mechanical College
in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

in

The Department of Electrical and Computer Engineering

by
Juho Song
B.S., Kyungpook National University, Korea, 1985
M.S., Louisiana State University, 1994
August 1996

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To my late aunt, Taechul Song, who taught me my first letters in life.

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ABSTRACT

The deposition and characterization of the silicon oxide and fluorinated silicon oxide films, as interlevel dielectrics in microelectronics devices, prepared by plasma enhanced chemical vapor deposition at low substrate temperature using Si_2H_6 as silicon precursor are studied.

The film deposition is limited by the mass transport regime, resulting in nearly temperature independent deposition rate. The characteristics for the silicon oxide films deposited at 120°C show that the film etch rate is comparable to that obtained by TEOS-based PECVD at 400°C and the leakage current is comparable to that of the films deposited at 350°C with conventional SiH_4 precursor. It also shows that the as-deposited silicon oxide films have 9.4 % increase in the film density compared to the thermal silicon oxide films, resulting in the Si-O-Si bridging bond angle of 138°. The post-metallization annealing in forming gas ambient at 400°C rather than post-deposition annealing at high temperatures in N_2 is the most effective way to reduce both the oxide charge and interface trap densities, especially for devices fabricated on the native oxide-free surface.

For the fluorinated silicon oxide film deposition, the optimum gas flow ratio of CF_4, as fluorine precursor, to Si_2H_6 is observed to be in the range of 8-10. The films deposited at a flow ratio of 10 give the film a dielectric constant of 4.25 which is 12 % lower than 4.88 obtained for the fluorine-free silicon oxide films. The addition of fluorine into Si-O network helps not only in reducing the effective oxide charges to as low as 1/6 of the value for the fluorine-free silicon oxide films, but also improves the breakdown property by significantly reducing early failures, resulting in the average dielectric breakdown field strength of 8.91 MV/cm.

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These films have a strong potential for the use as interlayer dielectric material making available a low temperature and high quality film deposition process for submicron device fabrication in the microelectronics industry.

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CHAPTER 1
INTRODUCTION

1.1 Overview

The present trend in the deposition of dielectric thin films for microelectronic integrated circuit applications is towards lower deposition temperatures. Low temperature deposition of dielectrics is advantageous for the reduction of diffusion related or temperature sensitive phenomenon such as hillock formation in metals, dopant redistribution, and lattice damage and stoichiometry degradation in compound semiconductors [1].

Numerous studies [2]-[6] have reported deposition of silicon oxide films as primary dielectric films for applications such as passivation layers, intermetal insulators, and lithographic masks. Recently, attention has also been given to the silicon oxide films as primary insulators in thin film transistors based on amorphous or polycrystalline silicon [7], enabling one to fabricate large arrays of thin film transistors for flat panel displays in conjunction with liquid crystal display technology to replace conventional cathode-ray tubes.

One of the widely preferred low temperature techniques for the deposition of the silicon oxide films is plasma enhanced chemical vapor deposition (PECVD). In the low pressure glow discharge plasma, high electron energy takes the place of thermal energy in activating the desired chemical reactions by dissociating the chemical vapor molecules to produce highly reactive free radicals. Properties of the PECVD silicon oxide films have been extensively studied in recent years, with regard to their applications in integrated circuits.

The PECVD silicon oxide films are typically obtained in the temperature range of 200-350°C by the chemical reaction of a silicon containing compound

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such as silane (SiH_4) or tetra-ethyl-ortho-silicate (TEOS, $Si(OC_2H_5)_4$) with a gaseous oxidant such as O_2, N_2O, and CO_2 [7]-[14]. In general, O_2 is not recommended in conventional PECVD due to its high reactivity with SiH_4, which may result in a general reduction in film quality, including nonreproducible deposition, increased particulates and pinhole densities, and nonuniform deposition [15]. Typically N_2O has been the oxidant of choice due to the low bonding energy (2.08 eV) of N-O in the molecule [16].

Numerous works have been reported on the physical, mechanical, and chemical properties of the silicon oxide films deposited by the use of SiH_4 as silicon precursor. The SiH_4-based PECVD silicon oxide process, however, possesses deposition temperature limitation, especially below 200°C. PECVD silicon oxide films deposited at temperature lower than 200°C show poor film integrity caused by undesirable chemical bonding groups. Though the use of helium as a dilution gas during the film deposition minimizes the formation of these bonding groups, the dilution process itself causes a significant decrease in the film deposition rate [10]. To compensate for the decrease in the deposition rate for the latter process, one requires either the use of much higher deposition temperatures which would be against the desirable trend or an increase in the deposition time which causes concern about the unwanted plasma radiation induced device degradation.

Disilane (Si_2H_6) is known to give better thermal processing budget to prepare silicon containing films due to its high reactivity resulting from the fact that Si_2H_6 has quite a long surface residence time and a high sticking coefficient compared to those for SiH_4 [17], [18]. The pyrolysis of Si_2H_6 was studied first by Emeleus and Reid [19] in 1939 and then modeled experimentally by Bowrey and Purnell [20] in 1971. Roenigh *et al.* [21] reported Arrhenius parameters for SiH_4 and Si_2H_6 decomposition kinetics. According to their study, activation

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energies for SiH_4 and Si_2H_6 were 57.4-61.1 kcal/mol and 51.1-52.5 kcal/mol, respectively. The important contribution towards understanding of Si_2H_6 chemistry was due to Gates [15] who analyzed the rates and mechanisms of chemisorption on the silicon surface for SiH_4 and Si_2H_6 and confirmed that the reactive sticking coefficient at room temperature, S^R, for SiH_4 was less than 0.001 (~ near zero coverage) on silicon (111) surface, while S^R for Si_2H_6 was 0.47. This suggests that the reactivity of Si_2H_6 over SiH_4 is at least 1000 times greater on a clean surface.

The first successful usage of Si_2H_6 was towards deposition of silicon films by molecular beam epitaxy [22] and showed advantages of the Si_2H_6-based process in preparation of epitaxial films at much lower deposition temperatures compared to the conventional SiH_4-based process. Gas-phase reaction mechanisms for the silicon oxide deposition from Si_2H_6 and N_2O for pyrolytic atmosphere CVD were modeled by Giunta *et al.* [23]. They suggested that rapid reaction of the decomposition products SiH_2 with N_2O, suppresses the formation of larger silicon hydrides, generates the film precursor, silanone(SiH_2O), and hence causes a strong dependence of the growth rate on Si_2H_6 concentration in presence of excess N_2O concentration. Several studies of Si_2H_6 application for the deposition of the silicon oxide films have been reported, mainly with the use of either excimer, ultraviolet, or synchrotron-induced photo CVD [18], [24]-[26].

1.2 General Principles of PECVD [27]

1.2.1 Nature of Plasma

The primary role of plasma is to produce chemically active species that subsequently react via conventional pathways. A key factor is that substitution of electron kinetic energy for thermal energy avoids excessive heating and consequent degradation of substrates. The plasmas used for semiconductor

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application are produced by the application of a high frequency electric field across a body of gas and are weakly ionized gases comprising of electrons, ions, and neutral species. The electron concentration ranges from 10^9 to 10^{12} cm^{-3}, the ratio of concentration of the charged species to neutral species ranges from 10^{-6} to 10^{-4}, and the electron energy varies from 1-20 eV. One important characteristic of the glow discharge plasma is the electron temperature (10^4-10^5 K), which is typically 30 to 1000 times greater than the average temperature for the ions and neutral species (25-300 K). This high electron energy relative to the low temperature neutral species makes the glow discharge useful in driving CVD reactions.

When the plasma process first starts, energy from the electric field is coupled into the gas almost entirely via the kinetic energy of a few free electrons. The electrons acquire energy rapidly from the applied electric field and lose it to collisions. Collisions between electrons and gas molecules in plasma can be characterized as either elastic or inelastic, according to whether or not the internal energies of the colliding bodies are maintained. In the elastic case, only a small amount of energy is transferred, while the inelastic case involves a much larger energy loss and the excitation of internal modes (electronic, vibrational or translations) of target molecules. Inelastic collisions between the high energy electrons and neutral molecules result in, among other processes, electron impact ionization and molecular dissociation. Electron impact ionization helps to sustain the glow discharge by producing secondary electrons. Meanwhile, molecular dissociation creates free radicals that contribute to the film deposition.

In many plasma deposition processes, inert carrier gases are normally used as carrier or dilute gases. At low pressure, inert gas can absorb electron energy from the glow discharge and be excited to metastable states which are

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summarized in Table 1.1. The metastable inert gas atoms can then transfer their energy to other reactant gases via inelastic collision. Thus, more ions and radical reactant gases are uniformly generated throughout the glow discharge. As a result, the deposition will be more uniform throughout the radius of reactor chamber.

1.2.2 Deposition Mechanism

The properties of plasma deposited films are strongly dependent on process parameters. Generally, the deposition mechanism of PECVD processes can be explained by four major steps. First, the primary reactions occur between electrons and reactant gases in the plasma to form a mixture of ions and free radical reactive species. Second, reactive species transport from the plasma to the substrate surface in parallel with various secondary inelastic and elastic reactions. Third, the reaction or adsorption of reactive species with or onto the substrate surface occurs. Finally, the rearrangement processes follow where active species or their reaction products incorporate into the film or re-emit from the surface back into the gas phase. However, many questions regarding plasma thin film deposition mechanism still remain unanswered.

In general, plasma deposition can be classified into two mechanisms, radical and ionic, depending on the type of species that interact with the solid surface during the plasma process. Both the radical and ionic mechanisms happen concurrently during the deposition process. Depending on the plasma process parameters, one mechanism may dominate the other.

1.2.2.1 Radical Mechanism

During the plasma deposition process, the generation rate and lifetime for neutral radicals are usually greater than they are for ions. These two effects make the radical concentration higher than that for ions. Hence, it is believed that neutral radicals are the major deposition agents under most deposition

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Table 1.1. Metastable energy levels and ionization energies of major inert gases used for thin film deposition in CVD.

Inert gas	Metastable energy (eV)	Ionization energy (eV)
He	19.8	24.53
Ne	16.6	21.56
Ar	11.5	15.76
Kr	9.9	14.0
Xe	8.32	12.13

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conditions. After being generated in the glow discharge and adsorbed on the substrate surface, the adsorbed radicals have to diffuse into a stable site to become a part of films. Surface diffusion of such adsorbed atoms is much slower, compared with diffusion in the CVD process, at normal plasma process temperature which is lower than 300°C.

At these low temperatures, surface diffusion and rearrangement of reactive species on the substrate become dominant and strongly affect the composition of weakly bonded and high diffusive species such as hydrogen. Thus, the films deposited at low temperatures normally contain more trapped radicals and defects. As a result, the films will be more porous and contain more hydrogen, resulting in poor thermal and electrical stability. The instabilities are due to a large amount of weakly bonded hydrogen that breaks easily under thermal or electrical stress and thus creates more dangling bonds in the film structure.

1.2.2.2 Ionic Mechanism

Coincidental with the large number of radicals generated during the plasma process, a small number of electron and ionic species are constantly bombarding the surface. Some ionic species react with the surface to become a part of the films, and others bounce off after neutralizing. Depending on the energy of the bombarding species and the surface state of the substrate, either deposition, densification, or sputtering may occur. Various ionic species exist during the plasma process with varying energies, so that all three reactions may happen at the same time. Because ionic species carry a charge, their attachment to the surface will be preferential. The constant bombardment of the surface by electrons and ions also speed up the rearrangement of adsorbed atoms on the substrate surface, resulting in higher compressive stress and a greater scratch resistance.

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1.3 Research Objectives

The research is directed towards developing a silicon oxide deposition process resulting in high quality and reliable films to be used as passivation layers and interlevel insulators in the integrated circuit fabrication. The work culminates in developing a fluorinated silicon oxide film deposition process.

In this work, the use of Si_2H_6, instead of SiH_4, as silicon precursor to deposit the films in PECVD is extensively studied for the first time in the history of silicon oxide film deposition process. The research is divided into two major parts which are the silicon oxide film deposition for the first phase and the fluorinated silicon oxide film deposition for the second phase, as shown in Fig. 1.1. The equipment used for the film deposition is a Plasma Therm model VII-70 parallel plate plasma reactor system which uses a 13.56 MHz rf plasma source and has 500 W maximum output power as shown in Fig. 1.2. The electrode spacing was held constant at 1 inch. The top electrode was always maintained at 60°C for the film deposition.

In chapter 2, the plasma process characteristics of the silicon oxide films as a function of various process parameters such as gas flow ratio of N_2O to Si_2H_6, rf input power, deposition temperature, total gas flow rate, and process pressure are addressed. This experiment enables not only to understand chemical reaction mechanisms but to optimize each and every process parameter that affects the film deposition and eventually the film properties.

In chapter 3, effect of deposition temperature on the chemical and electrical film properties is addressed with the help of chemical etch rate, infrared transmission spectroscopy, high-frequency capacitance-voltage (C-V) technique, and current-voltage (I-V) measurements. As the most important goal for this research is to decrease the deposition temperature as much as

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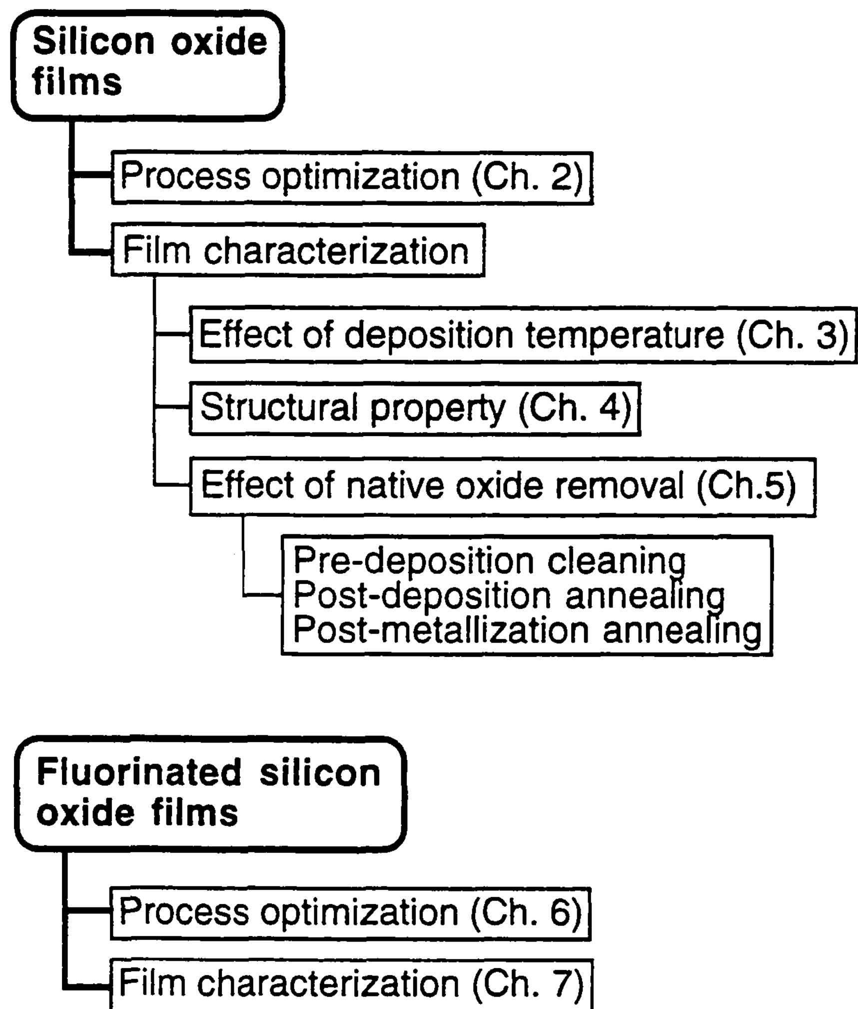

Fig. 1.1. Overall research outline. The research is divided into two major parts, silicon oxide and fluorinated silicon oxide film deposition.

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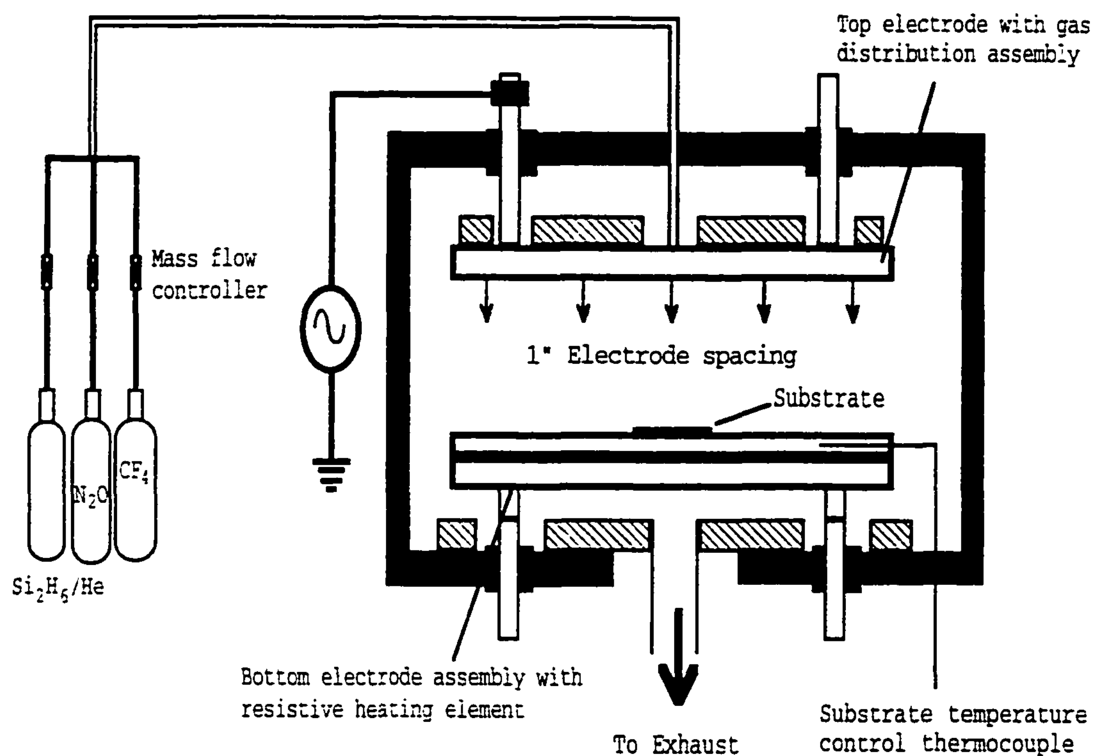

Fig. 1.2. Schematic diagram of a Plasma Therm VII-70 parallel plate plasma reactor equipped with 13.56 MHz rf source and 1 inch electrode spacing.

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possible, careful investigation is made to find the lowest viable deposition temperature.

In chapter 4, structural properties of the silicon oxide films annealed at various temperatures in the range of 300-1100°C are presented. The dependence of the physical and chemical properties of the silicon oxide films on the post-deposition annealing process is characterized.

In chapter 5, effect of the native oxide removal on the substrate surface prior to the silicon oxide film deposition is detailed. The electrical properties of the silicon oxide films derived from C-V and I-V measurements are studied. In addition, the effect of annealing the as-deposited films either in N_2 just after the film deposition or in forming gas ambient after the formation of metal electrode is discussed.

In chapter 6, deposition characteristics for the fluorinated silicon oxide films incorporating CF_4 as fluorine precursor into the silicon oxide deposition process, are addressed. The chemical and electrical film properties are examined as a function of flow rate ratio of CF_4 to Si_2H_6 in the film deposition process.

In chapter 7, electrical characterization details for the fluorinated silicon oxide films, deposited by the optimum deposition condition as derived from Chapter 6, are addressed. The results of C-V and I-V measurements are discussed. The improvements in film quality due to fluorine incorporation are summarized and comparisons made with the fluorine-free silicon oxide films.

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CHAPTER 2
SILICON OXIDE FILM DEPOSITION

2.1 Introduction

The many results presented in this chapter have been published in Journal of Electronic Materials, volume 24, pages 1507-1510, 1995. Their permission was gratefully acknowledged.

The deposition variables such as gas flow ratio of N_2O to Si_2H_6, deposition temperature, process pressure, total gas flow rate, and rf input power affect the film deposition in PECVD. It is necessary to understand these parameters that result in one mechanism becoming dominant between the radical and the ionic mechanisms, and how it effects the film properties. Therefore, each variable should be properly manipulated to optimize the film deposition process and to obtain high quality film properties. In this chapter, the first results on the silicon oxide films deposited by PECVD using Si_2H_6 and N_2O as silicon and oxygen precursors as a function of those variables in a conventional parallel plate plasma reactor are presented.

2.2 Experiment

Boron doped, chemically polished 10-20 Ω·cm silicon wafers with (100) orientation were used as the substrates. The film deposition was carried out without any in-situ cleaning. After loading the wafers into the process chamber, the chamber was pumped to a base pressure of 1×10^{-3} Torr. High purity N_2O (99.99 %) was then first introduced into the chamber, followed by a mixture of 4.8 % Si_2H_6 in helium. The deposition recipe in detail is shown in Fig. 2.1. The use of the inert gas, He, is known to increase the stoichiometry of the film by reducing the incorporation of hydrogen in SiH bonding groups, and of nitrogen in SiN and NH bonding groups [10].

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Parameter \ Step	1	2	3	4	5	6	Remark
N_2	→				→		
Si_2H_6			→	→			
N_2O		→	→	→			
CF_4			→	→			Fluorinated silicon oxide film
Chamber pressure			→	→			
Temperature	→	→	→	→	→	→	
rf power				→			
Time (min)	2	1.5	1	5-15	2	1.5	

Fig. 2.1. The detailed deposition recipe consisting of six different steps. The process chamber is pumped to a base pressure before starting step 1. The films are deposited during step 4.

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The thickness of the deposited silicon oxide films was measured by a Nanometrics 210XP thickness meter. Auger electron spectroscopy (AES) measurement on the films was carried out on a Physical Electronics model PHI-48 to determine the film composition. For the AES measurement, 100 nm thick silicon oxide film grown at 950°C by dry oxidation was used as a reference wafer to normalize the silicon and oxygen peaks. The etch rate was obtained by dipping the film for 1 min into P-etch solution consisting of 15 parts by volume 48 % HF, 10 parts by volume 70 % HNO_3, and 300 parts by volume of deionized water. Typical etch rate in the P-etch solution for the silicon oxide films prepared by various methods [7], [28] are summarized in Table 2.1.

2.3 Results and Discussion

Figure 2.2 shows the film deposition rate and the chemical etch rate in the P-etch solution as a function of the gas flow ratio of N_2O to Si_2H_6. The deposited silicon oxide film thicknesses are in the range of 100-150 nm for the 250°C deposition temperature. The rf input power and the process pressure was 50 W and 700 mTorr, respectively. The increase in the gas flow ratio results in decrease in both the deposition rate and the chemical etch rate. The increase in Si_2H_6 concentration causes higher film deposition rate presumably due to an increase in the number of active species in the glow discharge and drives the silicon oxide film more porous resulting in faster etch rate.

The gas flow ratio is the most important process parameter in determining the stoichiometry of the film [29]. The ratio for obtaining stoichiometric silicon oxide depends on the process condition used, as shown in Fig. 2.3. It can be seen that N_2O/Si_2H_6 ratios, which are smaller than 50, result in silicon-rich oxide films while the ratio in the range of 50-150 gives the stoichiometric silicon oxide films with the atomic ratio of silicon to oxygen equal to 50 %. At ratios higher than 150, the film becomes oxygen-rich.

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Table 2.1. Typical etch rate in the P-etch solution for the silicon oxide films prepared by various methods.

Films	Etch rate (nm/sec)
Sputtered silicon oxide	2-7
Atmospheric pressure CVD silicon oxide	1-2
Thermal silicon oxide	0.2
SiH_4-based PECVD silicon oxide	~ 1.6

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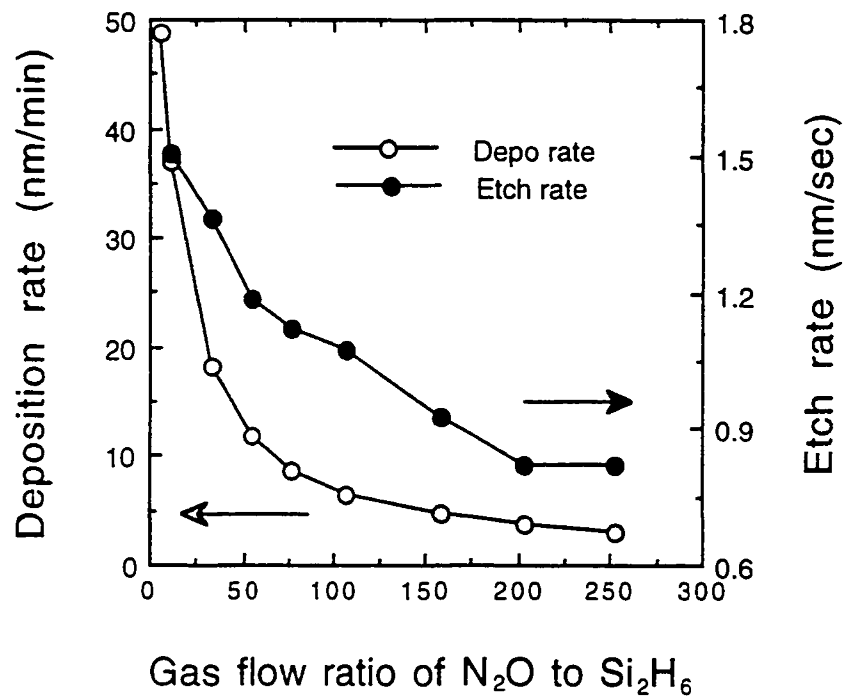

Fig. 2.2. Deposition rate and etch rate in the P-etch solution as a function of N_2O/Si_2H_6 gas flow ratio.

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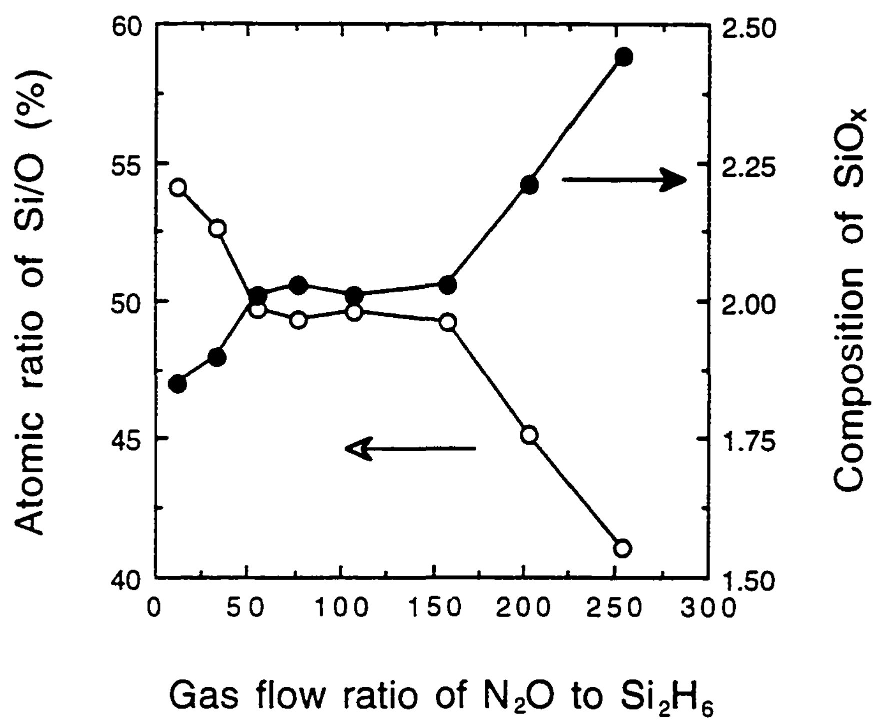

Fig. 2.3. Atomic ratio of silicon to oxygen and composition of SiO_x obtained from Auger electron spectroscopy measurements as a function of N_2O/Si_2H_6 gas flow ratio.

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The dependence of film deposition rate as a function of deposition temperature is illustrated in Fig. 2.4. The rf input power was 50 W, total flow rate was 140 sccm, and N_2O/Si_2H_6 flow ratio was 55. Under these experimental conditions, it is evident from Fig. 2.4 that the deposition is limited by the mass transport process. For pyrolytic atmosphere pressure CVD of the silicon oxide films using Si_2H_6 and N_2O as source materials, formation of a gas phase intermediary SiH_2O precursor has been suggested [23]. Disiloxane, $(SiH_3)_2O$, gas phase intermediary precursor has been suggested for the silicon oxide films in PECVD by using SiH_4 and N_2O [10]. These precursor molecules reach the surface and undergo surface reaction by which hydrogen is replaced by oxygen. It is quite likely that intermediary gas phase precursors are also formed in PECVD utilizing Si_2H_6 and N_2O. From Fig. 2.4, the deposition rate is seen to decrease with an increase in deposition pressure. This is consistent with lower flux of the active intermediary species transported to the surface through the boundary layer. Thermal dissociation study of Si_2H_6 has shown that Si_2H_6 partially dissociates on a clean silicon (100) surface even below room temperature [30]. Hence, Si_2H_6 can also contribute to film deposition observed in this study at low temperature.

The peak deposition rates are dependent on the process pressure and are observed to be 22 nm/min and 14 nm/min for the deposition pressure of 300 mTorr and 700 mTorr, respectively. The slight decrease in the deposition rate for higher deposition temperatures is believed to be due to the re-emission characteristics of the adsorbed active radical species on the surface. Films deposited at low deposition rate (7-15 nm/min) reveal reproducible deposition properties and good thickness uniformity of within ± 3 % across four inch diameter wafers.

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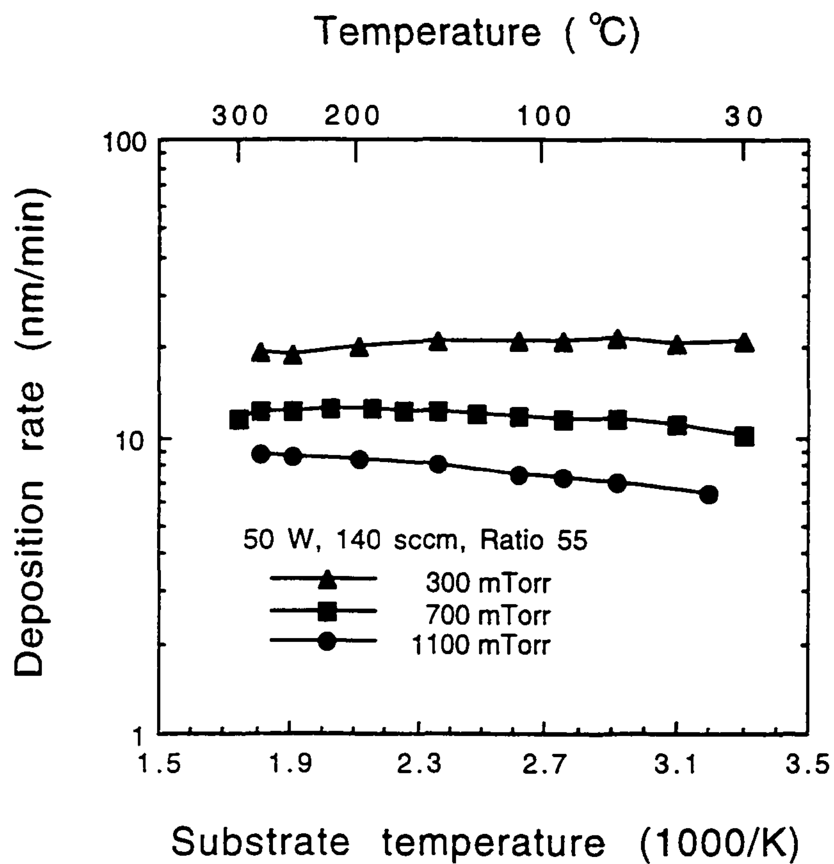

Fig. 2.4. Deposition rate as a function of temperature for the silicon oxide films deposited at 300, 700, 1100 mTorr.

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Deposition rate is plotted as a function of the total gas flow rate into the process chamber with the gas flow ratio of N_2O to Si_2H_6 held at a constant value in Fig. 2.5. The rf input power was 50 W, process pressure was 700 mTorr, and the deposition temperature was 250°C. As evident from this figure, the deposition rate increases with increase in the total flow rate with deposition pressure held constant. This observation is consistent with a mass transport limited process.

Figure 2.6 shows the chemical etch rate of the films as a function of deposition temperature at 50 W rf power, constant N_2O/Si_2H_6 ratio of 55, and constant gas flow rate of 140 sccm. The silicon oxide film deposited at room temperature at 300 mTorr has an etch rate of 7-8 nm/sec, which is four times faster than the etch rate of 1.7 nm/sec for the film deposited at 250°C at the same pressure. In addition, the silicon oxide films deposited at room temperature with higher pressure of 700 mTorr show almost twice the etch rate of 2.5 nm/sec, compared to 1.3 nm/sec etch rate of the silicon oxide deposited at 250°C. The faster etch rate for lower deposition temperature indicates less film integrity, which may be due to lower surface diffusion and rearrangement of active species on the substrate surface. For purposes of comparison, the P-etch solution used here etches silicon oxide films deposited at 350°C in PECVD utilizing SiH_4 at a rate of 1.6 nm/sec, as summarized in Table 2.1. This suggests that the etch rate of the Si_2H_6-based PECVD silicon oxide films deposited at 200°C is comparable to that of the SiH_4-based PECVD films deposited at 350°C.

The effect of the deposition rate on the rf discharge power is illustrated in Fig. 2.7 for three different pressure conditions. The deposition temperature is maintained at 250°C, total flow at 140 sccm, and the N_2O/Si_2H_6 ratio at 55. At low power (< 30 W), the reaction is limited by the number of active radical

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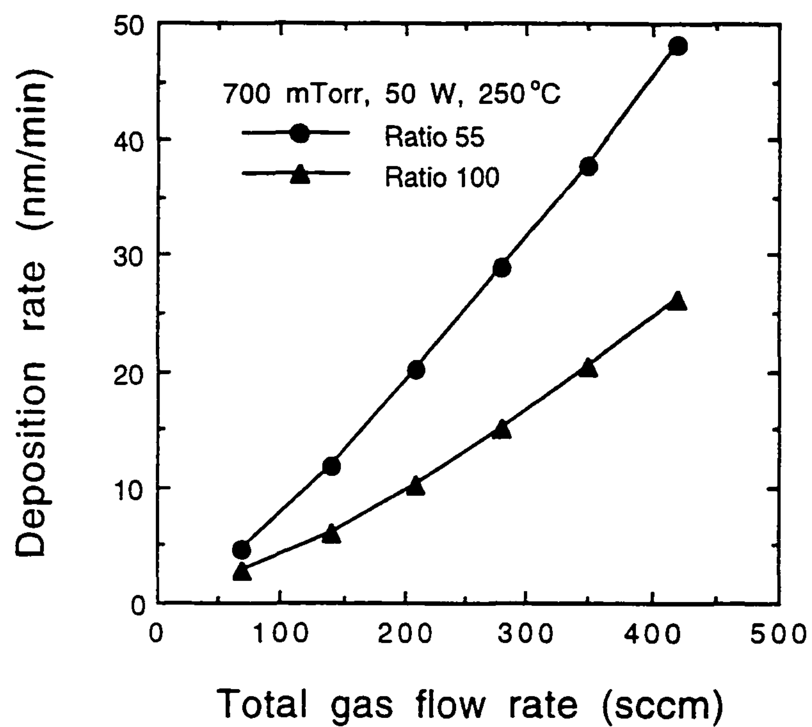

Fig. 2.5. Deposition rate as a function of total gas flow rate for the silicon oxide films deposited with N_2O/Si_2H_6 gas flow ratio of 55 and 110.

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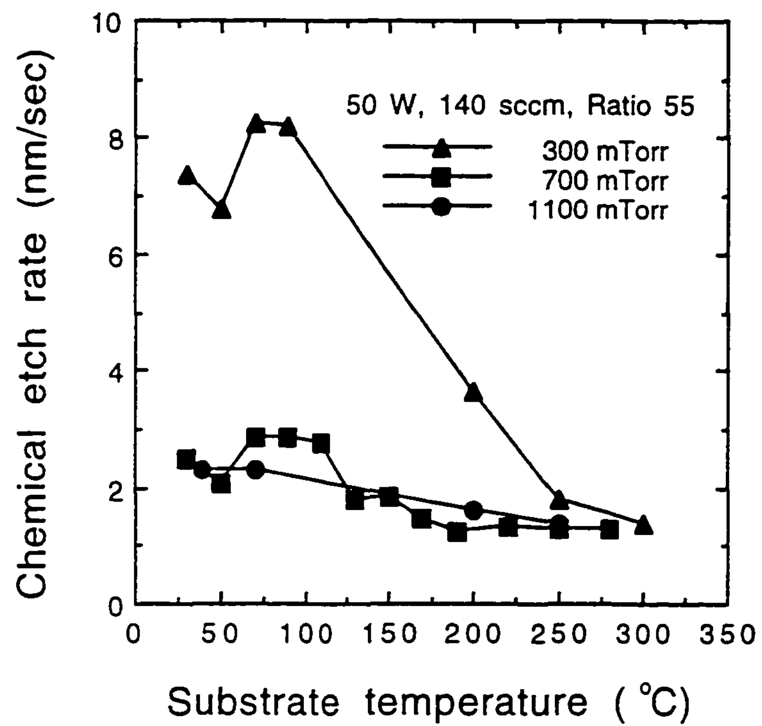

Fig. 2.6. Chemical etch rate in the P-etch solution vs. substrate deposition temperature.

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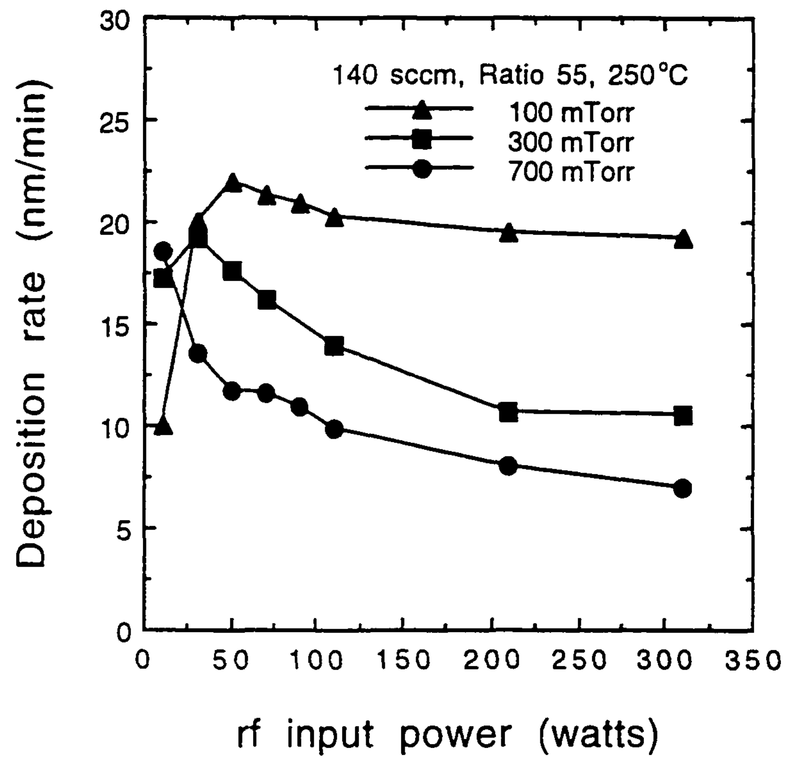

Fig. 2.7. Deposition rate as a function of rf input power for the silicon oxide films deposited at 100, 300, and 700 mTorr.

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species created in the glow discharge. The low chamber pressure causes an increase in the mean free path resulting in low deposition rate. As the rf power increases, the deposition rate saturates and then decreases. This decrease in the deposition rate with high power is mainly due to the sputtering effects caused by higher energy of the bombarding species [27].

The deposition rate and the etch rate as a function of the process pressures are shown in Fig. 2.8. The deposition rate in the mass transport controlled regime is strongly affected by a change in the total pressure and is proportional to the diffusivity of the active radical species in the boundary layer. The diffusivity in the boundary layer is inversely proportional to the total pressure. Increasing pressure decreases the number of species arriving on the substrate surfaces, thus causing a fall in the deposition rate from 22 nm/min at 100 mTorr to 6 nm/min at 1400 mTorr. The almost flat curve for pressures above 300 mTorr indicates lower dependence of etch rate on pressure. However, the etch rate has a minimum value of 1.3 nm/sec for the silicon oxide films deposited at 700 mTorr.

2.4 Conclusion

Stoichiometric, reproducible, and uniform PECVD silicon oxide films have been deposited between room temperature and 300°C using Si_2H_6 and N_2O as silicon and oxygen precursors, respectively. The dependence of film properties for processing parameters was investigated. The stoichiometric silicon oxide films were obtained when the gas ratio of N_2O to Si_2H_6 was in the range of 50-150. The deposition was also found to be nearly temperature independent indicating the mass transport limited regime. Films deposited at low deposition rate (7-15 nm/min) showed reproducible deposition properties and good thickness uniformity of within $\pm$ 3% across 4 inch diameter silicon wafers. The best process parameters were 700 mTorr for the pressure, 50 W

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for the plasma power, 50 for the gas flow ratio of N_2O to Si_2H_6, and 140 sccm for the total gas flow rate. The film deposition rate with this condition at the deposition temperature of 120°C was about 12-13 nm/min. This process shows significant promise as a low temperature substitute for the conventional SiH_4-based PECVD silicon oxide deposition process in the integrated circuit technology.

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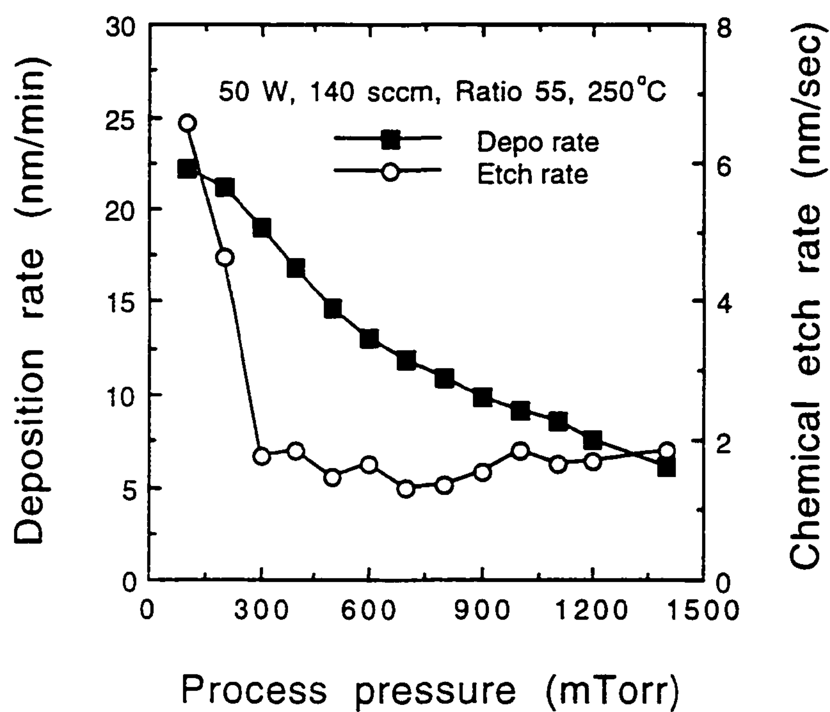

Fig. 2.8. Deposition rate and chemical etch rate vs. deposition pressure.

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CHAPTER 3
EFFECT OF DEPOSITION TEMPERATURE ON FILM QUALITY

3.1 Introduction

The many results presented in this chapter have been published in Thin Solid Films, volume 270, pages 512-516, 1995. Their permission was gratefully acknowledged.

Semiconductor devices are being scaled down to submicron dimensions to meet device requirements for high operaing speed, low power consumption, and high packing density. This requires the semiconductor industry to look for lower temperature processes. Silicon oxide is a common dielectric material in the integrated circuit technology for purposes such as interlevel isolation and dielectric passivation. It is desirable to deposit the silicon oxide films at as low a temperature as possible to avoid the various adverse effects accompanied with processing at elevated temperatures.

In this chapter, results of deposition of PECVD silicon oxide films at significantly lower temperatures using Si_2H_6, instead of SiH_4, as the silicon source, are presented. For the first time, the chemical and electrical characteristics of the silicon oxide films deposited in the temperature range of 30-250°C with the above Si_2H_6 process are studied. In particular, the effect of the film deposition temperature on the film properties measured by chemical etch rate, infrared transmission spectroscopy, high-frequency C-V technique, and I-V measurements are discussed.

3.2 Experiment

Boron doped, chemically polished 100 mm diameter p-type silicon wafers with (100) orientation and resistivity in the range of 5-15 Ω·cm were used as the substrate material. The chamber pressure during film deposition was kept at

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700 mTorr. The deposition rf power was 50 W. The total gas flow rate was 140 sccm while the N_2O to Si_2H_6 gas ratio set at 50. The deposition temperature was the only process parameter varied in this experiment. The wafers for the electrical characterization were cleaned as per the standard RCA cleaning process [31], followed by a dip in dilute HF (100:1 by volume ratio of deionized water to 48 % HF).

The RCA cleaning procedure consists of two different steps. In the first step (called standard clean-1 or SC1), wafers are exposed to 5:1:1 solution of deionized water : 30 % H_2O_2 : 30 % NH_4OH at 70°C for 5 min. This procedure is designed to remove organic surface films and to expose the surface to decontamination reactions. In the second step (called SC2), the rinsed wafer is exposed to 6:1:1 solution of deionized water : 30 % H_2O_2 : 37 % HCl at 70°C for 5 min. This procedure is designed to remove metallic contaminants that were not entirely removed by the first treatment.

The wafers were then rinsed in deionized water and blown dry using N_2. Silicon oxide films of 100 nm thickness were deposited at different deposition temperatures within the 30-250°C temperature range. A 300 nm thick aluminum film was then thermally evaporated on the silicon oxide films. Metal-oxide-semiconductor (MOS) capacitors with predefined electrode area were fabricated by wet etching aluminum using standard photolithography techniques. The chemical solution, consisting of 1:1:17:1 by volume of 70 % HNO_3 : CH_3COOH : 85 % H_3PO_4 : deionized water, was used as an aluminum etchant. The typical etch rate for a sputtered aluminum with this solution is about 50 nm/min at room temperature.

The gate electrode areas for the C-V and the I-V measurements were 2.73×10^{-3} cm^2 and 8.3×10^{-3} cm^2, respectively. Post-metallization annealing was done at 400°C in N_2 ambient for 30 minutes. The thickness of the silicon

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oxide films was measured by ellipsometry on an Applied Materials Ellipsometer II and by a Nanometrics 210XP thickness meter. The dielectric constant of the silicon oxide films was calculated from the accumulation capacitance and conductance at high-frequency (1 MHz) C-V measurements with a HP 4275A LCR meter. The ramp I-V characteristics were obtained with a HP 4140 voltage source and a Keithley 485 picoammeter.

Infrared transmission spectroscopic measurements were made on 200-220 nm thick silicon oxide films deposited on substrates that had not undergone any pre-deposition cleaning. The vibrational properties in the 400-4000 cm^{-1} wave number range were observed using a Perkin Elmer Fourier transform infrared spectrophotometer 1600 with a resolution of 4 cm^{-1}. A bare silicon wafer was used as the background reference.

3.3 Results and Discussion

The deposition rate and etch rate of the silicon oxide films as a function of the deposition temperature is shown in Fig. 3.1. The etch rate was obtained by dipping the films in the P-etch solution. The silicon oxide deposition by PECVD using Si_2H_6 and N_2O chemistry is a mass transport limited process [32] especially in the temperature range above 150°C as evident from the nearly temperature independent deposition rate observed in Fig. 3.1. The fastest deposition rate observed in this study is 12.5 nm/min at 220°C. The faster etch rate for the films deposited at lower temperature reflects a increase in the film porosity, probably due to reduced surface diffusion and rearrangement of active species on the substrate surface [33]. This may result in a higher density of hydroxyl (OH)-containing bonds as explained later. The etch rate approaches a constant value of 1.3 nm/sec for films deposited at 150°C and above. This observed etch rate value of 1.3 nm/sec is comparable to the etch rate observed on silicon oxide films deposited by TEOS/ozone CVD at 400°C [34].

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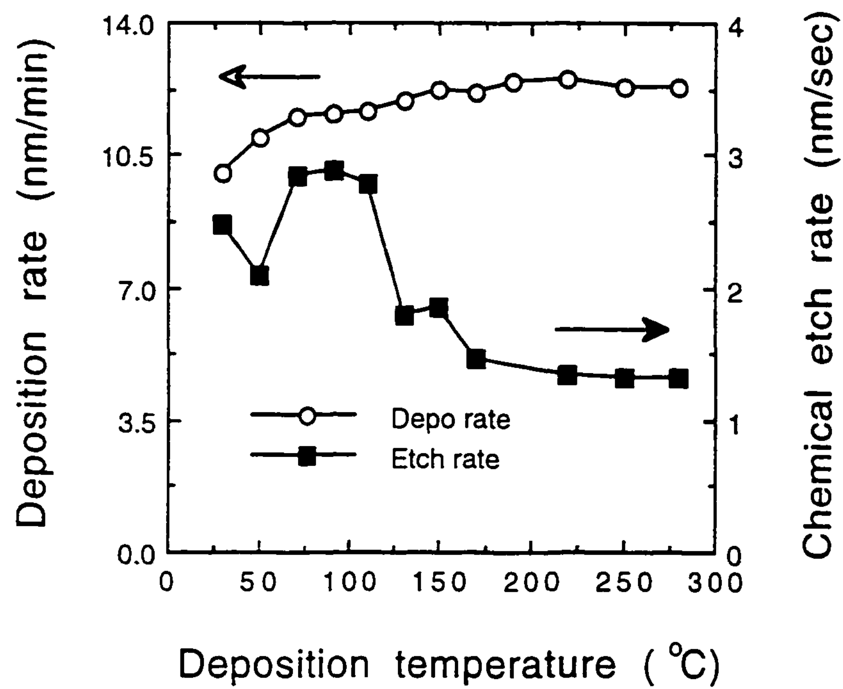

Fig. 3.1. Deposition rate and etch rate of the silicon oxide films as a function of deposition temperature. The P-etch solution consists of 15 parts by volume of 48 % HF, 10 parts by volume 70 % HNO_3, and 300 parts by volume of deionized water.`

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Figure 3.2 shows the infrared transmission spectra of the silicon oxide films deposited at various deposition temperatures from 30°C to 250°C. A decrease in the transmission intensity of the hydroxyl-containing bonds located at 3380-3620 cm^{-1} and at 940 cm^{-1} is observed with an increase in the deposition temperature [5]. This gradual disappearance of the hydroxyl-containing peaks with increasing deposition temperature is consistent with the improvement in the film integrity reflected by a decrease in the etch rate in Fig. 3.1.

In the silicon oxide, the basic structural unit is the SiO_4 tetrahedron with a silicon atom at the center, bonded to four oxygen atoms placed at the corners as shown in Fig. 3.3. Each oxygen atom belongs to two tetrahedra and is thus bonded to two silicon atoms. The vibrational mode associated with the Si-O-Si stretching is frequently used to study the structural property of the silicon oxide films. The infrared transmission spectra for stoichiometric silicon oxide film exhibits three characteristic peaks [35] which occur approximately at 450, 800, and 1075 cm^{-1}. The lowest frequency vibration near 450 cm^{-1} is a Si-O-Si rocking mode in which the oxygen atom motion is out of the plane of the Si-O-Si bond. The intermediate frequency and the weakest transmission at about 800 cm^{-1} is a Si-O-Si bending vibration mode in which the oxygen atom motion is in the plane of the Si-O-Si bond and along the direction of the bisector of Si-O-Si bridging bond angle. The strongest transmission near 1075 cm^{-1} is a stretching vibration in which the oxygen atom motion is in the plane of the Si-O-Si bond and in a direction parallel to a line joining the two silicon atoms.

The Si-O-Si stretching peak and its full width at half maximum (FWHM) as a function of the deposition temperature is shown in Fig. 3.4. As the deposition temperatures increase, the wave number corresponding to the Si-O-Si stretching decreases from 1073 cm^{-1} to 1054 cm^{-1} while the FWHM increases

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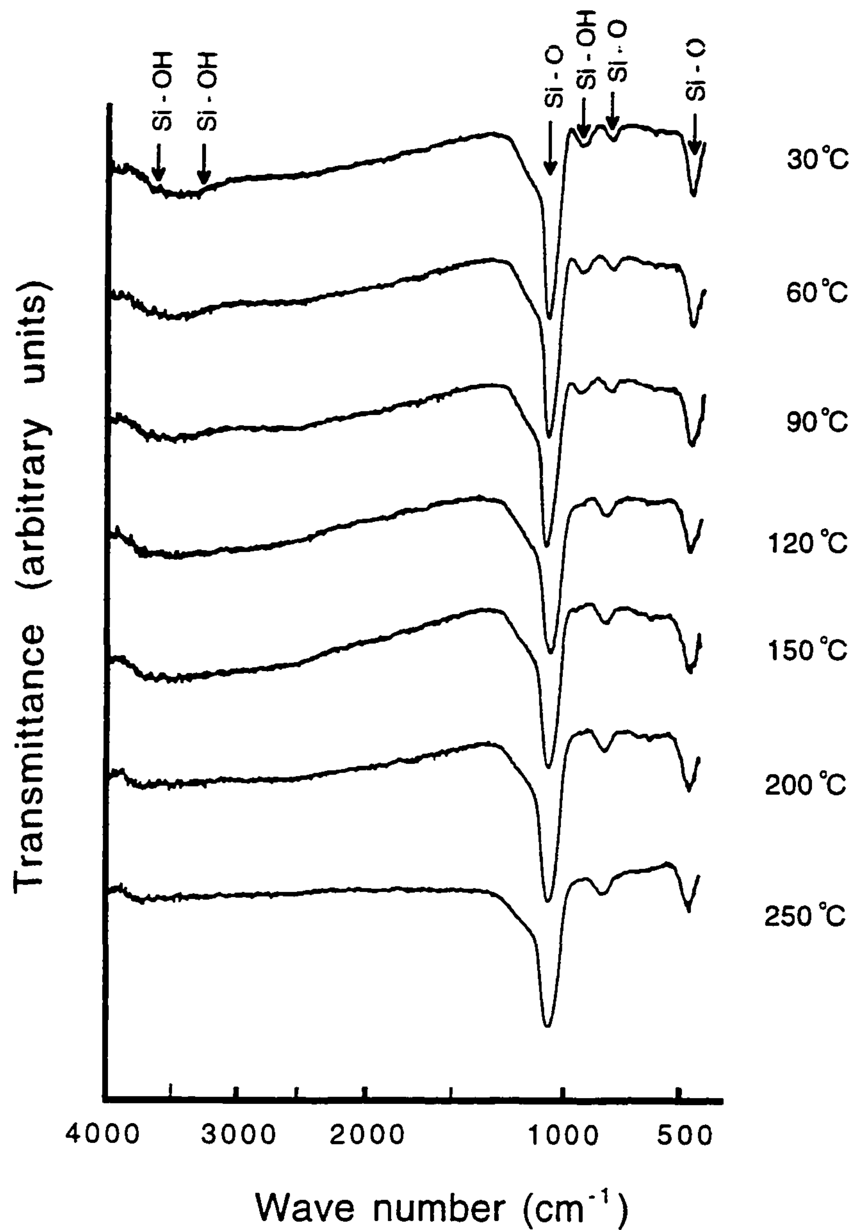

Fig. 3.2. Infrared transmission spectra of the as-deposited silicon oxide films as a function of deposition temperature in the range of 30-250°C. The arrows indicate the location of absorption peaks in the vibrational spectra.

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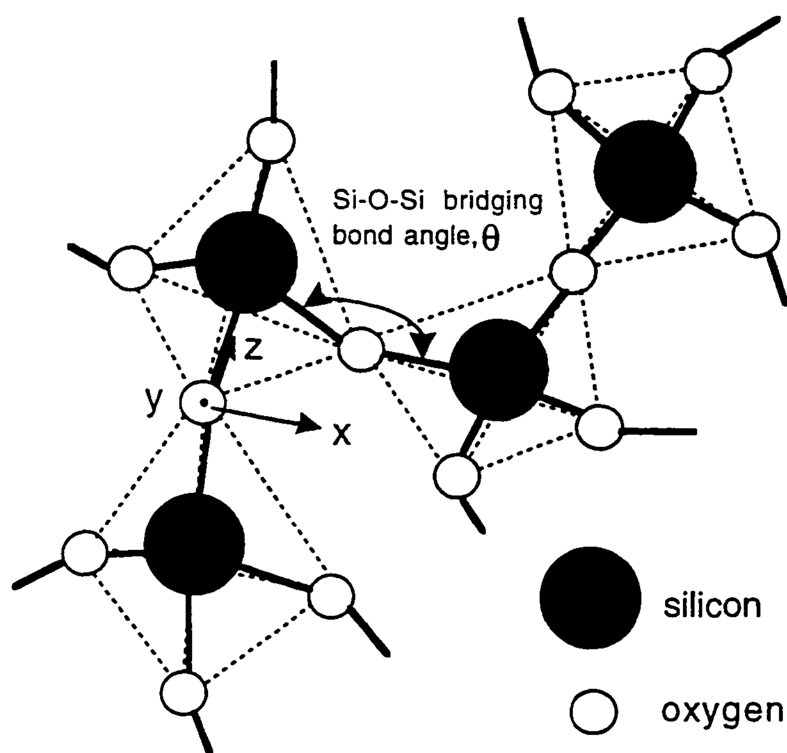

x : Si-O-Si rocking vibration

y : Si-O-Si stretching vibration

z : Si-O-Si bending vibration

Fig. 3.3. Three-dimensional representation of two neighboring SiO_4 cell, bridged by an oxygen atom. Directions for three characteristic vibration motions are also marked.

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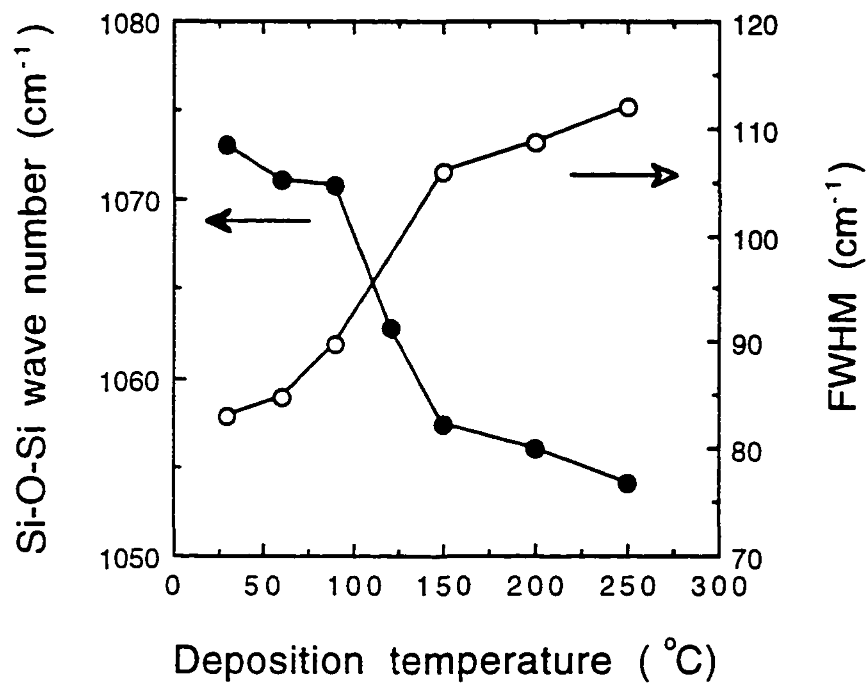

Fig. 3.4. Si-O-Si stretching absorption peak and FWHM of the as-deposited silicon oxide films shown in Fig. 3.2 as a function of film deposition temperature.

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from 83 cm^{-1} to 112 cm^{-1}. It is now well accepted [1], [11], [36], [37] that shifts in the stretching wave number toward lower values and increases in the FWHM are related to smaller values of the average Si-O-Si bridging bond angle which is believed to be about 144° for thermally grown silicon oxide and somewhat smaller than 144° for PECVD films [38]. As the Si-Si distance is directly related to the Si-O-Si bond angle, changes in wave number with compaction can be explained in terms of changes in the bond angle. By assuming that the density of silicon oxide scales inversely as the cube of the Si-Si distance, a decrease in the Si-O-Si bond angle results in an increase in the film density. From Fig. 3.2, the hydroxyl content decreases with increasing deposition temperature. An increase in the Si-OH content is known to result in more porous silicon oxide CVD films [3], causing faster etch rate for the silicon oxide films deposited at lower deposition temperatures.

The infrared transmission spectra as a function of the deposition temperature after conventional furnace anneal at 400°C in N_2 ambient for 30 min is shown in Fig. 3.5. For the annealed case, the hydroxyl-containing peak located at 940 cm^{-1} has nearly disappeared even for the silicon oxide deposited at 30°C.

Figure 3.6 indicates the relative dielectric constant of the as-deposited and annealed silicon oxide films as a function of the deposition temperature. The dielectric constant is calculated from the observed values of the capacitance in accumulation of MOS devices fabricated with the deposited films. The observed capacitance was corrected for series resistance [39], as described in Appendix A. The dielectric constant has been reported to be proportional to the hydroxyl-containing species in the films. The increase in the dielectric constant due to H_2O and OH content can be explained by the fact [3] that these are dipolar species with relatively large dipole moments μ_{H_2O}=1.84

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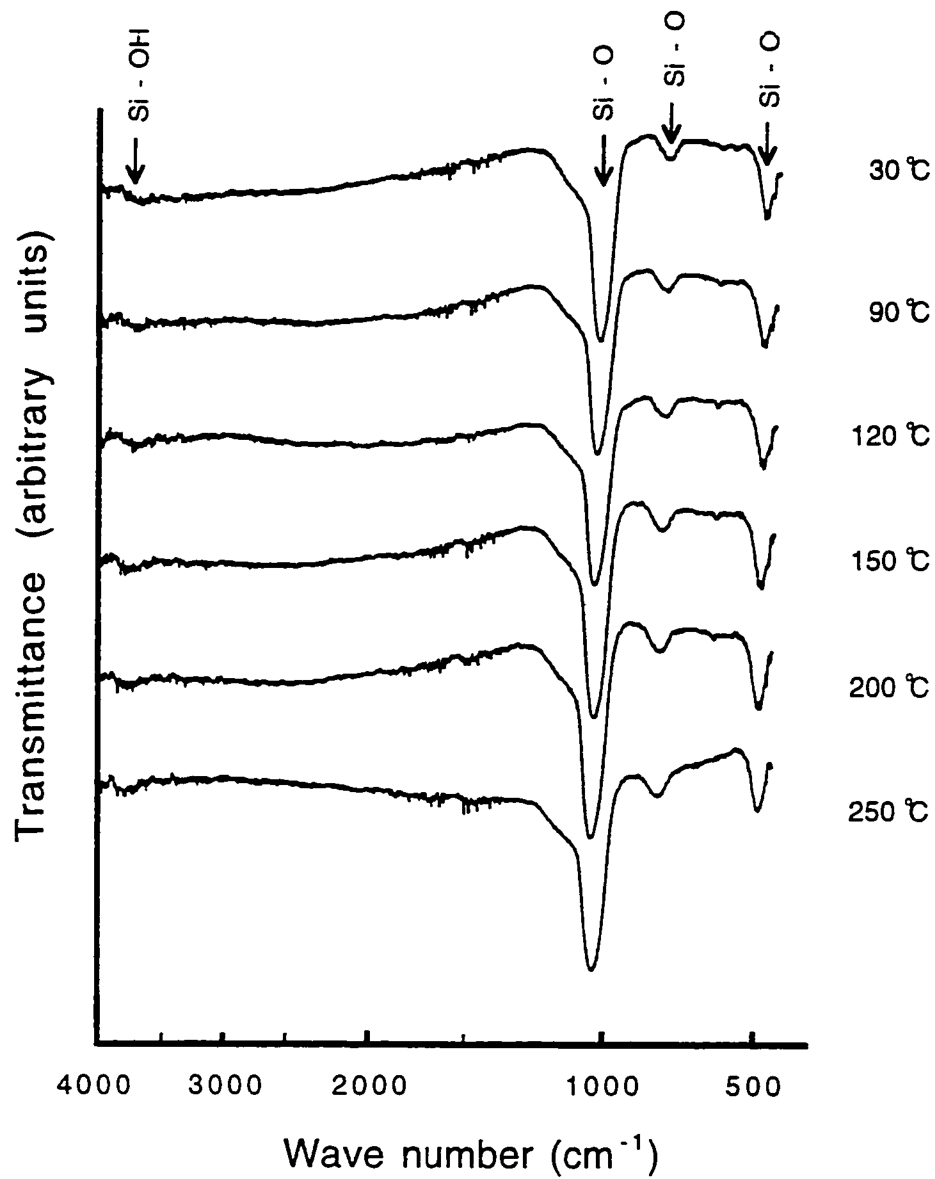

Fig. 3.5. Infrared transmission spectra of the annealed silicon oxide films as a function of film deposition temperature. The annealing is carried out at 400°C in N_2 ambient for 30 min.

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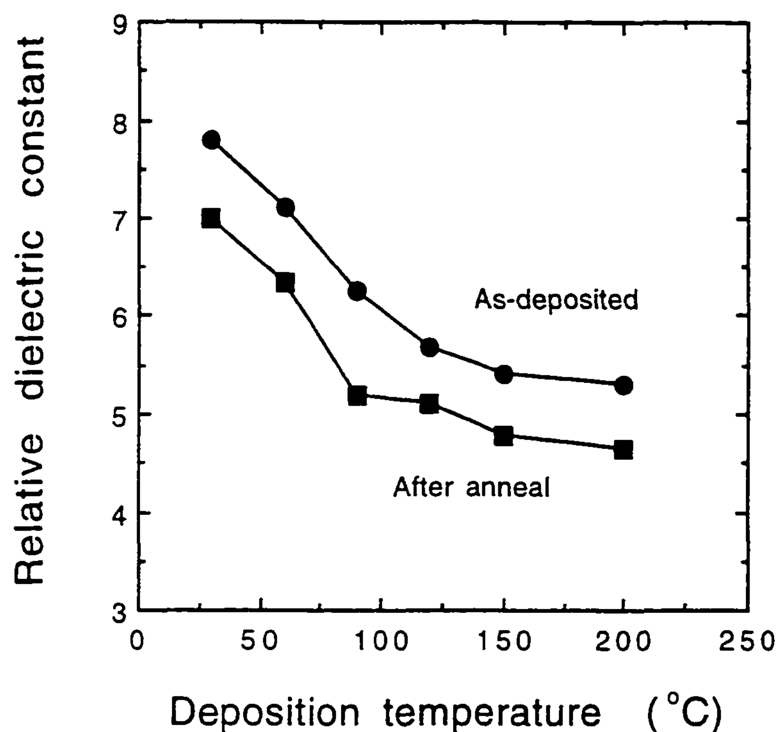

Fig. 3.6. Dielectric constant of the as-deposited and the annealed silicon oxide films as a function of film deposition temperature. Anneal is carried out at 400°C in N_2 ambient for 30 min. The thickness of the silicon oxide film is about 100 nm and the gate area is 2.7×10^{-3} cm^2.

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debye and μ_{OH}=1.5 debye (1 debye=3.338 × 10^{-30} C·m), respectively, with the relative dielectric constant of 78.2 for liquid water being large. Hence, the silicon oxide films deposited at lower temperatures with higher Si-OH content result in higher values for the relative dielectric constant. The dielectric constant of the as-deposited silicon oxide films decreases from 7.8 to 5.2 as the deposition temperature increases from 30°C to 200°C. Similarly, the dielectric constant of the annealed silicon oxide films decreases from 7 to 4.6. Assuming that the anneal temperature at 400°C is low enough not to change the thickness of the silicon oxide films, the decreased values of the dielectric constant indicate that even though the annealing is carried out after the gate electrode fabrication, it is able to partially reduce the hydroxyl-related bonds. The smallest value that of 4.6 for the relative dielectric constant obtained in this study, is still higher than the corresponding value of 3.9 for the thermally grown silicon oxide. The N_2 ambient gas during annealing is chemically stable at the 400°C annealing temperature used and can not result in significant nitridation [40].

Time zero dielectric breakdown characteristics of the silicon oxide films deposited at different deposition temperatures are shown in Fig. 3.7. The details of the ramp I-V characteristic are basically described as follows [7]. As a current flows through the silicon oxide, some electrons are captured into deep bulk traps, creating a space charge. At a suitably high current, the charge build-up is enough to significantly affect the electric field at the injecting interface which opposes the ramp voltage and on a logarithmic plot a trapping ledge is observed. If all of the traps are filled, or if a dynamic equilibrium is achieved between trapping and high field detrapping, then the curve may go through the ledge onto a new Fowler-Nordheim characteristic before breakdown. The ramp I-V measurements, here, are taken at 25°C with the voltage ramp rate set at 1 V/sec. The polarity of the field causes carrier accumulation at the substrate

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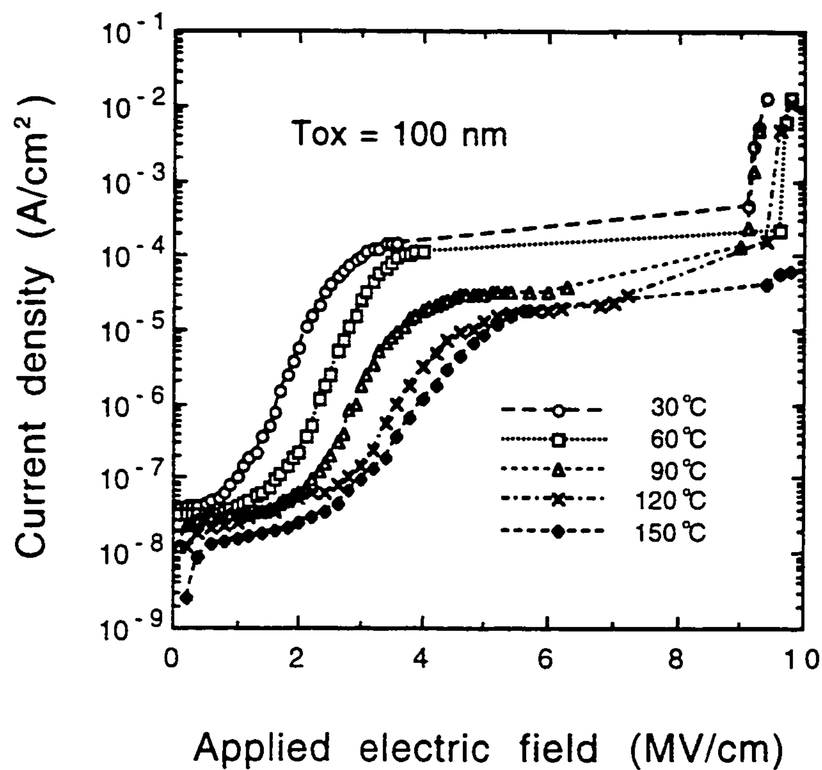

Fig. 3.7. J-E characteristics of the silicon oxide films for various deposition temperatures in the range of 30-150°C. The voltage ramp rate is fixed at 1 V/sec. The bias polarity corresponds to electron injection from the gate. The oxide thickness is 100 nm and the gate area is 8.3×10^{-3} cm^2.

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surface. This for p-type substrate used in this study corresponds to electron injection from the aluminum gate. Current density, J, in the silicon oxide film as a function of the applied electric field, E, indicates higher leakage currents for the films deposited at lower temperatures. However, the leakage current density of 5×10^{-8} A/cm^2 at 0.5 MV/cm field strength for the silicon oxide film deposited at the lowest temperature of 30°C is of the same order as through the silicon oxide film deposited by PECVD using SiH_4 as the silicon source at 350°C [7]. The J-E characteristics in Fig. 3.7 have similar features for all the deposition temperatures considered. The current through the silicon oxide film saturates at high electric field, known as the trapping ledge [41], [42]. The trapping ledge seems to be caused by the hydroxyl-containing bonds which either act as deep traps or recombination centers in the silicon oxide films [2]. Further experiments are required for a better understanding of the parameters related to the trapping ledge. At about 10 MV/cm, the intrinsic dielectric breakdown of the silicon oxide films is observed. For the film deposition at 150°C, the dielectric breakdown field is greater than 10 MV/cm.

In Fig. 3.8, J/E^2 is plotted against 1/E. The slope corresponds to the barrier height [43] as shown in Fig. 3.9. The slope of the linear part of this curve is observed to increase with increasing deposition temperature. From this, the barrier height values of 3.1 eV and greater obtained for the oxide films deposited at 120°C and above are close to the reported value of 3.2 eV. For the silicon oxide films deposited at 30°C, the observed barrier height of 1.59 eV is half that of the reported value, indicating existence of a large number of traps or energy states in the film.

A distribution of the non-destructive dielectric breakdown field of the silicon oxide films deposited at various deposition temperatures is shown in Fig. 3.10. In the measurements, a non-destructive breakdown field is defined as the

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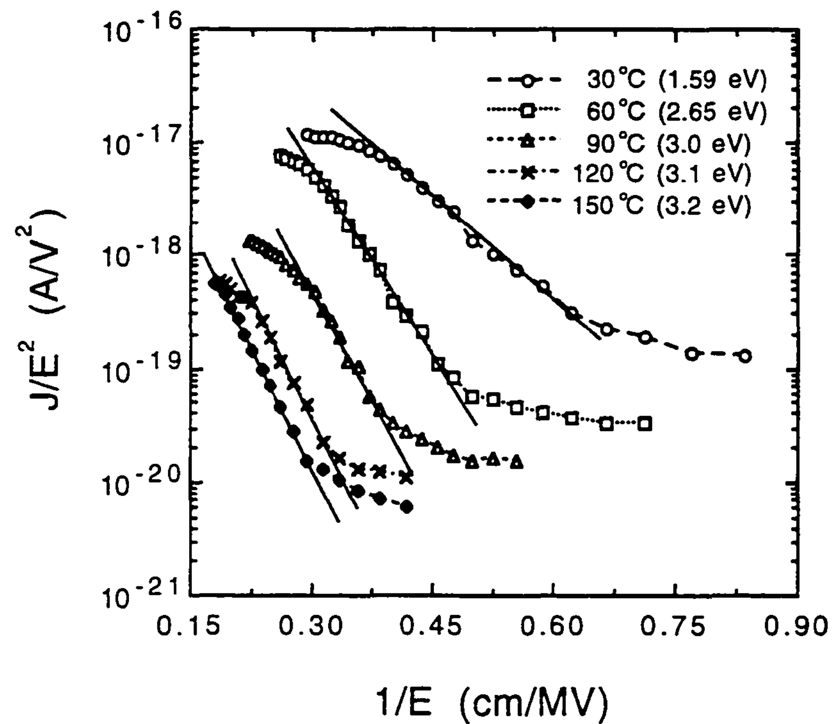

Fig. 3.8. Fowler-Nordheim current plots of the silicon oxide films shown in Fig. 3.7. The linear dependence of J/E^2 against 1/E gives the barrier height indicated in the parentheses .

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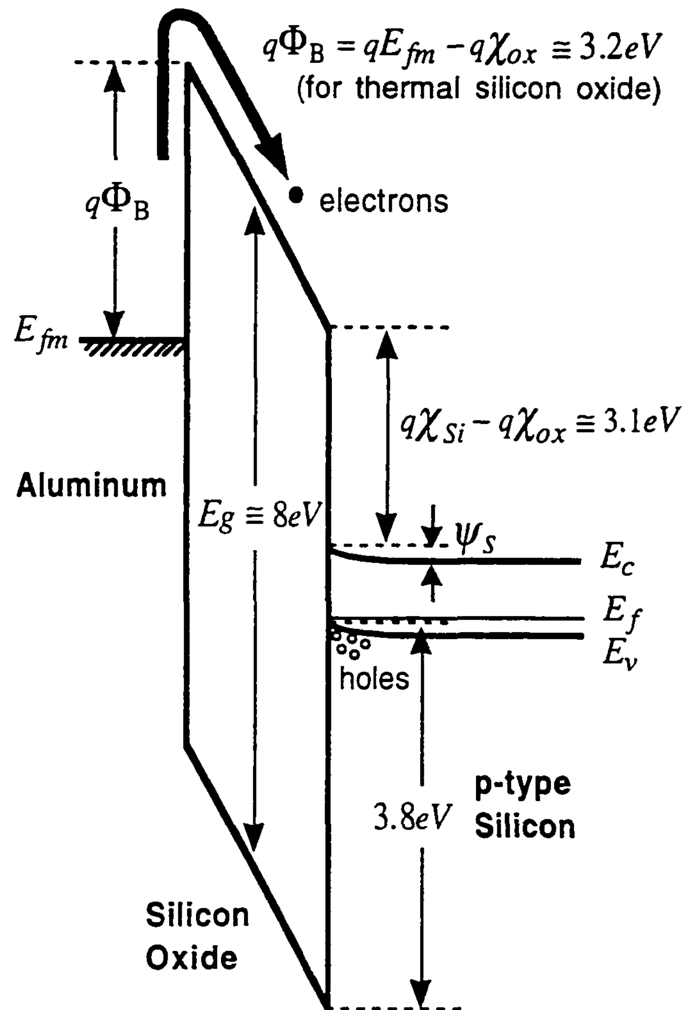

Fig. 3.9. Energy-band diagram of a MOS system with p-type silicon biased into accumulation. The barrier height is marked.

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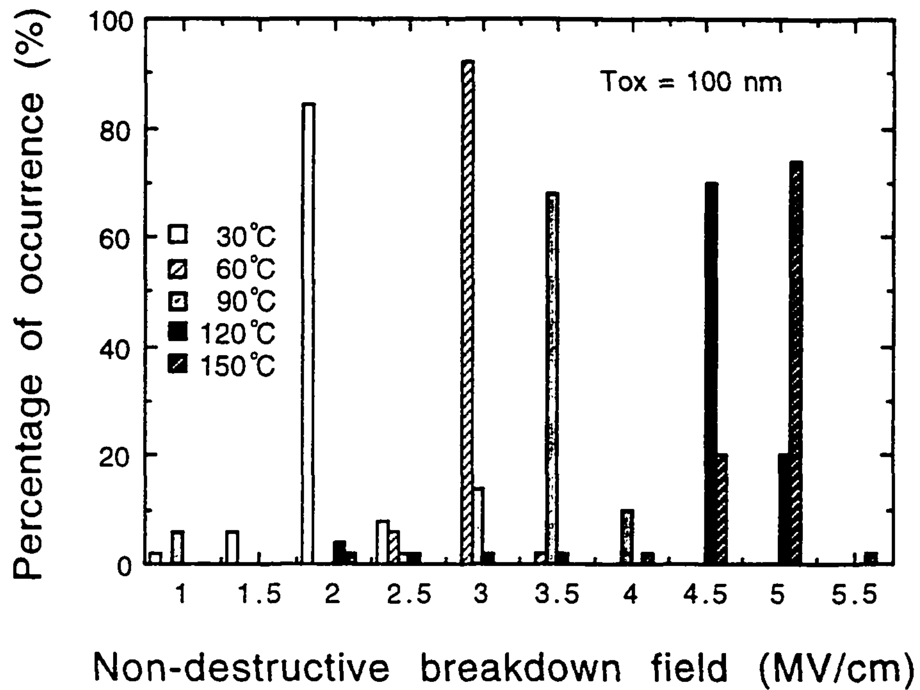

Fig. 3.10. Distribution of the non-destructive dielectric breakdown occurrence as a function of electric field for the silicon oxide films deposited at different temperatures. Fifty devices are measured for each case. The voltage ramp rate is fixed at 1 V/sec and the gate polarity is negative with respect to the substrate.

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electric field at which the current level reaches 83 nA which is equivalent to a current density of 10 $\mu A/cm^2$. Fifty devices for each case were measured at room temperature and voltage was increased at a ramp rate of 1 V/sec biasing the device towards accumulation. No initial device failures such as the ones caused by pin-holes in the films were observed. Figure 3.10 shows a very consistent distribution with the peaks occurring at higher values of applied field as the film deposition temperature is increased. The average value of non-destructive breakdown field, summarized in Table 3.1, of the silicon oxide films deposited at 30°C was 2.1 MV/cm. However, it increased to 3.4 MV/cm for the films deposited at 90°C, to 4.5 MV/cm for the films deposited at 120°C, and to 4.8 MV/cm for the films deposited at 150°C.

3.4 Conclusion

The characteristics of the silicon oxide films prepared by plasma enhanced chemical vapor deposition using Si_2H_6 and N_2O as a function of the deposition temperature in the range of 30-250°C were examined. For deposition temperature above 150°C, the deposition rate and the P-etch rate were observed to be relatively independent of temperature. The film deposition rate increased slightly and the P-etch rate decreased with deposition temperature in the range of 30-150°C. Film density and the dielectric constant improved with deposition temperature. Infrared transmission spectra indicated a decrease in hydroxyl-containing peaks in the silicon oxide films located at 940 cm^{-1} and at 3380-3630 cm^{-1} with increasing deposition temperature. A post-metallization anneal at 400°C for 30 min in N_2 showed further improvement in the dielectric property of the deposited films.

The leakage current density through the silicon oxide film decreased with deposition temperature. The leakage current density of 5×10^{-8} A/cm^2 for devices biased towards accumulation for the field strength of 0.5 MV/cm

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Table 3.1. Average non-destructive dielectric breakdown field strength for the silicon oxide films deposited at different temperatures.

Film deposition temperature (°C)	Non-destructive dielectric breakdown field (MV/cm)
30	2.1
60	3.4
120	4.5
150	4.8

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through silicon oxide film deposited at 30°C is comparable to the current through oxide films deposited at 350°C with conventional SiH_4 precursor. The Fowler-Nordheim plots indicate a barrier height of 3.0 eV for oxide films deposited at 90°C and above. The lower values of the effective barrier height were obtained in the silicon oxide films deposited at lower temperatures, probably due to incorporation of a larger number of traps. The average value of non-destructive dielectric breakdown field increased from 2.1 MV/cm for 30°C deposited samples to 4.8 MV/cm for the 150°C deposited samples.

The Si_2H_6 precursor provides superior PECVD silicon oxide films at lower temperatures than the traditionally used precursor SiH_4. The etch rate of film deposited with Si_2H_6 is comparable to that obtained by TEOS/ozone CVD at a higher temperature of 400°C. This process, hence, shows promise for depositing dielectric layers for microelectronics processes that require low temperatures.

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CHAPTER 4

STRUCTURAL PROPERTIES OF SILICON OXIDE FILMS

4.1 Introduction

The many results presented in this chapter have been published in Applied Physics Letters, volume 67, pages 2986-2988, 1995. Their permission was gratefully acknowledged.

It is generally accepted [44] that the short range order in the amorphous silicon oxide films on a microscopic scale is composed of ring networks of tetrahedra which link in such a way as to produce a distribution of intertetrahedral Si-O-Si bond angles whose mean is about 144°. This angle corresponds to that at which calculation predicts the bond energy per silicon oxide molecule to be a minimum. One of the interesting physical properties of the amorphous silicon oxide films is the plastic densification produced by either large hydrostatic pressure (> 8 GPa at room temperature) or a combination of high pressure and temperature. These densifications may be relaxed only by heating to very high temperature (> 900°C). The densified, amorphous silicon oxide films may also be grown thermally on silicon substrates by low temperature processing or deposited by CVD.

In this chapter, the dependence of the structural properties of the silicon oxide films prepared by PECVD using Si_2H_6 and N_2O at 120°C on the post-deposition annealing process is presented. The film characteristics in terms of bond stretching motion and relative dielectric constant are discussed in detail.

4.2 Experiment

Chemically polished, 4" diameter boron doped silicon wafers with (100) orientation and 5-15 Ω·cm resistivity were used as the substrates. The deposition process parameters were maintained the same throughout this

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study. The deposition temperature was set at 120°C while the top electrode temperature was 60°C. A 140 sccm gas mixture of 4.8 % Si_2H_6 in He and pure N_2O was introduced into the process chamber to deposit 100 nm thick silicon oxide films while the gas flow ratio of N_2O to Si_2H_6 was fixed at 50 in order to ensure the stoichiometry of the silicon oxide films. The process pressure and rf power were 700 mTorr and 50 W, respectively. These conditions gave a deposition rate of 12.5 nm/min and thickness uniformity of within ± 3 % across four inch wafers. The conventional RCA cleaning followed by a dip in 100:1 parts by volume of deionized water-HF (48 %) was used as pre-deposition cleaning procedure.

The thickness of the deposited silicon oxide films was measured using an Applied Materials Ellipsometer II. The post-deposition annealing processes were carried out in conventional tube furnace flowing N_2 at different temperatures for 30 min. The vibrational properties in the 400-4000 cm^{-1} wave number range were observed using a Perkin Elmer Model 1600 Fourier transform infrared spectrophotometer with a resolution of 4 cm^{-1}. A bare silicon wafer was used for background subtraction purposes.

Aluminum gate MOS capacitors with predefined area of 2.6×10^{-3} cm^2 were fabricated using a standard photolithography technique to investigate the dielectric constant of the silicon oxide films annealed at different temperatures. Forming gas anneal with 5 % H_2 in N_2 ambient at 400°C for 30 min was carried out as the post-metallization anneal (PMA) prior to C-V measurements.

4.3 Results and Discussion

In Fig. 4.1, the chemical etch rate in the P-etch solution is plotted as a function of the post-deposition annealing temperature. The chemical etch rate was obtained by dipping the films in the P-etch solution. The etch rate of the as-deposited silicon oxide films was found to be 0.81 nm/sec. As the annealing

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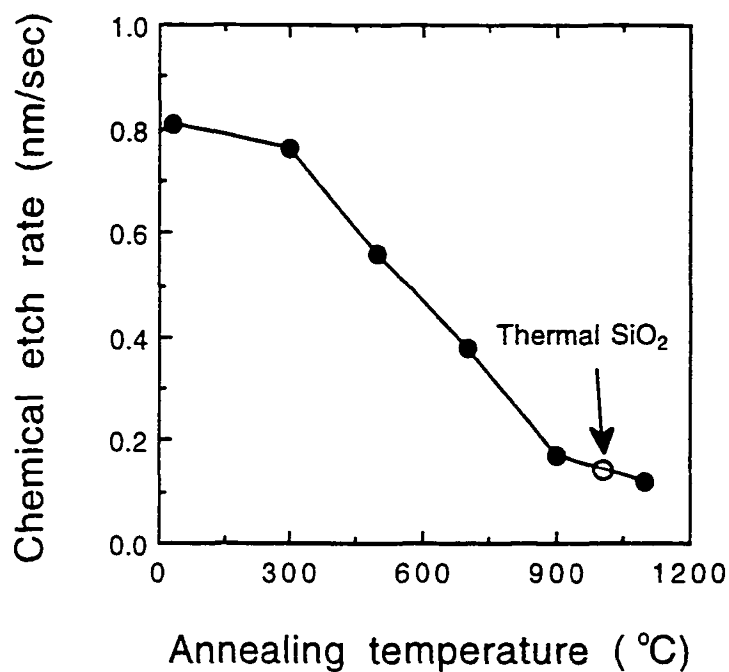

Fig. 4.1. Chemical etch rate in the P-etch solution of the silicon oxide films as a function of post-deposition annealing temperature. Experimental data at 25°C are for the as-deposited film. The circle corresponds to etch rate of the thermal silicon oxide films grown at 1000°C, 0.15 nm/sec.

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temperature increases, the etch rate decreases. The etch rate ratio of the as-deposited to the annealed silicon oxide films at 1100°C was 7.4. Higher etch rates obtained indicate that the as-deposited silicon oxide films may have strained bonds, micropores, and impurities in the network. The stress induced cracking which is known to occur during high temperature processing, particularly in films prepared at low temperatures, has not been observed even at 1100°C.

Infrared transmission spectra of the silicon oxide films annealed at different temperatures are shown in Fig. 4.2. Three characteristic peaks located at 1075 cm^{-1}, 800 cm^{-1}, and 450 cm^{-1} corresponding to Si-O-Si asymmetric stretching, bending, and rocking motion, respectively, are evident [34], [45], [46]. Also from the figure, transmission intensities of the hydrogen containing bonds [47] such as Si-H (2270 cm^{-1}, 880 cm^{-1}), Si-OH (3620 cm^{-1}), H_2O (1620 cm^{-1}) are below the spectrophotometer's detection level. It is claimed [48] that the detection limit for a 100 nm film is five times higher than the 0.5-1 at.% limit estimated for 500 nm films [10]. This indicates less than 5 at.% of bonded hydrogen content in the films studied.

The Si-O-Si stretching vibration mode is commonly used to study the structural property of the silicon oxide films. The Si-O-Si stretching peak wave number and its relative peak intensity as a function of the annealing temperature are plotted in Fig. 4.3. As the annealing temperature increases, the stretching peak wave number increases: for example, from 1056 cm^{-1} for as-deposited silicon oxide films to 1077 cm^{-1} for silicon oxide films annealed at 1100°C. Also, the relative intensity of the stretching peak increases with annealing temperature and is up to 2.5 times higher for films annealed at 1100°C compared with as-deposited films.

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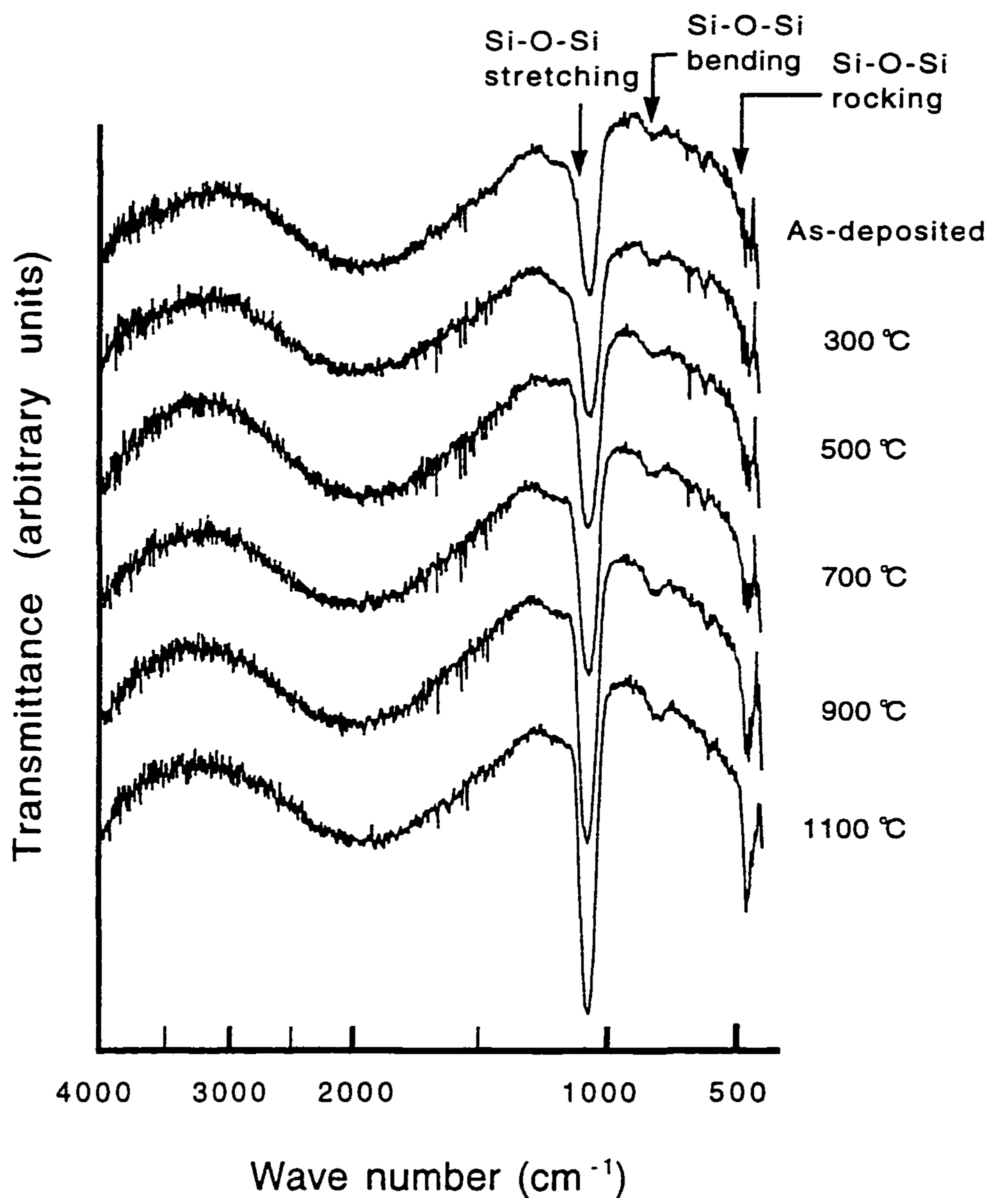

Fig. 4.2. Infrared transmission spectra of the silicon oxide films annealed at different temperatures. Three characteristic peaks of Si-O-Si vibrational motion are marked.

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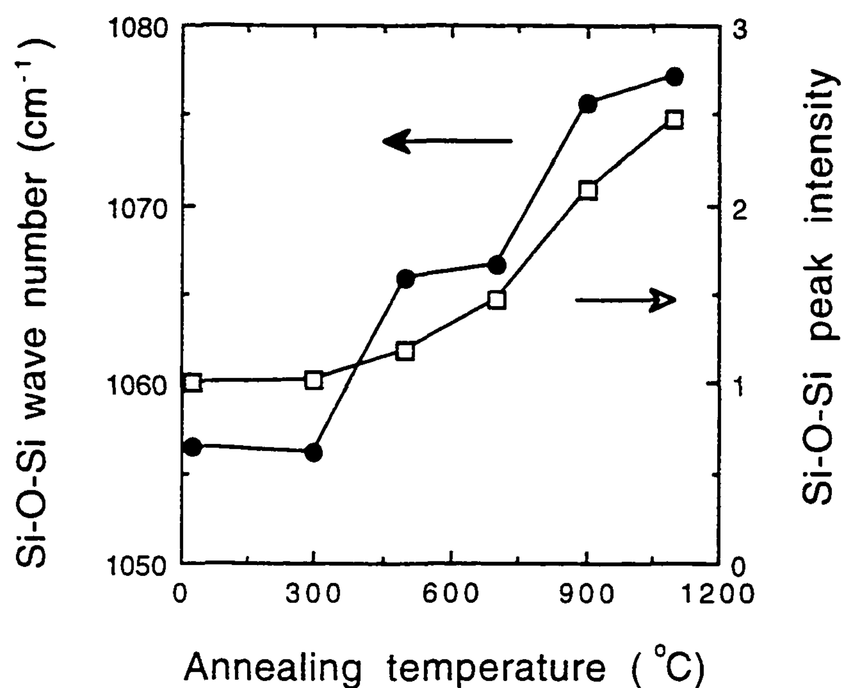

Fig. 4.3. Si-O-Si asymmetric stretching peak wave number and its relative peak intensity with respect to the as-deposited silicon oxide films as a function of post-deposition annealing temperature.

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Previous studies [36], [49] had reported that the position of the stretching peak wave number (ω) is related to the film density (ρ),

$$\frac{d\omega}{d\rho} = -93 g^{-1} cm^{2}, \tag{4.3.1}$$

and to the mean Si-O-Si bridging bond angle (θ),

$$\frac{d\theta}{d\rho} = -28^{o} g^{-1} cm^{3}. \tag{4.3.2}$$

The changes in the film density ($\Delta\rho/\rho$) and θ calculated using these relationships are plotted in Fig. 4.4. The Si-O-Si stretching peak wave number of 100 nm thick thermal silicon oxide films grown at 1000°C in our laboratory is located at 1076 cm^{-1} and is used as the reference wave number for the undensified silicon oxide films. Assuming [36], [50] that ρ and θ of the undensified amorphous silicon oxide films are 2.2 g/cm^3 and 144°, the film density and Si-O-Si bridging bond angle of the as-deposited silicon oxide films are calculated to be 2.4 g/cm^3 and 138°, as summarized in Table 4.1. This results in 9.4 % densification of the as-deposited silicon oxide films compared to the undensified silicon oxide films. It is believed that the high temperature annealing favors the relaxation of the silicon oxide film network [51], presumably by reduction of porosity and hydrogen-containing species.

The effect of high temperature annealing in terms of change in dielectric constant was also investigated using C-V measurement and is shown in Fig. 4.5. The dielectric constant is calculated from the measured values of the capacitance in the accumulation region of MOS devices with silicon oxide films,

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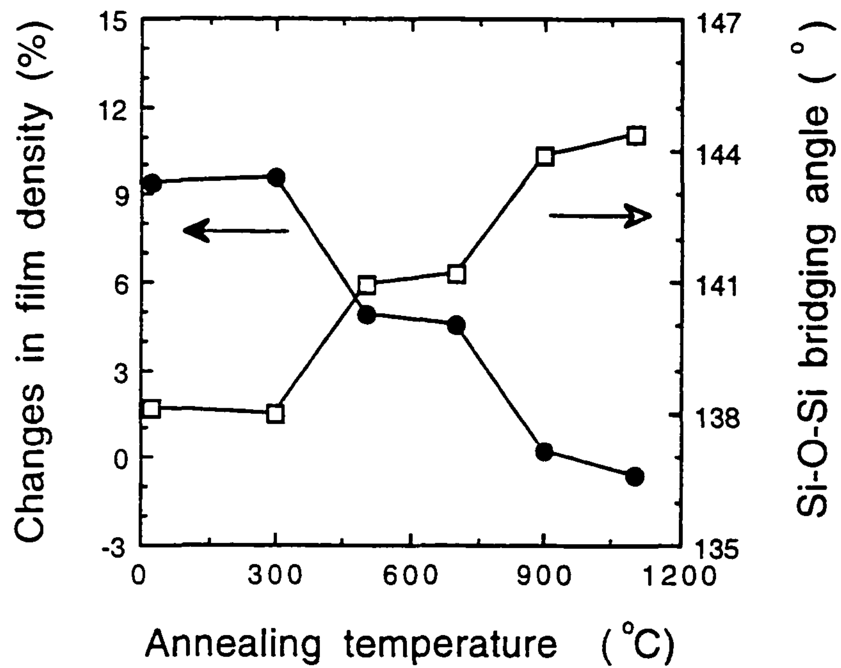

Fig. 4.4. Changes in the silicon oxide film density, $\Delta\rho/\rho$, and Si-O-Si bridging bond angle, θ as a function of post-deposition annealing temperature. It is assumed that ρ and θ of the undensified amorphous silicon oxide films are 2.2 g/cm^3 and 144°, respectively.

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Table 4.1. Summary of structural properties of the silicon oxide films.

Film property	As-deposited film	Annealed film at 1100°C	Thermal SiO_2 at 1000°C
Si-O-Si stretching wave number (cm^{-1})	1056	1077	1076
Film density (g/cm^3)	2.4	~2.2	2.2
Si-O-Si bridging bond angle (°)	138	~144	144

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annealed at different temperatures prior to aluminum evaporation. Increase in annealing temperature caused the reduction of dielectric constant of the silicon oxide films. For instance, the dielectric constant of the as-deposited silicon oxide films was 5.88 whereas that of the silicon oxide films annealed at 1100°C was 4.16. Dielectric constant has been known to be proportional to the hydroxyl content in the film [3], thereby suggesting the presence of reduced number of the hydroxyl-containing bonds in the silicon oxide films annealed at higher temperature. It was also found that the PMA resulted in further reduction of the dielectric constant. This may be due to hydrogen related passivation [52] known to occur during forming gas anneal. More detailed study is in progress to understand the bearing of these results on the electrical properties of the silicon oxide films.

4.4 Conclusion

The results reported in this chapter indicate that the structural properties of the PECVD silicon oxide films deposited at 120°C using Si_2H_6 and N_2O are not significantly different from the conventional SiH_4-based silicon oxide films deposited at 250-350°C. The etch rate of the as-deposited silicon oxide films was found to be 0.81 nm/sec. The etch rate ratio of the as-deposited to the annealed silicon oxide films at 1100°C was 7.4. Infrared transmission measurements indicated less than 5 at.% of bonded hydrogen content in the silicon oxide films studied. The shift of Si-O-Si stretching peak wave number of the as-deposited films compared to the undensified films was attributed to 9.4% increase in the film density, resulting in smaller Si-O-Si bridging bond angle of 138°. It was also believed that the high temperature annealing resulted in the reduction of hydroxyl containing species in the film and, in turn, drove the dielectric constant towards that of thermal silicon oxide films.

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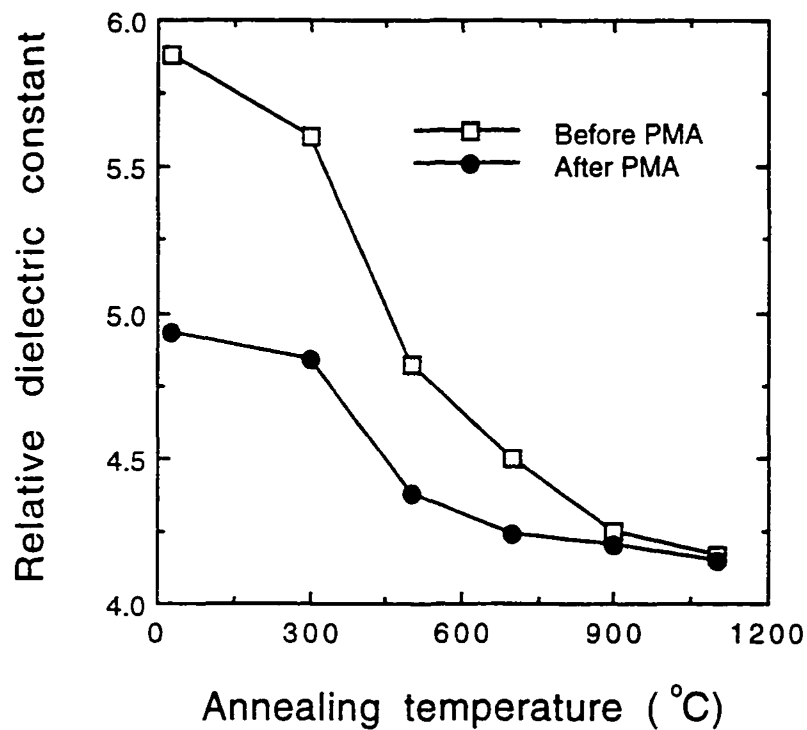

Fig. 4.5. Dependence of dielectric constant of the silicon oxide films annealed at different temperatures on post-metallization annealing. The post-metallization annealing was carried out in 5 % H_2 in N_2 ambient at 400°C for 30 min.

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CHAPTER 5
EFFECT OF NATIVE OXIDE REMOVAL ON FILM QUALITY

5.1 Introduction

The many results presented in this chapter have been published in Journal of Vacuum Science & Technology B, volume 14, pages 727-731, 1996. Their permission was gratefully acknowledged.

In this chapter, the electrical properties of the silicon oxide films deposited at 120°C using Si_2H_6 and N_2O derived from C-V and I-V measurements are presented. The effect of native oxide removal on the substrate surface prior to the film deposition is examined. Also, the effect of annealing the as-deposited films either in N_2 (post-deposition annealing) or in forming gas ambient after the formation of aluminum electrode (post-metallization annealing) is discussed.

5.2 Experiment

Boron doped (100) oriented silicon wafers, 4 inch in diameter and 10 Ω·cm resistivity were used as the substrate material. The deposition temperature was maintained at 120°C with the top electrode temperature at 60°C. A gas mixture containing 40 sccm of 4.8 % Si_2H_6 in He and 100 sccm of pure N_2O which resulted in the gas flow ratio of N_2O to Si_2H_6 of 50 was introduced into the process chamber to deposit 100 nm thick silicon oxide films . The deposition pressure and rf power were 700 mTorr and 50 W, respectively. Under these conditions, film deposition rate of about 13 nm/min was obtained.

The post-deposition annealing was performed in a tube furnace in N_2 ambient for 30 min at different temperatures, followed by thermal evaporation of 250 nm thick aluminum on the silicon oxide films. MOS capacitors were fabricated using standard photolithography techniques with a predefined gate

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area of 2.7×10^{-3} cm^2 and then subjected to the post-metallization annealing in 5 % H_2 in N_2 ambient at 400°C for 30 min. The thicknesses of the deposited silicon oxide films were measured using an Applied Materials ellipsometer model II. The C-V measurements were carried out by superimposing a 25 mV ac signal at 1 MHz with a HP 4275A LCR meter. A dc voltage sweep rate of 1 V/sec was used. The capacitance values observed were corrected for the presence of series resistance, based on the procedures in Appendix A. The I-V characteristics were obtained with a HP 4140 voltage source and a Keithley 485 picoammeter.

5.3 Results and Discussion

5.3.1 Effect of Native Oxide on C-V Curves

The substrate wafers used in this work were cleaned as per the standard RCA cleaning procedure. They were then either loaded directly into the deposition chamber after this cleaning procedure or were subjected to an additional immersion in a dilute HF solution (100:1 by volume of deionized water : 48 % HF) before loading into the deposition chamber. The samples immersed in the dilute HF in the latter case were rinsed with deionized water and blown dry with a N_2 jet.

The C-V curves for the devices on the as-deposited silicon oxide films processed under identical conditions except for the pre-deposition dip in the dilute HF are shown in Fig. 5.1. Neither post-deposition nor post-metallization annealing was performed before these measurements. There are four different types of charges associated with the silicon oxide-silicon system [53]. The overall effect of these charges is to shift the actual C-V curve with respect to the reference curve for a device having no charges. For our case, the work function difference (Φ_{MS}) between the gate material and the substrate is -0.83 V for the substrate doping used. The devices on the films cleaned with the RCA

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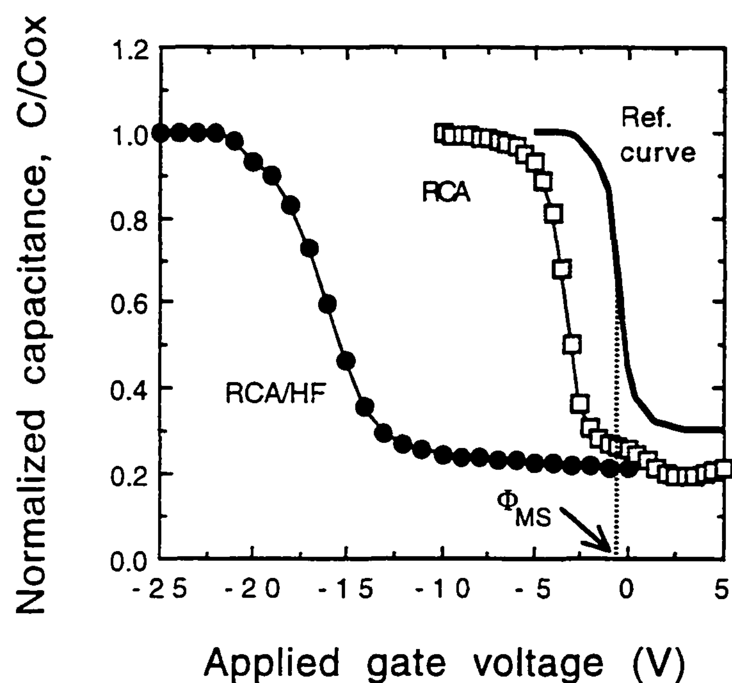

Fig. 5.1. High frequency normalized capacitance as a function of applied gate voltage for two different pre-deposition cleaning procedures which are RCA and RCA followed by a dip in a dilute HF. The reference curve marked is drawn for Φ_{MS}= -0.83 V and with no oxide or interface charges. Neither post-deposition nor post-metallization annealing was performed on these samples.

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procedure showed the flat band voltage (V_{FB}) of -3.66 V, corresponding to the flat band voltage shift (ΔV_{FB}) of -2.83 V with respect to the reference curve shown in Fig. 5.1. The devices on the films cleaned with RCA followed by a dip in the dilute HF solution (RCA/HF) to etch off the native oxide on the surface had ΔV_{FB} of about -17 V. Such a large value of the flat band voltage shift for the devices on the native oxide free surface was in good agreement with the result reported elsewhere [54]. The C-V curve for the latter also showed distortion in the shape referred to as stretch-out along the voltage axis when compared to the shape of the reference curve.

We can use ΔV_{FB} to calculate an effective oxide charge density (Q_o) located at the silicon oxide-silicon interface from the relationship

$$Q_o = -\frac{C_{ox}\Delta V_{FB}}{q} \qquad (5.3.1.1)$$

where C_{ox} is the oxide capacitance per unit area and q is the magnitude of the electron charge. The average values for Q_o for the RCA and the RCA/HF cleaning procedures were 9.3×10^{11} and 4.8×10^{12} cm^{-2}, respectively.

In the high-frequency capacitance method, capacitance is measured as a function of gate bias with measurement frequency being sufficiently high so that the interface traps do not respond. Although interface traps do not follow the ac gate voltage in a high-frequency C-V measurement, they follow very small changes in gate bias as the MOS capacitor is swept from accumulation to inversion. Because interface traps do not respond to the ac gate voltage, they contribute no capacitance to the high-frequency C-V curve. However, they cause the high-frequency C-V curve to stretch out along the gate bias axis as

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the interface trap occupancy may be changed in addition to changing surface space charge.

From the corrected capacitance (C_c) and the calculated value of C_{ox} obtained from the equations in Appendix A, the semiconductor space charge region capacitance (C_S) at each applied bias for the C-V measurements is easily determined from

$$C_s = \frac{C_{ox} C_c}{C_{ox} - C_c}. \tag{5.3.1.2}$$

Once the space charge capacitance is known, the semiconductor surface potential (Ψ_S) is calculated by the use of the computer program attached in Appendix B, assuming that the minority carrier concentration is negligible compared to the majority carrier concentration (This is certainly the case in the accumulation and depletion regions of the C-V curves). The semiconductor surface potential, except when the surface potential is equal to zero, is obtained from [55]

$$Cs(\Psi_s) = \sqrt{\frac{q^2 \varepsilon_S N_A}{2kT}} \frac{\left[1 - e^{-\frac{q\Psi_s}{kT}} + e^{-\frac{2q\Phi_F}{kT}}\left(e^{\frac{q\Psi_s}{kT}} - 1\right)\right]}{\sqrt{\left[\left(e^{-\frac{q\Psi_s}{kT}}\right) + \frac{q\Psi_S}{kT} - 1\right] + e^{-\frac{2q\Phi_F}{kT}}\left[\left(e^{\frac{q\Psi_s}{kT}}\right) - \frac{q\Psi_S}{kT} - 1\right]}}$$

(5.3.1.3)

where ε_s is the dielectric constant of the silicon, q is the magnitude of the electron charge, k is the Boltzmann's constant, T is the temperature, N_A is the substrate carrier concentration, and Φ_F is the Fermi potential.

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For a flat band condition where the surface potential is zero, the space charge capacitance is calculated from [56]

$$C_s(\Psi_s = 0) = \sqrt{\frac{q^2 \varepsilon_s N_A}{kT}}. \tag{5.3.1.4}$$

Interface trap density (D_{it}) can be calculated by the high-frequency C-V method developed by Terman [57]. From the slope of the semiconductor surface potential versus the gate voltage (V_G), the interface trap capacitance $C_{it}(\Psi_s)$ per unit area is obtained by

$$C_{it}(\Psi_s) = C_{ox}\left[\left(\frac{d\Psi_s}{dV_G}\right)^{-1} - 1\right] - C_s(\Psi_s) \tag{5.3.1.5}$$

where $C_S(\Psi_s)$ is the semiconductor capacitance per unit area. The D_{it} at the flat band condition is obtained from the equation

$$D_{it}(\Psi_s = 0) = \frac{C_{it}(\Psi_s = o)}{q} \quad \text{in cm}^{-2}\text{eV}^{-1}. \tag{5.3.1.6}$$

The calculated interface trap densities for the RCA and the RCA/HF cleaning procedures were 5×10^{11} and 2.4×10^{12} $cm^{-2}eV^{-1}$, respectively. It is clear that the samples, with the native oxide etched off the surface prior to the film deposition, had the effective oxide charge density and the interface trap density that were nearly five times higher than for the samples with the native oxide. This may be attributed to the interfacial bonding imperfections, caused by

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the energetic electron induced bond breaking processes in the plasma on the surface where hydrogen or fluorine atoms are terminated [9], [58]. These broken silicon bonds act as positive hole traps [59]. These traps located at the silicon oxide-silicon interface play a critical role in making the C-V curves stretch-out along the dc gate voltage axis as seen in Fig. 5.1.

5.3.2 Improvement of the Film Quality by Annealing

Since many device processes use a dip into a dilute HF solution as a final cleaning step before the film deposition process [60], the effect of annealing on the electrical properties of the films cleaned with the RCA/HF procedure was investigated. Here, two different annealing processes, that of the post-deposition annealing and the post-metallization annealing, were examined. The C-V curves for the samples annealed at different post-deposition annealing temperatures are plotted in Fig. 5.2. The C-V curves generally shifted towards right along the voltage axis upon annealing, indicating smaller magnitude of Q_o in the films. The films also indicated a smaller value for the film dielectric constant as the annealing temperature was raised as previously shown in Fig. 4.5. Increase in capacitance values under strong inversion on the annealed film samples is attributed to lateral spreading of the charges beyond the gate in strong inversion [59]. Figure 5.2 also indicates a decrease in the stretch-out along the voltage axis for the C-V curves with increase in the annealing temperature, resulting in almost the same capacitance gradient at flat band condition as the case of thermal silicon oxide grown at 1000°C in our laboratory in dry O_2 ambient. The C-V curve for the latter is also shown in Fig. 5.2.

In Fig. 5.3, the observed capacitance of the above samples after post-metallization annealing is plotted as a function of the gate voltage. From the location of the C-V curves for the as-deposited films in Fig. 5.3, it is seen that there is no memory of the earlier post-deposition annealing of the samples. The

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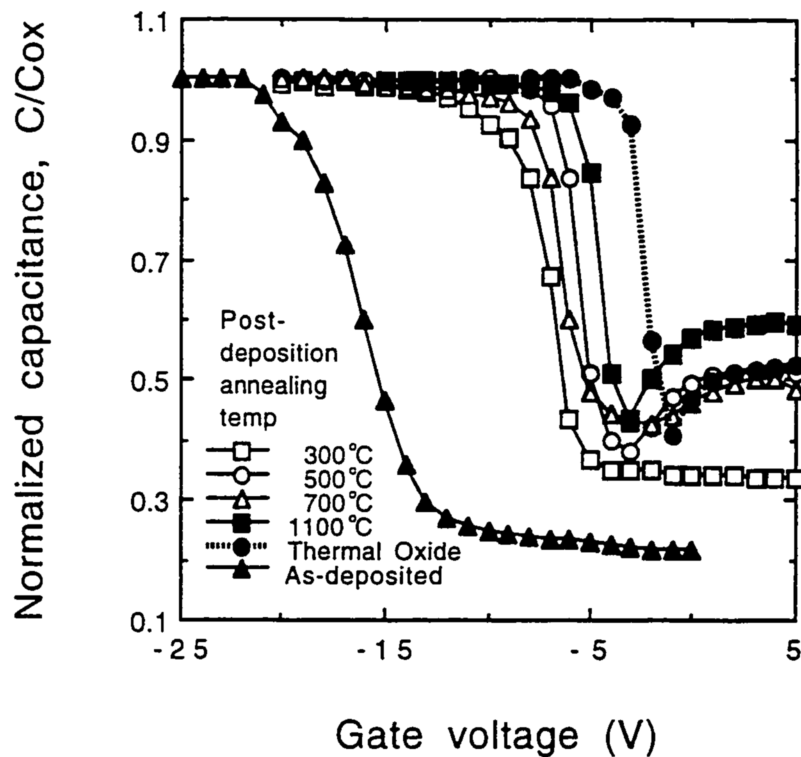

Fig. 5.2. Normalized high frequency capacitance for devices on the silicon oxide films cleaned with RCA followed by a dip in dilute HF as a function of applied gate voltage for post-deposition annealing at different temperatures in N_2 ambient for 30 min. For comparison purposes, values for a thermal silicon oxide film grown at 1000°C are also shown.

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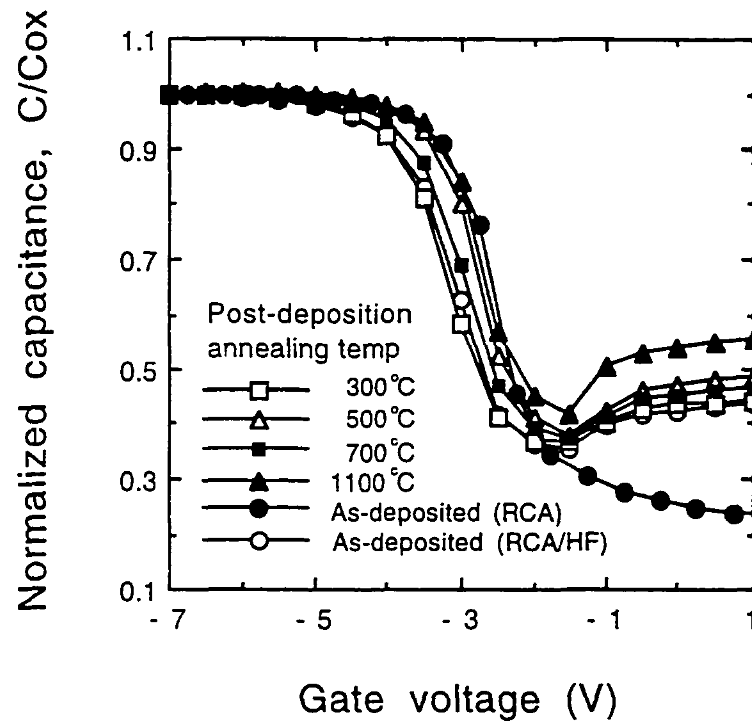

Fig. 5.3. Normalized high frequency capacitance for devices on the silicon oxide films shown in Fig. 5.2 as a function of applied gate voltage after subjecting the samples to post-metallization annealing in 5 % H_2 in N_2 ambient at 400°C for 30 min. The values for the as-deposited films cleaned with two different pre-deposition procedures, RCA and RCA/HF, are also shown.

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V_{FB} for all samples was observed to be in the range of -3.15 ± 0.4 V. These values are very close to V_{FB} of -3.06 V for the films cleaned with the RCA procedure and subjected to the post-metallization annealing. It suggests that the effect of the native oxide removal on the charge distribution in the films can be minimized if the films are annealed in forming gas ambient after metallization [56]. However, the increase in inversion capacitance was still observed for all samples.

A bias-temperature (BT) stress test (± 5 V bias at 200°C for 20 min) was also performed on the as-deposited silicon oxide films cleaned with the RCA/HF procedure. The measured V_{FB} difference before and after the BT test was 0.515 V, corresponding to the mobile ionic charge density of 1.7×10^{11} cm^{-2} in the films which was almost the same value as for the samples cleaned with the RCA procedure.

The calculated effective oxide charge densities Q_o for the samples in Fig. 5.2 and Fig. 5.3 are plotted in Fig. 5.4. Prior to the post-metallization annealing, the oxide charge density decreases with the post-deposition annealing temperature as indicated earlier from 4.5×10^{12} cm^{-2} for the as-deposited silicon oxide films to 8×10^{11} cm^{-2} for the silicon oxide films annealed at 1100°C. This is still a large value compared to 2.8×10^{11} cm^{-2} observed on the thermally grown silicon oxide films in this work. However, there is a significant reduction in the effective oxide charge density after the post-metallization annealing, resulting in its value in the range of 4-5 $\times 10^{11}$ cm^{-2} regardless of the condition of the post-deposition annealing used. This suggests that the annealing in a hydrogen containing ambient reduces the effective oxide charges much more effectively than in a nitrogen ambient at much higher temperatures. An interesting result is that no significant difference in the

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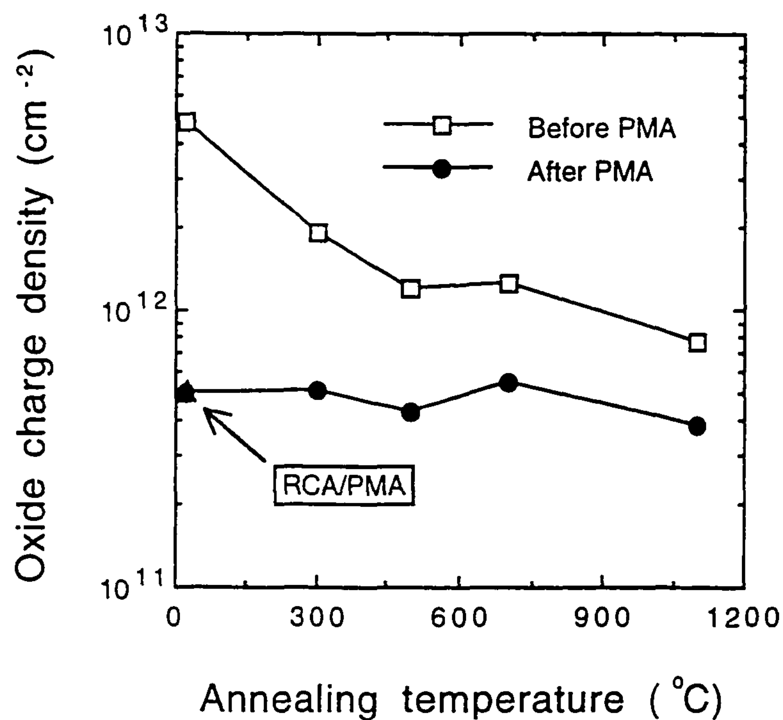

Fig. 5.4. Effective oxide charge density in the silicon oxide films cleaned with RCA followed by a dip in a dilute HF before and after poet-metallization annealing as a function of post-deposition annealing temperatures. Experimental data indicated at 25°C are for the as-deposited films. The observed value after the post-metallization annealing for the as-deposited films on RCA cleaned substrates is also shown (Δ) for comparison purposes.

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effective oxide charge density after post-metallization annealing was observed for the samples on the as-deposited silicon oxide films cleaned with the two different pre-deposition cleaning procedures. The observed effective oxide charge density for the RCA cleaning procedure was 4.3×10^{11} cm^{-2} while that for the RCA/HF cleaning procedure was 5×10^{11} cm^{-2} which are close enough to be within the measurement scatter.

The calculated interface trap densities D_{it}, under the flat band condition (0.26 eV above the valence band edge), for the samples cleaned with the RCA/HF procedure are plotted in Fig. 5.5. The C-V curves shown in Fig. 5.2 and 5.3 are utilized to obtain the data shown in Fig. 5.5. It is clear that the post-metallization annealing in H_2 ambient passivates the interface trap charges much more effectively than the post-deposition annealing at much higher temperatures in N_2. The D_{it} values for this cleaning procedure were calculated to be in the order of 10^{12} and 10^{11} cm^{-2}eV^{-1} for before and after the post-metallization annealing, respectively. The D_{it} value obtained after the post-metallization annealing for the samples on the as-deposited films on the RCA cleaned substrates without the final dip in the dilute HF also showed almost the same value (~ 2×10^{11} cm^{-2}eV^{-1}). These results support the generally stated position [61], [62] that the annealing in a hydrogen-containing ambient after metallization can reduce the interface state density as well as the oxide charges in the films. This hydrogen related passivation is attributed to formation of Si-H bonds in the oxide bulk as well as the interface, and results in the overall improvement of the film quality.

The ramp I-V characteristics of silicon oxide films for different post-deposition annealing temperatures followed by post-metallization annealing are shown in Fig. 5.6. The current conduction mechanism of the silicon oxide films at smaller values of electric field, E, ($\leq$ 3.5 MV/cm) seems to be identical for all

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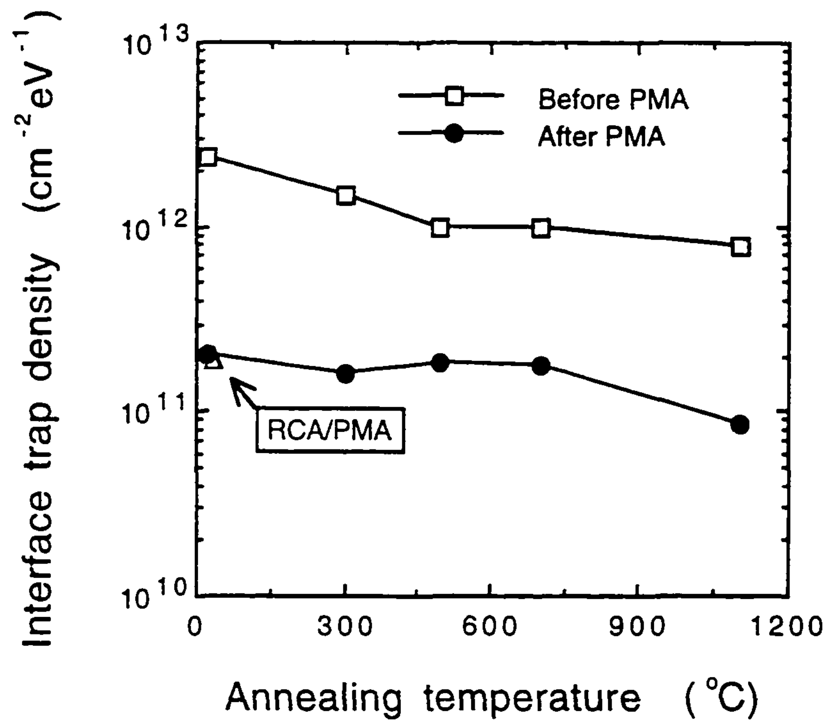

Fig. 5.5. Interface trap density under the flat band condition before and after poet-metallization annealing as a function of post-deposition annealing temperatures. The substrates were cleaned with the RCA/HF procedure. Experimental data at 25°C are for the as-deposited films. The observed value after the post-metallization annealing for the as-deposited films on RCA cleaned substrates is also shown (Δ) for comparison purposes.

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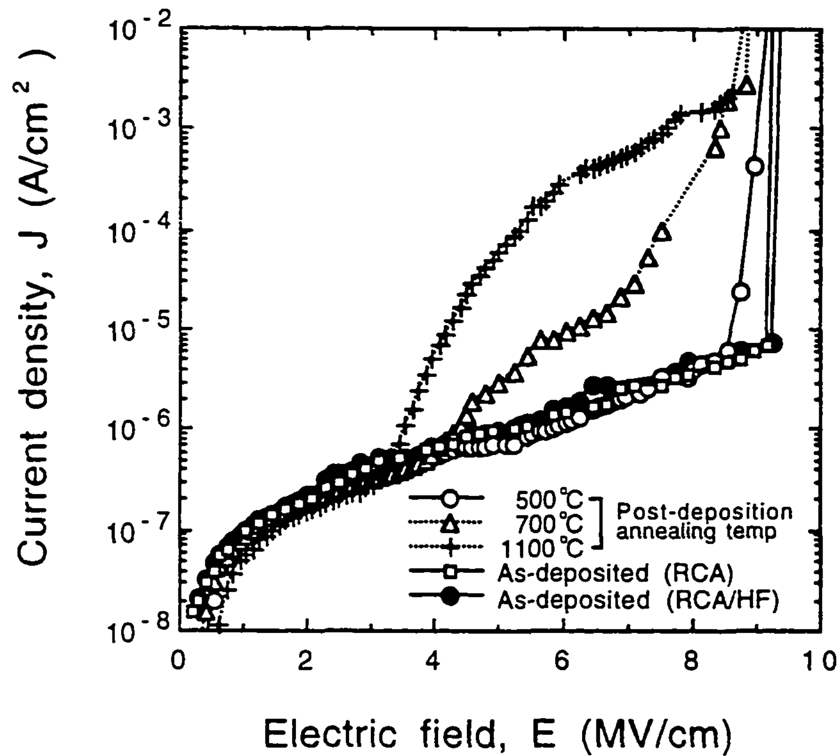

Fig. 5.6. J-E characteristics of the silicon oxide films for various post-deposition annealing temperatures followed by post-metallization annealing. The voltage ramp rate is fixed at 0.5 V/sec. The bias polarity corresponds to electron injection from the gate.

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cases, presumably dominated by the hopping of the thermally excited electrons from one isolated trap to another [63]. For the silicon oxide films with the post-deposition annealing temperature of 500°C or lower for both pre-deposition cleaning procedures used, the hopping mode of conduction dominates till catastrophic dielectric breakdown condition is reached. However, for the silicon oxide films subjected to the post-deposition annealing at 700°C and higher, the current increases at about 3.5 MV/cm showing a linear relationship for $ln(J/E^2)$ versus 1/E. This behavior is similar to the Fowler-Nordheim dominated conduction process. The model to explain this behavior of current conduction processes is not available at this time.

A distribution of catastrophic dielectric breakdown fields of the as-deposited silicon oxide films cleaned with the RCA and the RCA/HF procedures is shown in Fig. 5.7. The measurements were carried out after the post-metallization annealing step. Fifty devices were used in the measurement done at room temperature and the voltage was increased at a ramp rate of 0.5 V/sec with the gate biased negative with respect to the substrate. The distribution showed no significant differences except for more widely distributed breakdown for the devices on silicon oxide films cleaned with the RCA procedure, particularly at the moderate values of the electric field. The early breakdown (≤ 3 MV/cm) of the samples cleaned with the RCA and the RCA/HF procedure, presumably caused by the particles or micropores in the films, was seen on 27 % and 30 % of devices tested, respectively. The intrinsic breakdown (≥ 8 MV/cm) of the samples cleaned with the RCA and the RCA/HF procedure was 64 % and 66 %, respectively. The measured average dielectric breakdown field was 7.1 MV/cm for the RCA and 7.3 MV/cm for the RCA/HF cleaning procedure.

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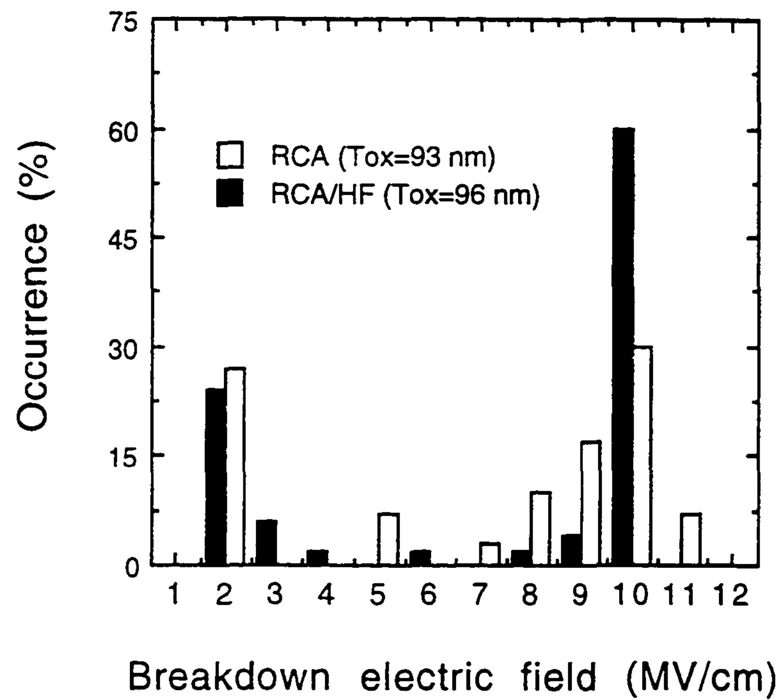

Fig. 5.7 Distribution of occurrence of catastrophic dielectric breakdown as a function of electric field for the as-deposited silicon oxide films cleaned with two different pre-deposition cleaning procedures. The measurements were performed after poet-metallization annealing at 400°C for 30 min in a forming gas ambient. T_{ox} is a silicon oxide thickness.

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The silicon oxide film properties related to the pre-deposition cleaning procedure are summarized in Table 5.1 and 5.2. The quality degradation caused by the native oxide removal on the substrates prior to film deposition can be reduced by performing the post-metallization annealing at 400°C in forming gas ambient, resulting in no significant differences for characteristics of charge distribution and dielectric breakdown behavior.

5.4 Conclusion

In summary, the effect of native oxide removal from the substrate surface before film deposition and the improvement of electrical properties of PECVD silicon oxide films deposited at 120°C using Si_2H_6 and N_2O by annealing are examined. The films deposited on the native oxide free surface showed five times more effective oxide charge and flat band interface trap densities than the films deposited on native oxide. In the former case, post-deposition annealing in N_2 reduced the effective oxide charge densities with the higher annealing temperature resulting in smaller charge density values. The improvement in the film quality due to reduction in both the effective oxide charge and the interface trap density was accomplished much more effectively by the post-metallization annealing at 400°C in forming gas for 30 min. The values for both these charge densities were comparable after this post-metallization annealing regardless of the substrate cleaning procedure used and regardless of the post-deposition annealing in N_2. The films deposited on substrates without native oxide and annealed at 700°C and higher temperatures during post-deposition annealing had higher current densities at electric fields greater than 3.5 MV/cm. No significant difference in the dielectric breakdown field was observed after post-metallization annealing for the samples having undergone the two different pre-deposition cleaning procedures. The silicon oxide film quality deposited at 120°C followed by annealing at 400°C in the forming gas ambient shows

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Table 5.1. Summary of high-frequency C-V measurements for the silicon oxide films cleaned with two different pre-deposition cleaning procedures.

Pre-depo cleaning	Effective oxide charge density ($\times 10^{11}$ cm^{-2})		Interface trap density at flat band condition ($\times 10^{11}$ cm^{-2}eV^{-1})	
	As-deposited	After PMA[a]	As-deposited	After PMA[a]
RCA	9.3	4.3	5.0	1.9
RCA/HF	48.0	5.0	24.0	2.0

[a]PMA means the post-metallization annealing at 400°C for 30 min in 5 % H_2 in N_2 ambient.

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Table 5.2. Intrinsic dielectric breakdown distribution for devices cleaned with two different pre-deposition cleaning procedures.

Pre-depo cleaning	Dielectric breakdown measured after PMA[b]		
	E_{av}[a](MV/cm)	$\leq$ 3 MV/cm	$\geq$ 8 MV/cm
RCA	7.1	27 %	64 %
RCA/HF	7.3	30 %	66 %

[a]E_{av} means the average catastrophic dielectric breakdown field.

[b]PMA means the post-metallization annealing at 400°C for 30 min in 5 % H_2 in N_2 ambient.

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potential for application as passivating and insulating layers in the microelectronics industry.

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CHAPTER 6
FLUORINATED SILICON OXIDE FILM DEPOSITION

6.1 Introduction

As the complexity of integrated circuits increases, the role of interlayer dielectric films deposited at low temperatures and with low dielectric constants has become more important to prevent the degradation of device operating speed caused by parasitic capacitances [64], [65]. The rate of signal transmission within the device is related to the delay constant (RC)

$$RC = \frac{\rho_m \varepsilon_{ox} L_m^2}{T_m T_{ox}} \tag{6.1.1}$$

where ρ_m is the resistivity of the interconnection metal, L_m is the length of the interconnection metal, and ε_{ox} is the dielectric constant of the intermetal dielectric. T_m and T_{ox} are the thickness of the interconnection metal and intermetal dielectric, respectively. A low RC can be achieved by reducing the resistance of the interconnection metal, the dielectric constant of the intermetal dielectric, or by modifying the interconnection metal schemes. The most preferred way to reduce the delay constant at this moment is the use of a intermetal dielectric with a low dielectric constant.

One of the intermetal dielectrics which has received much attention recently is fluorinated silicon oxide (F_xSiO_y), where incorporation of fluorine into the Si-O network causes the reduction of the dielectric constant as a result of it being the most electronegative and the least polarizable element in the periodic table. Different approaches [66]-[69] in depositing fluorinated silicon oxide films include PECVD, electron cyclotron resonance plasma CVD or atmospheric

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pressure CVD using silicon precursors such as SiF_4, $FSi(OC_2H_5)_3$ or $Si(OC_2H_5)_4$ in the presence of NF_3, CF_4, N_2O or C_2F_6.

In this chapter, details of deposition of PECVD fluorinated silicon oxide films at 120°C utilizing CF_4 as the fluorine source into the silicon oxide deposition process with Si_2H_6 and N_2O are discussed. The chemical and electrical properties of the films are studied as a function of the flow rate ratio of CF_4 to Si_2H_6 in the film deposition process.

6.2 Experiment

The starting materials used in this study were p-type chemically polished 4" diameter silicon wafers with (100) orientation and 10 Ω·cm resistivity. The wafers were cleaned as per the standard RCA cleaning procedure. Films of nominally 100 nm thickness were deposited by flowing 40 sccm of 4.8 % Si_2H_6 in He, 100 sccm of N_2O, and 0-48 sccm of CF_4 in the deposition chamber. The CF_4 flow rate was the only process parameter varied in this experiment which resulted in the flow rate ratio of CF_4 to Si_2H_6 varying from 0 to 24. The deposition temperature was maintained at 120°C with the top electrode at 60°C. The process pressure and rf power were 700 mTorr and 50 W, respectively.

The thickness and refractive index of the films were measured using an Applied Materials ellipsometer model II. The etch rate was obtained by dipping the films in the P-etch solution. The vibrational properties in the 600-1400 cm^{-1} wave number range were observed using a Perkin Elmer Model 1600 Fourier transform infrared spectrophotometer with a resolution of 4 cm^{-1}. A bare silicon wafer was used as a background reference. Aluminum gate MOS capacitors with an area of 2.7×10^{-3} cm^2 were fabricated using standard photolithography techniques and annealed in a forming gas (5 % H_2 in N_2) ambient at 400°C for 30 min prior to C-V measurements. The C-V measurements were carried out by superimposing a 25 mV ac signal at 1 MHz on a dc voltage with a HP 4275A

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LCR meter. A dc voltage sweep rate of 1V/sec was used. The dielectric constant of the film was calcuiated from the values of capacitance and conductance in accumulation.

6.3 Results and Discussion

In Fig. 6.1, film deposition rate and chemical etch rate in the P-etch solution are plotted as a function of flow rate ratio of CF_4 to Si_2H_6. The deposition rate increases with increasing the flow rate ratio until the flow rate ratio is 12 and then becomes independent of the gas flow ratio with its maximum value at 14.3 nm/min. The deposition rate without the addition of CF_4 was about 13.5 nm/min. The film etch rate without CF_4 flow was approximately 2 nm/sec. As the flow rate ratio increases, the etch rate increases gradually up to about 3.5 nm/sec at the flow rate ratio of 22 and then shows a dramatic increase to 5.8 nm/sec for the flow ratio of 24. Higher etch rates reflect that the film deposited at higher flow rate ratio may have more strained bonds and micropores associated with more fluorine incorporation into the Si-O network.

Infrared transmission spectra of the films deposited at different flow rate ratio of CF_4 to Si_2H_6 are shown in Fig. 6.2. The characteristic peak of Si-O-Si asymmetric stretching motion located around 1075 cm^{-1} is evident. Also from the figure, the peak intensity of Si-F stretching motion [70] located at 924 cm^{-1} becomes distinct and bigger as the flow rate ratio increases. The Si-O-Si stretching vibration mode is commonly used to study the structural property of the silicon oxide films. The Si-O-Si stretching peak wave number obtained from infrared transmission measurements and refractive index obtained from ellipsometric measurements for the films as a function of flow rate ratio of CF_4 to Si_2H_6 are plotted in Fig. 6.3. As the flow rate ratio increases, the peak wave number increases: for example, from 1059 cm^{-1} for films deposited at ratio of 0, corresponding fluorine-free silicon oxide, to 1070 cm^{-1} for films deposited at

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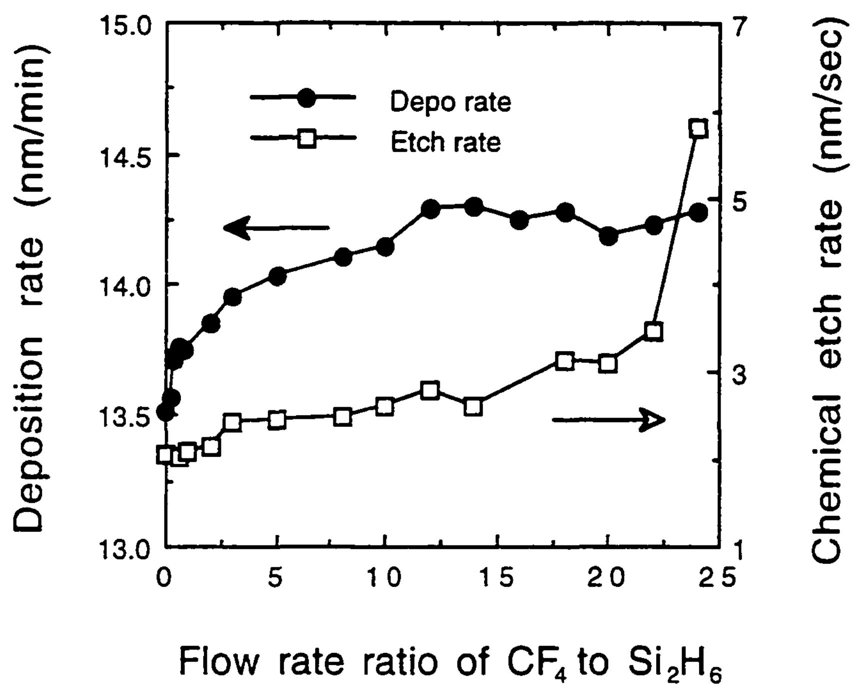

Fig. 6.1. Deposition rate and etch rate in the P-etch solution of the films as a function of flow rate ratio of CF_4 to Si_2H_6 during film deposition. Films were deposited at 120°C by flowing 40 sccm of 4.8 % Si_2H_6 in He (2 sccm of Si_2H_6), 100 sccm of N_2O, and 0-48 sccm of CF_4. The process pressure and rf power were 700 mTorr and 50 W, respectively.

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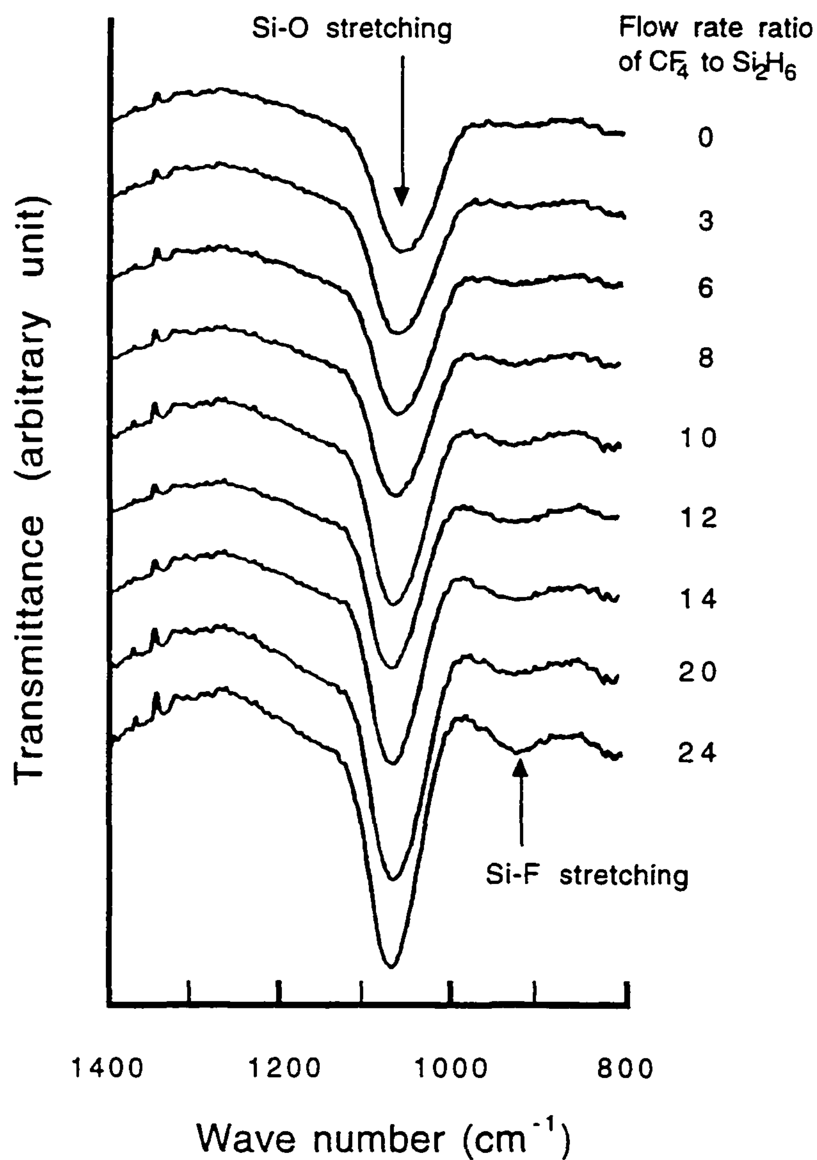

Fig. 6.2. Infrared transmission spectra of the films deposited with different flow rate ratios of CF_4 to Si_2H_6. The process conditions were the same as in Fig. 6.1. The characteristic peaks of Si-O and Si-F stretching motion are marked.

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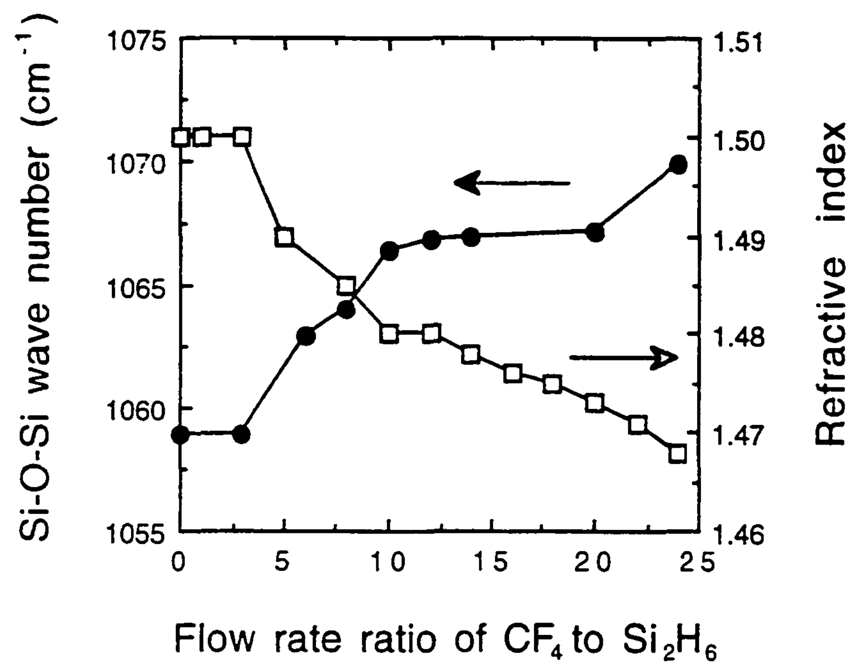

Fig. 6.3. Si-O-Si asymmetric stretching peak wave number and refractive index of the film as a function of flow rate ratio of CF_4 to Si_2H_6 during film deposition.

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ratio of 24. Meanwhile, the refractive index decreases as the flow rate ratio increases from 1.50 for films deposited at ratio of 0 to 1.468 for films deposited at ratio of 24. The stretching wave number and refractive index have not reached the values of the silicon oxide films grown by thermal oxidation in dry O_2 at 1000°C in our laboratory which are 1076 cm^{-1} for the stretching peak wave number and 1.46 for the refractive index.

The Lorentz-Lorenz relationship links the refractive index (n) of the film to the film density (ρ)through

$$\left[\frac{n^2-1}{n^2+2}\right]\frac{M}{\rho}=\frac{4\pi R}{3} \qquad (6.3.1)$$

where R and M are the molecular polarizability and the molecular weight, respectively. If no significant change in the molecular weight M is assumed, then decrease either in the film density or in the molecular polarizability causes the decrease in the refractive index. Hence, a replacement of Si-O bonds by Si-F bonds in fluorinated silicon oxide films shows two distinct effects. First, fluorine incorporation promotes the structural relaxation of film network, resulting in decrease in film density as evident from the shift of the stretching wave number to higher values. There is an ample evidence that for silicon oxide films, the stretching wave number increases with decreasing film density [70]. Second, fluorine incorporation causes less polarizability of films, driving the films to a smaller value for the dielectric constant. It is also observed that a linear plot of the Si-O-Si stretching peak wave number (ω) vs. refractive index for films deposited at different flow rate ratios yielded $dn/d\omega$ = -2.9 × 10^{-3} cm which is somewhat higher in magnitude than -1.7 × 10^{-3} cm for silicon oxide films [49] thermally grown at temperatures between 700°C and 1000°C.

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The effect of fluorine incorporation into the Si-O network in terms of change in flat band voltage was also studied using C-V measurement and is shown in Fig. 6.4. The devices on the fluorine-free silicon oxide films showed the flat band voltage of -1.75 V, corresponding to the flat band voltage shift of -0.92 V with respect to the work function difference of -0.83 V. As the addition of fluorine into the films increases, the flat band voltage approached the value of the work function difference indicating a decrease in the net effective positive charge density at the silicon-insulator interface. However, the films deposited at flow rate ratio of 14 and higher showed that the flat band voltage returned to the value of fluorine-free silicon oxide films, suggesting deterioration of the interface and the film resulting from larger concentration of fluorine [71].

The relative dielectric constant is calculated from the measured values of the capacitance in the accumulation region of MOS devices and is plotted as a function of flow rate ratio of CF_4 to Si_2H_6 in Fig. 6.5. The dielectric constant of the films deposited at flow ratio of 0 for fluorine-free silicon oxide was 4.82. Increase in flow rate ratio caused a reduction of the dielectric constant of the films. However, no more decrease in the dielectric constant was observed for films deposited at a ratio of 8 and higher, resulting in a nearly constant value of 4.25 for the dielectric constant. This value is 12 % lower dielectric constant observed on the fluorine-free silicon oxide films. The minimum value of 4.25 is close to the value of 4.16 for the fluorine-free silicon oxide films deposited at 120°C by PECVD and annealed at 1100°C. The dielectric constant depends on the hydroxyl content in the film [3]. Presence of fluorine-containing species during film deposition is expected to favor a replacement of the hydroxyl-containing bonds by Si-F bonds and, in turn, drive the film dielectric constant to a lower value. From the results of both the flat band voltage and the dielectric constant measurements, the optimum flow rate ratio of CF_4 to Si_2H_6 seems to

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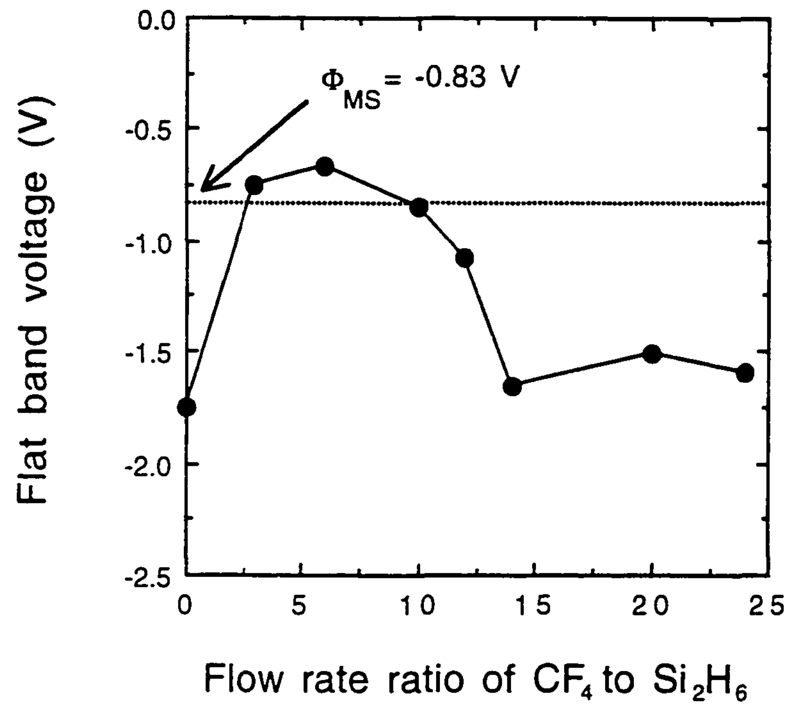

Fig. 6.4. Dependence of flat band voltage of the films as a function of flow rate ratio of CF_4 to Si_2H_6 during film deposition. The broken line is drawn for Φ_{MS}= -0.83 V. The post-metallization annealing was carried out in 5 % H_2 in N_2 ambient at 400°C for 30 min prior to measurements.

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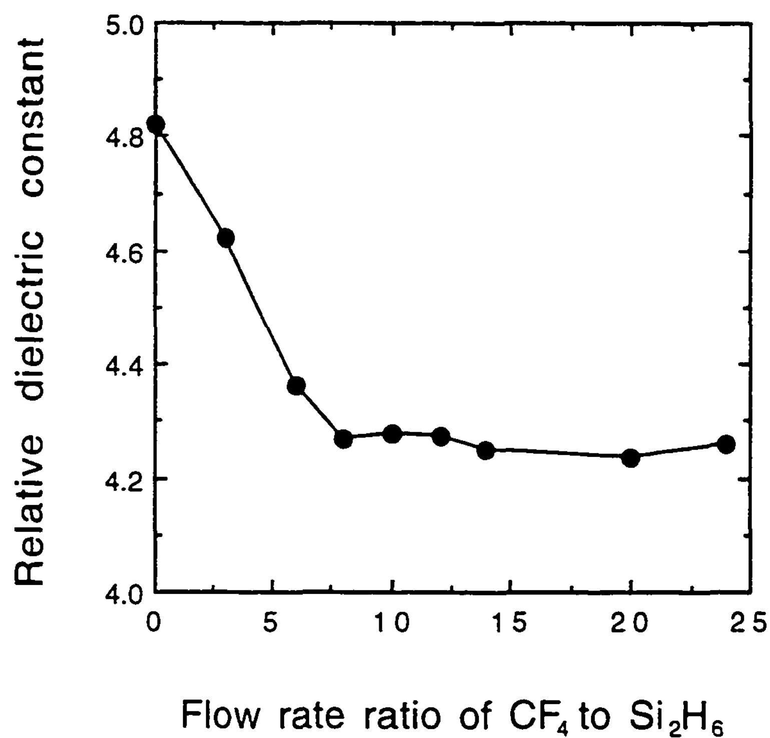

Fig. 6.5. Dependence of dielectric constant of the films as a function of flow rate ratio of CF_4 to Si_2H_6 during film deposition. The post-metallization annealing was carried out in 5 % H_2 in N_2 ambient at 400°C for 30 min prior to measurements.

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be in the range of 8-10, which corresponds to 16-20 sccm of CF_4 for 2 sccm of Si_2H_6 flow in our deposition chamber.

6.4 Conclusion

The results in this work show the importance of the flow rate ratio of CF_4 to Si_2H_6 to get high-quality PECVD fluorinated silicon oxide films deposited at 120°C with Si_2H_6 as the silicon source. As the flow rate ratio increases, the deposition rate increases, the films become more porous and less polarizable. However, too much incorporation of fluorine into Si-O network degrades the electrical and physical properties of the films.

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CHAPTER 7
HIGH QUALITY FLUORINATED SILICON OXIDE FILM

7.1 Introduction

In this chapter, electrical properties of fluorinated silicon oxide films deposited with the gas flow ratio of CF_4 to Si_2H_6 set to 10 are detailed. Results on the effective oxide charge density and the interface trap density as a function of the energy level location deduced from the high-frequency C-V measurements are presented. The film reliability estimated with the ramp I-V techniques is also discussed. The improvements in the film quality due to fluorine incorporation are summarized and comparisons made with the fluorine-free silicon oxide films.

7.2 Experiment

Chemically polished, boron doped 4 inch silicon wafers with (100) orientation and 10 Ω·cm resistivity were used as the substrates. The wafers were cleaned as per the standard RCA cleaning procedure. The fluorinated silicon oxide films of nominally 100 nm thickness were deposited by flowing 40 sccm of 4.8% Si_2H_6 in He, 100 sccm of N_2O, and 20 sccm of CF_4 in the deposition chamber. The CF_4 gas line was closed for the silicon oxide film deposition. The deposition temperature was maintained at 120°C with the top electrode temperature at 60°C. The deposition pressure and rf power were 700 mTorr and 50 W, respectively.

Aluminum gate MOS capacitors were fabricated using standard photolithography techniques with a predefined gate area of 2.7×10^{-3} cm^2 and then subjected to the post-metallization annealing in 5 % H_2 in N_2 ambient for 30 min at 400°C. The thickness of the deposited films was measured using an Applied Materials ellipsometer model II. The C-V measurements were carried

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out by superimposing a 25 mV ac signal at 1 MHz with a HP 4275A LCR meter. A dc voltage sweep rate of 10 mV/sec was used. The I-V characteristics were obtained with a HP 4140 voltage source and a Keithley 485 picoammeter.

7.3 Results and Discussion

The C-V curves for the silicon oxide and fluorinated silicon oxide films are shown in Fig. 7.1. The work function difference between the gate material and the substrate for the substrate doping used here is -0.83 V. The devices on the silicon oxide films without fluorine showed the flat band voltage of -1.75 V which corresponds to an additional flat band voltage shift of -0.92 V after the contribution due to the work function difference is taken into account. The devices on the fluorinated silicon oxide films had smaller flat band voltage of about -1 V.

The C-V curve for the latter showed a slight distortion, particularly near the accumulation and in the depletion regions, referred to as stretch-out along the voltage axis. A careful investigation based on an earlier study by Hughes [72] indicates that this is associated with donor-type interface traps located in the lower half of the energy band gap.

The effective oxide charge density values calculated from the shift of the flat band voltage for the silicon oxide and the fluorinated silicon oxide films were 2.56×10^{11} cm^{-2} and 4.12×10^{10} cm^{-2}, respectively. It indicates that the oxide charges for the fluorinated silicon oxide films were decreased by a factor of 1/6 compared to that observed on the silicon oxide films. This may be attributed to replacement of the hydroxyl or defect-related bondings in the oxide network by fluorine.

The interface trap densities calculated from the procedures described in Chapter 5 for the silicon oxide and the fluorinated silicon oxide films are plotted as a function of the energy level location from the majority band edge

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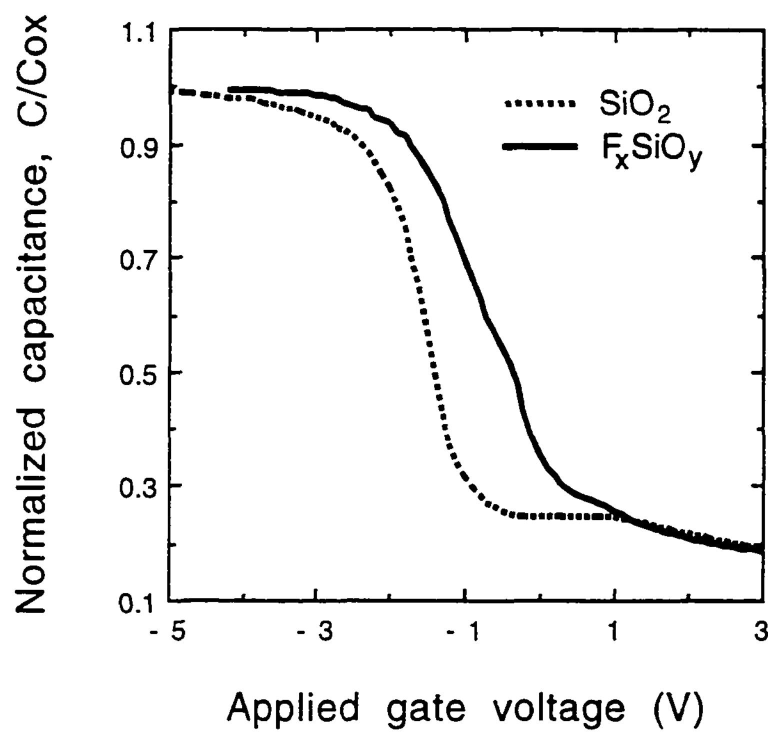

Fig. 7.1. High-frequency normalized capacitance as a function of applied gate voltage for devices on the silicon oxide and the fluorinated silicon oxide films. The post-metallization annealing was carried out in 5 % H_2 in N_2 ambient at 400°C for 30 min prior to measurements.

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E_v in Fig. 7.2. The interface trap density distributions seem to follow the W-shape having two minimums as reported elsewhere[73]. For the fluorinated silicon oxide films, two minimums of 1.99×10^{11} $cm^{-2}eV^{-1}$ at 0.165 eV and 1.07×10^{11} $cm^{-2}eV^{-1}$ at 0.395 eV both from the top of the valence band were obtained. Meanwhile for the silicon oxide films, the observed two minimums were 1.25×10^{11} $cm^{-2}eV^{-1}$ at 0.15 eV and 2.13×10^{11} $cm^{-2}eV^{-1}$ at 0.36 eV both from the top of the valence band. The interface trap density distributions for the two films show slight differences in that the interface trap density values for the fluorinated silicon oxide films in the energy range ($E - E_v$) of about 0.15 eV and lower are slightly higher and in the range of 0.35-0.55 eV are slightly lower than those for the corresponding values in the silicon oxide films. These are consistent with the observed shapes of the C-V curve.

A typical I-V characteristic curve of the MOS structure fabricated on the fluorinated silicon oxide films is shown in Fig. 7.3. This time-zero dielectric breakdown measurements are taken at room temperature with the voltage ramp rate set at 0.5 V/sec. The polarity of the field causes carrier accumulations at the substrate surface, corresponding to electron injection from the gate. The hopping current dominates at low electric fields (< 2 MV/cm). The onset of current injection occurs at the electric field of about 2 MV/cm. The electric field which drives the films into intrinsic breakdown phenomenon starts at about 8.5 MV/cm. The inserted plot shows the linearity for $ln(J/E^2)$ versus $1/E$ relationship consistent with the simple Fowler-Nordheim mechanism [7]. The measured value of the slope was about 2.88 eV which is somewhat smaller than the well-accepted barrier height of 3.2 eV and may indicate an additional tunneling component from the metal gate to the silicon conduction band.

Distribution of the destructive dielectric breakdown field strength for the fluorinated silicon oxide films along with the distribution for the silicon oxide

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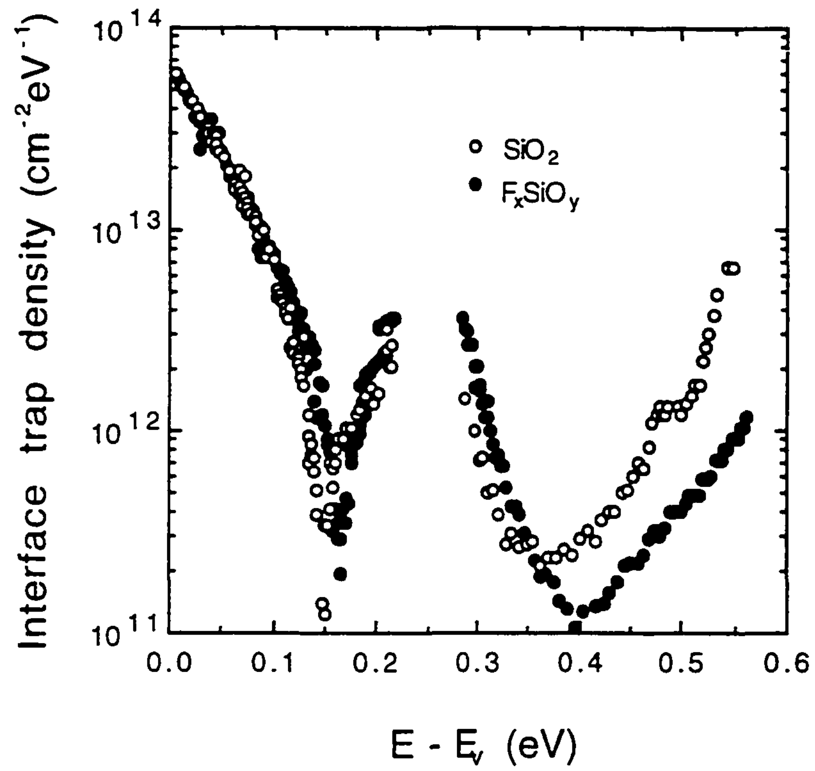

Fig. 7.2. Interface trap density vs. the energy level location from the majority carrier band edge (E_V) for the silicon oxide and the fluorinated silicon oxide films.

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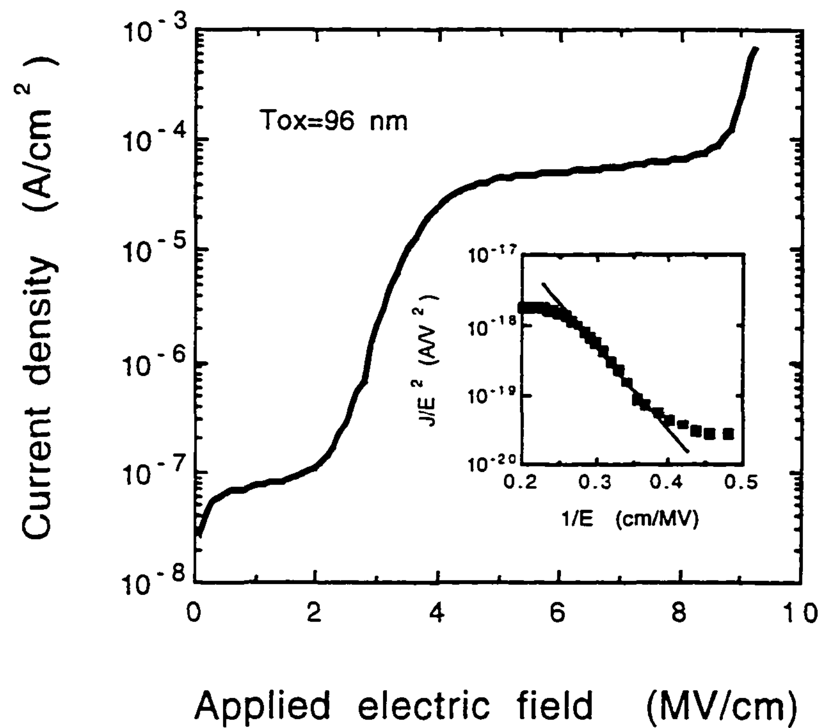

Fig. 7.3. Typical J-E characteristic of the fluorinated silicon oxide films with a thickness of 96 nm. The voltage ramp rate is fixed at 0.5 V/sec. The bias polarity corresponds to electron injection from the gate. The inserted figure is a plot of *ln*(J/E^2) vs. 1/E described by the simple Fowler-Nordheim expression.

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films without fluorine are shown in Fig. 7.4 and summarized in Table 7.1. The data for the fluorine-free silicon oxide films used in Fig. 5.7 are shown for comparison purposes. Fifty devices were used in the measurement. The early breakdowns at field values of ≤ 3 MV/cm were observed on 27 % of devices on the silicon oxide films and on 2 % of devices on the fluorinated silicon oxide films. At the higher end, 88 % of devices on the fluorinated silicon oxide films had the breakdown field strength of 8 MV/cm and higher, compared to only 64 % for the devices on the silicon oxide. The measured average dielectric breakdown field strength for the fluorinated silicon oxide films was 8.91 MV/cm which was 1.81 MV/cm higher than the value of 7.1 MV/cm measured on the devices on the silicon oxide films. This indicates that significantly fewer devices on the fluorinated silicon oxide films have early breakdowns and that there is an overall shift of the breakdown distribution to higher values of electric field. This may be one of the most promising effect of fluorine addition into the silicon oxide films which improves the film quality by reducing significant portions of early failures.

7.4 Conclusion

In summary, electrical characteristics of the fluorinated silicon oxide films prepared by plasma enhanced chemical vapor deposition at 120°C using Si_2H_6 as silicon precursor and CF_4 as fluorine precursor were studied. The addition of fluorine into Si-O network results in smaller shift in flat band voltage due to oxide and interface charges and significantly fewer early breakdown compared to the fluorine-free silicon oxide films. These films have a strong potential for the use as interlayer dielectric material making available a low temperature and high quality film deposition process for submicron device fabrication.

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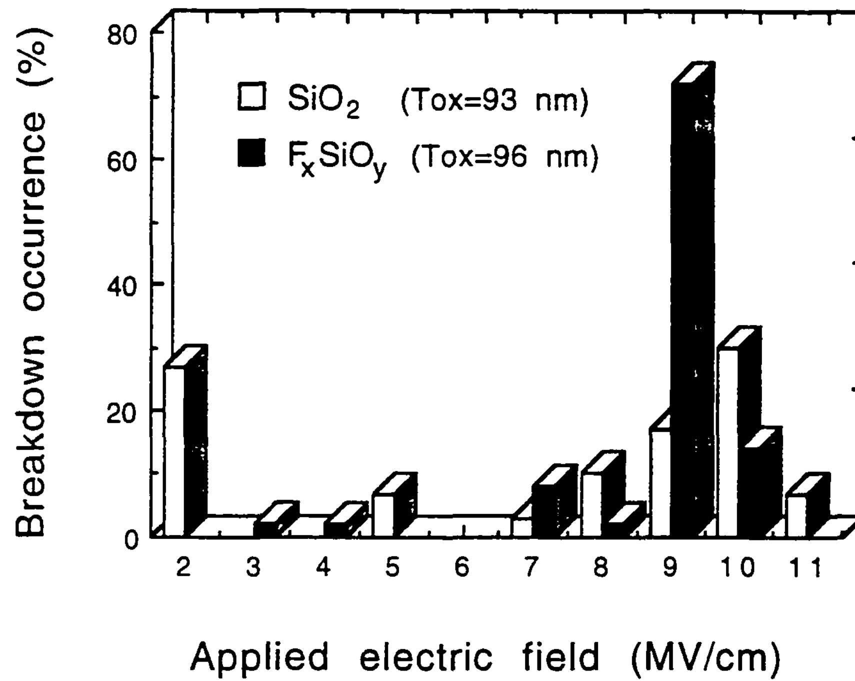

Fig. 7.4. Distribution of breakdown occurrences as a function of electric field strength for the silicon oxide and the fluorinated silicon oxide films. Fifty devices were used in the measurement done at room temperature. T_{ox} stands for oxide thickness.

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Table 7.1. Comparison of intrinsic dielectric breakdown distributions for the silicon oxide and the fluorinated silicon oxide films.

Films	Dielectric breakdown measured after PMA		
	E_{av} (MV/cm)	≤ 3 MV/cm	≥ 8 MV/cm
SiO_2	7.1	27 %	64 %
F_xSiO_y	8.9	2 %	88 %

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CHAPTER 8
SUMMARY

PECVD silicon oxide and fluorinated silicon oxide films prepared at low temperature with Si_2H_6 as silicon precursor, as interlevel dielectrics in microelectronics devices, were studied.

The film deposition was limited by the mass transport regime, resulting in nearly temperature independent deposition rates. The stoichiometric silicon oxide films were obtained when the gas flow ratio of N_2O to Si_2H_6 was in the range of 50-150. Films deposited at low deposition rate of 7-15 nm/min reveal reproducible deposition characteristics and a thickness uniformity of within ± 3 % across 4 inch diameter wafer. The characterization process for the silicon oxide films deposited at 120°C showed that the film etch rate was comparable to that obtained for films deposited by TEOS-based PECVD at 400°C and the leakage current was comparable to the value for the films deposited at 350°C with conventional SiH_4 precursor.

The structural properties of the silicon oxide films deposited at 120°C were also investigated. The shift of Si-O-Si stretching peak wave number of the as-deposited silicon oxide films compared to the undensified thermal silicon oxide films was attributed to 9.4 % increase in the film density, resulting in smaller Si-O-Si bridging bond angle of 138°. It was also believed that the high temperature annealing resulted in the reduction of hydroxyl-containing species in the film and, in turn, drove the dielectric constant towards that of the thermal silicon oxide films.

The effect of native oxide removal from the silicon substrate surface and annealing on the silicon oxide films deposited at 120°C was studied. The

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effective oxide charge and the interface trap densities for the as-deposited silicon oxide films with the native oxide etched off the substrate surface prior to the film deposition were nearly five times higher than for the as-deposited films without the removal of the native oxide. Post-deposition annealing in N_2 reduced the effective oxide charges for the films deposited on substrates without the native oxide. However, a 30 min post-metallization anneal at 400°C in 5 % H_2 in N_2 ambient reduced both the effective oxide charge density and the interface trap density much more effectively. The charge densities and the dielectric breakdown field values were comparable after this post-metallization annealing regardless of the substrate cleaning procedure and the post-deposition annealing cycle in N_2.

Fluorinated silicon oxide films have been deposited at 120°C using CF_4, N_2O and Si_2H_6 and the dependency of film properties on gas flow ratio of CF_4 to Si_2H_6 was studied. The optimum gas flow ratio of CF_4 to Si_2H_6 was observed to be in the range of 8-10. This process condition resulted in a dielectric constant of 4.25 which was 12 % lower than the value obtained for fluorine-free silicon oxide films. A linear relationship of the Si-O-Si stretching peak wave number (ω) vs. refractive index (n) for the fluorinated silicon oxide films deposited at different flow rate ratios yielded a value of -2.9×10^{-3} cm for $dn/d\omega$.

Electrical characteristics of the fluorinated silicon oxide films deposited with the gas flow ratio of CF_4 to Si_2H_6 set at 10 showed that the addition of fluorine into Si-O network resulted in a decrease in the effective oxide charges to as low as 1/6 of the value for the fluorine-free silicon oxide films. It also improved the film breakdown property by reducing early failures, resulting in the measured average dielectric breakdown field strength of 8.91 MV/cm.

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APPENDIX A
SERIES RESISTANCE CORRECTION

By high-frequency measurement of the capacitance and the conductance of a MOS capacitor in strong accumulation, the series resistance (R_S) can be determined from

$$R_s = \frac{G_m}{G_m^2 + 4\pi^2 f^2 C_m^2} \quad \text{(A.1)}$$

where f is the measurement frequency and G_m and C_m are the measured conductance and capacitance, respectively. The corrected oxide capacitance (C_{ox}) in strong accumulation is obtained from

$$C_{ox} = C_m\left[1 + \left(\frac{G_m}{2\pi f C_m}\right)^2\right]. \quad \text{(A.2)}$$

Once the series resistance is known, the influence of it on the capacitance can be calculated for determining the true corrected capacitance (C_c) at each applied bias from

$$C_c = \frac{\left(G_m^2 + 4\pi^2 f^2 C_m^2\right)C_m}{\left[G_m - \left(G_m^2 + 4\pi^2 f^2 C_m^2\right)R_s\right]^2 + 4\pi^2 f^2 C_m^2}. \quad \text{(A.3)}$$

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APPENDIX B

C-V MEASUREMENT PROGRAM

This program in Basic language edited by Mr. Golden Hwaung is used to measure high-frequency C-V characteristics of MOS capacitor system. The main computer (IBM PC) is connected to a HP 4275A LCR meter interfaced with a HP 4140B power source. The minimum step for the applied gate voltage is programmed to be 10 mV. The procedure in Appendix A is used to obtain the corrected capacitance from the measured values of capacitance and conductance. The procedure described in Chapter 5 is also used to calculate the semiconductor surface potential.

```
10    REM THE PROGRAMMER IS GOLDEN
20    OPTION BASE 1
30    DIM A(1501), B(1501), C(1501), D(1501), E(1501), R(1501),
      K(1501), W(1501)
40    PRINT "THIS PROGRAM IS TO DO THE CV MEASUREMENT,
      PLEASE PUT YOUR SAMPLE IN THE PROBE STATION, TURN
      ON THE HP 4140B AND HP4275A"
50    PRINT "IF THE PROGRAM BREAKS FOR SOME REASON OR
      YOU WANT TO DO THE MEASUREMENT AGAIN, TYPE CV
      THEN HIT ENTER KEY TO RE-RUN THE PROGRAM"
60    LINE INPUT "WHAT IS THE WAFER NAME : ";W$
70    INPUT "WHAT IS THE START VOLTAGE :";S
80    S = S × 100
90    INPUT "WHAT IS THE STOP VOLTAGE :";O
100   O = O × 100
110   INPUT "WHAT IS THE STEP VOLTAGE :";E
120   E = E × 100
130   OPEN "GPIB0" FOR OUTPUT AS #1
140   OPEN "GPIB0" FOR INPUT AS#2
150   PRINT #1, "ABORT"
160   PRINT #1, "REMOTE 16"
170   PRINT #1, "REMOTE 17"
180   PRINT #1, "OUTPUT 16#3; A6E"
```


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```
190     PRINT #1, "OUTPUT 17#23; T1A2B3C1D0F17H1I0X1R31E"
200     PRINT #1, "OUTPUT 16#3; M3E"
210     N = 1
220     PRINT #1, "OUTPUT 16#3; B1E"
230     PRINT #1, "OUTPUT 16#7; PB0,CR"
240     PRINT #1, "OUTPUT 16#1; E"
250     FOR A = 1 TO 100
260     NEXT A
270     PRINT #1, "OUTPUT 16#3; W1E"
280     FOR B = 1 TO 2000
290     NEXT B
300     PRINT #1, "ENTER 17"
310     INPUT #2, A$, B$
320     PRINT #1, "OUTPUT 16#3; W7E"
330     PRINT "WAFER'S NAME :"; W$
340     PRINT "VOLT" TAB(10) "CAPACITANCE" TAB(24)
        "CONDUCTANCE" TAB(39) "RESISTANCE" TAB(52)
        "CORRECTED CAPACITANCE"
350     FOR M = S TO O STEP E
360     K = M / 100
370     PRINT #1, "OUTPUT 16#3; B1E"
380     PRINT #1, "OUTPUT 16#11; PB" + STR$(K) +", CR"
390     PRINT #1, "OUTPUT 16#1; E"
400     REM FOR A = 1 TO 100
410     REM NEXT A
420     PRINT #1, "OUTPUT 16#3; W1E"
430     REM FOR B = 1 TO 5000
440     REM NEXT B
450     PRINT #1, "ENTER 17"
460     INPUT #2, A$, B$
470     A$ = RIGHT$(A$,11)
480     B$ = RIGHT$(B$,11)
490     A(N) = VAL(A$)
500     B(N) = VAL(B$)
510     R(N) = B(N) / [(B(N)^2 + (2 x 3.141592 x 10^6)^2 x A(N)^2]
520     K(N) = [B(N)^2 + (2 x 3.141592 x 10^6)^2 x A(N)^2]
530     D(N) = K(N) x A(N)
540     E(N) = [B(N) - K(N) x R(N)]^2 + [2 x 3.141592 x 10^6 x A(N)]^2
550     C(N) = D(N) / E(N)
560     PRINT K TAB(9) A(N) TAB(23) B(N) TAB(38) R(N) TAB(51) C(N)
570     PRINT #1, "OUTPUT 16#3; W7E"
580     N= N + 1
```

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```
590     NEXT M
600     N = 1
610     INPUT "DO YOU WANT TO PRINT OUT (Y/N) :";C$
620     IF C$ =  "Y" OR C$ = "y" THEN 640 ELSE 630
630     IF C$ =  "N" OR C$ = "n" THEN 730 ELSE 610
640     INPUT "DO YOU TURN ON THE PRINTER (Y) :";C$
650     IF C$ =  "Y" OR C$ = "y" THEN 660 ELSE 640
660     LPRINT "WAFER'S  NAME :";W$
670     LPRINT "VOLT" TAB(10) "CAPACITANCE" TAB(24)
        "CONDUCTANCE" TAB(39) "RESISTANCE" TAB(52)
        "CORRECTED CAPACITANCE"
680     FOR M = S TO O STEP E
690     K = M / 100
700     LPRINT K TAB(9) A(N) TAB(23) B(N) TAB(38) R(N) TAB(51) C(N)
710     N = N + 1
720     NEXT M
730     N = 1
740     INPUT "DO YOU WANT TO STORE IT (Y/N) :";C$
750     IF C$ =  "Y" OR C$ = "y" THEN 770 ELSE 760
760     IF C$ =  "N" OR C$ = "n" THEN 970 ELSE 740
770     LINE INPUT "WHAT IS THE FILE NAME YOU WANT TO STORE
        :";F$
780     INPUT "HOW DO YOU WANT TO STORE DATA ? NORMAL (N)
        OR REVERSE (R) :",B$
790     IF B$ =  "N" OR B$ = "n" THEN 810 ELSE 800
800     IF B$ =  "R" OR B$ = "r" THEN 890 ELSE 780
810     OPEN "O", 3, F$
820     FOR M = S TO O STEP E
830     K = M / 100
840     PRINT #3, CHR$(9), K, CHR$(9), A(N), CHR$(9), B(N), CHR$(9),
        R(N), CHR$(9), C(N)
850     N = N + 1
860     NEXT M
870     CLOSE #3
880     GOTO 970
890     OPEN "O", 3, F$
900     N = INT(ABS(O-S) / ABS(E)) + 1
910     FOR M = O TO S STEP -E
920     K = M / 100
930     PRINT #3, CHR$(9), K, CHR$(9), A(N), CHR$(9), B(N), CHR$(9),
        R(N), CHR$(9), C(N)
940     N = N - 1
```

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```
950    NEXT M
960    CLOSE#3
970    INPUT "DO YOU WANT TO CALCULATE THE SURFACE
       POTENTIAL (Y/N) :", D$
980    IF D$ = "Y" OR B$ = "y" THEN 1020 ELSE 990
990    IF D$ = "N" OR B$ = "n" THEN 1000 ELSE 970
1000   PRINT "THAT'S IT, HAVE A NICE DAY"
1010   END
1020   INPUT "WHAT IS THE EQUILIBRIUM ELECTRON
       CONCENTRATIONS :", NP
1030   INPUT "WHAT IS THE EQUILIBRIUM HOLE CONCENTRATIONS
       :",PP
1040   INPUT "WHAT IS THE GATE AREA :",A
1050   REM INPUT "WHAT IS THE THICKNESS :", D
1060   REM CO = ES × A / D × 3.9 / 11.7
1070   ES = 11.7 × 8.854 × 10^-14
1080   RP = EXP[-2 × {0.0259 × LOG(PP / 1.5E+10)} × 38.61]
1090   N = 1
1100   FOR M=S TO O STEP E
1110   TEST = C(N) - CO
1120   IF TEST > 0 THEN 1130 ELSE 1140
1130   CO = C(N)
1140   N = N + 1
1150   NEXT M
1160   N = 1
1170   DEF FNF(A,B) = [EXP(-A) + A - 1] + B × [EXP(A) - A - 1]
1180   L = SQR [ES / (1.6 × 10^-19 × RP × 38.61)]
1190   PRINT TAB(10) "VOLT" TAB(31) "SURFACE POTENTIAL"
1200   CF = A × ES × 10^11 / L
1210   FOR M = S TO O STEP E
1220   K = M / 100
1230   IF CO = C(N) THEN 1440 ELSE 1240
1240   CT = C(N) × CO / [C0 - C(N)] × 10^11
1250   IF CT > CF THEN W = -0.4 ELSE W = 0.0001
1260   F W > 0 THEN H = 0.1 ELSE H = 40
1270   IF CT = CF THEN 1390 ELSE 1280
1280   IF W > O THEN 1350 ELSE 1290
1290   G = 1 - EXP(38.61 × W)
1300   J = 1 - EXP(-38.61 × W)
1310   WB = 38.61 × W
1320   IF FNF(WB,RP) < 0.0001 THEN 1370 ELSE 1330
1330   CS = A × ABS (ES × [J + RP × (-G)] / [1.414 × L ×
```

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```
         SQR{FNF(WB,RP)}])
1340     GOTO 1360
1350     CS = A × SQR (ES × 2 × 1.6 × 10^-19 × PP) / (2 × SQR (W + 0.0259
         × EXP (38.61 × W) × RP))
1360     IF ABS [(10^11 × CS - CT)] < H THEN 1420 ELSE 1370
1370     W = W + 0.0005
1380     IF W = 0 THEN 1370 ELSE 1410
1390     W(N) = 0
1400     GOTO 1430
1410     IF W > 0.8 THEN 1390 ELSE 1280
1420     W(N) = W
1430     PRINT TAB(10) K TAB(31) W(N)
1440     N = N + 1
1450     NEXT M
1460     N = 1
1470     INPUT
1470     INPUT "DO YOU WANT TO PRINT OUT (Y/N) :",A$
1480     IF A$ =  "Y" OR A$ = "y" THEN 1500 ELSE 1490
1490     IF A$ =  "N" OR A$ = "n" THEN 1580 ELSE 1470
1500     INPUT "DO YOU TURN ON THE PRINTER (Y) :",A$
1510     IF A$ =  "Y" OR A$="y" THEN 1520 ELSE 1500
1520     LPRINT TAB(10) "VOLT" TAB(31) "SURFACE POTENTIAL"
         TAB(52) "CORRECTED CAPACITANCE"
1530     FOR M = S TO O STEP E
1540     K = M / 100
1550     LPRINT TAB(10) K TAB(31) W(N) TAB(52) C(N)
1560     N = N + 1
1570     NEXT M
1580     N = 1
1590     INPUT "DO YOU WANT TO STORE IT (Y/N) :",A$
1600     IF A$ =  "Y" OR A$ = "y" THEN 1620 ELSE 1610
1610     IF A$ =  "N" OR A$ = "n" THEN 1000 ELSE 1590
1620     LINE INPUT "WHAT IS THE FILE NAME YOU WANT TO STORE
         :",F$
1630     INPUT "HOW DO YOU WANT TO STORE DATA ? NORMAL (N)
         OR REVERSE (R) :",B$
1640     IF B$ =  "N" OR B$ = "n" THEN 1660 ELSE 1650
1650     IF B$ =  "R" OR B$ = "r" THEN 1730 ELSE 1630
1660     OPEN "O", 3, F$
1670     FOR M = S TO O STEP E
1680     K = M / 100
1690     PRINT #3, CHR$(9), K, CHR$(9), W(N), CHR$(9), C(N)
```

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```
1700    N = N + 1
1710    NEXT M
1720    GOTO 1000
1730    OPEN "O", 3, F$
1740    N = INT(ABS(O - S) / ABS(E)) + 1
1750    FOR M = O TO S STEP -E
1760    K = M / 100
1770    PRINT #3, CHR$(9), K, CHR$(9), W(N), CHR$(9), C(N)
1780    N = N - 1
1790    NEXT M
1800    GOTO 1000
```

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APPENDIX C

LETTERS OF PERMISSION

Parts of this dissertation, particularly from Chapter 2 through Chapter 5, were published in the following four major refereed journals. With the written permission of the publishers, attached herein, the contents of each paper were reorganized.

1. Juho Song, G. S. Lee, and P. K. Ajmera, "Low temperature plasma enhanced chemical vapor deposition of silicon oxide films using disilane and nitrous oxide," *J. Electron. Mat.* **24**, 1507 (1995).

2. Juho Song, G. S. Lee, and P. K. Ajmera, "Chemical and electrical characteristics of low temperature plasma enhanced CVD silicon oxide films using Si_2H_6 and N_2O," *Thin Solid Films* **270**, 512 (1995).

3. Juho Song and G. S. Lee, "Structural properties of low temperature plasma enhanced chemical vapor deposited silicon oxide films using disilane and nitrous oxide," *Appl. Phys. Lett.* **67**, 2986 (1995).

4. Juho Song, P. K. Ajmera, and G. S. Lee, "Effects of native oxide removal from silicon substrate and annealing on SiO_2 films deposited at 120°C by plasma enhanced chemical deposition using disilane and nitrous oxide," *J. Vac. Sci. Technol. B* **14**, 727 (1996).

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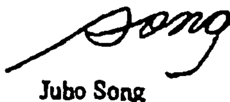

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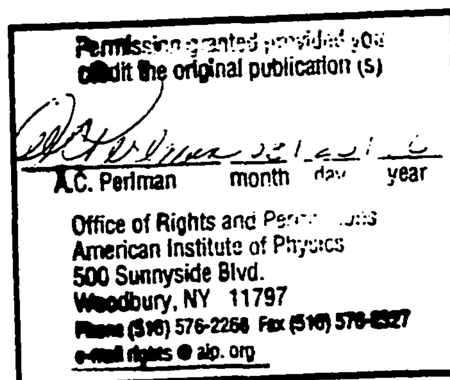

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VITA

Juho Song was born on February 25, 1963, in Taegu, Korea, where he graduated from Hae-An Elementary School in 1975, Cheong-Gu Middle School in 1978, and Sim-In High School in 1981. He earned his bachelor of science degree from the Kyungpook National University in 1985.

In late 1984 he joined R & D center at Samsung Electronics Co. in Korea, where he worked as semiconductor process engineer for 7 years in developing submicron CMOS process technology. For the first two years, he specialized in the area of photolithographic processes. He spent the next two years developing and integrating processes for the trench-based DRAM memory cell which was one of the hottest topics in the semiconductor industry. For the last three years at Samsung, he was one of the members that developed 16 Mega bit DRAM device integrated with 0.55 μm twin-well CMOS process technology. He also participated in setting up one of the best R & D clean rooms in the world.

In 1992, he came to the Louisiana State University to continue his graduate study. He earned his master of science in electrical engineering in 1994, and is now a candidate for a doctor of philosophy degree in electrical engineering. During his graduate work at Louisiana State University, he has developed low temperature film deposition processes for silicon oxide and fluorinated silicon oxide films in PECVD by the use of Si_2H_6 as silicon precursor for the first time in the history of CVD process. He has published four technical papers and submitted two more papers since 1995.

He was married in 1987 to Myungae Lim. They have two children, Youngmin who is a 7-year-old boy and Michelle who is a 2-year-old girl.

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Major Field: Electrical Engineering

Title of Dissertation: Low Temperature Silicon Oxide and Fluorinated Silicon Oxide Films Prepared by Plasma Enhanced Chemical Vapor Deposition Using Disilane as Silicon Precursor

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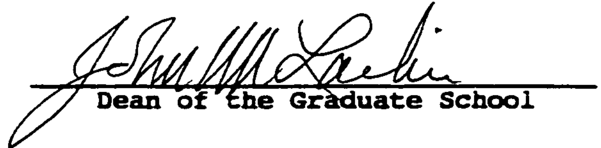

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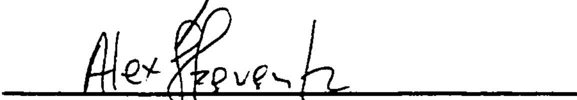

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