AIP | Applied Physics Letters

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Citation: Applied Physics Letters **104**, 083513 (2014); doi: 10.1063/1.4865583
View online: http://dx.doi.org/10.1063/1.4865583
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/104/8?ver=pdfcov
Published by the AIP Publishing

Low thermal resistance GaN-on-diamond transistors characterized by three-dimensional Raman thermography mapping

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(Received 28 November 2013; accepted 31 January 2014; published online 26 February 2014)

In order to achieve ultra-high radio frequency output power densities in GaN-based transistors new thermal management solutions must be developed for efficient heat extraction, including the use of high thermal conductivity substrates. Integration of GaN devices with the highest thermal conductivity material available, diamond, instead of the standard GaN-on-SiC, can lead to a substantial reduction in device thermal resistance. Current GaN-on-diamond transistors are shown to result in a 40% reduction in peak channel temperature when benchmarked against equivalent GaN-on-SiC transistors, with the potential for even further reductions through optimization. In order to understand the contribution of substrate and GaN/substrate interface to the device thermal resistance, a 3D Raman thermography mapping and modelling approach has been developed. The GaN/diamond interface thermal resistance is found to have the largest contribution to the thermal resistance of current GaN-on-diamond devices. © *2014 AIP Publishing LLC*.
[http://dx.doi.org/10.1063/1.4865583]

Great progress had been made in the field of high-frequency, high-power amplifiers in the past decade, enabled by the excellent electrical properties of AlGaN/GaN-based high electron mobility transistors (HEMTs): High operating voltage, operating frequency and radio frequency (RF) output power density.[1,2] Managing Joule self-heating at such high RF output power densities is currently one of the key challenges for further developing GaN-based RF devices, as these devices operate at much higher power densities than GaAs RF devices for example. Self-heating is detrimental to performance and reliability, especially considering the Arrhenius relationship between channel temperature and device mean time to failure (MTTF), whereby a small increase in operating temperature can lead to significant decrease in lifetime.[3] Therefore, power dissipation is typically de-rated to ensure long-term reliability. Improved thermal management will enable channel temperatures to be kept within a safe working limit and achieve the full output power density potential of GaN-based RF devices.

Contributions to the thermal resistance of AlGaN/GaN HEMTs arise in the heat path between the transistor channel and heat sink, including: GaN epilayer, substrate and ultimately die mounting and packaging.[4] The role of the substrate as a heat spreader is particularly important because of its close proximity to the 2DEG conduction channel at the AlGaN/GaN interface, where Joule self-heating occurs. Silicon carbide has a relatively high thermal conductivity (up to $\kappa_{SiC} \approx 420$–490 W/mK) when compared to alternative substrate materials used for GaN epitaxy, for example silicon ($\kappa_{Silicon} = 140$ W/mK). GaN-on-SiC devices are therefore currently the standard for high-power RF applications.[5,6] However, the thermal resistance of GaN-on-SiC devices is still a limiting factor when designing RF devices with high output power densities. While some improvement in GaN-on-SiC can be gained by optimizing thermal transport across the AlN nucleation layer at the GaN/SiC interface,[7,8] a far greater reduction in thermal resistance could be gained by replacing the substrate with the highest thermal conductivity material available, diamond ($\kappa_{Diamond}$ up to 2000 W/mK).[9]

Two methods exist for forming GaN-on-Diamond: Direct GaN-on-diamond epitaxy or transferring pre-grown GaN. Although encouraging transistor performance has been achieved by AlGaN/GaN HEMTs grown epitaxially on single crystal CVD diamond substrates,[9,10] this approach is currently uneconomical due to the unavailability of large single crystal diamond substrates. Alternatively, GaN layers originating from GaN-on-Si epitaxy can be integrated with polycrystalline diamond substrates after removing the silicon substrate by chemical etching. Polycrystalline diamond substrates can be grown in the larger diameters (>3 in.) required for commercially viable device fabrication, while still retaining much of the thermal conductivity improvement over SiC, in the range 800–2000 W/mK depending on the diamond growth conditions.[11] GaN layers can either be atomically attached to the diamond substrate by wafer bonding,[12] or the diamond can be grown on the bottom surface of the GaN after the silicon substrate is removed and following the deposition of a thin intermediate dielectric layer; the latter method is used in this work.

Although excellent electrical performance has been demonstrated for GaN HEMTs on polycrystalline diamond substrates,[13] experimental assessment of their thermal resistance has been limited. The thermal resistance of the GaN-on-diamond adhesion layer material has been measured using picosecond time domain thermoreflectance (TDTR), with values ranging from 1.7 to 4.2×10^{-8} m^{2}K/W, although the TDTR measurement is not sensitive to the underlying diamond at the GaN/diamond interface.[14] In order to assess the thermal performance of GaN-on-diamond, we use a measurement approach based on transistor self-heating for

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determining the thermal resistance contributions arising from both the diamond substrate and the GaN/diamond interface. This technique is based on 3-D Raman thermography mapping, including measured surface and depth temperature profiles in HEMT structures. The improvement in current GaN-on-diamond transistor thermal resistance is demonstrated by benchmarking against equivalent GaN-on-SiC transistors. An experimentally validated thermal model is used to explore the potential for further thermal resistance reduction in GaN-on-Diamond.

The measured GaN-on-Diamond devices originated from a 4 in.-diameter GaN-on-Si wafer consisting of a $\sim$1 μm-thick AlGaN transition layer, 1 μm-thick GaN buffer layer, and 20 nm AlGaN top barrier layer. The silicon substrate and AlGaN epitaxial transition layer, used to accommodate the lattice mismatch during GaN-on-Si growth, were removed to leave only the AlGaN/GaN layers. It is important that the low thermal conductivity $\sim$1 μm-thick AlGaN transition layer ($\kappa_{AlGaN} \approx 1/10\ \kappa_{GaN}$), is completely removed to avoid an additional thermal barrier between the GaN layer and diamond substrate.[14] Two wafers were measured: *Wafer A,* consisting of a 95 μm-thick hot-filament CVD diamond layer grown on the GaN back-side following the deposition of the 25 nm dielectric interlayer.; *Wafer B*, consisting of a 120 μm-thick microwave plasma CVD diamond layer grown following the deposition of a 50 nm dielectric interlayer. The appearance of diamond Wafers A and B was opaque and translucent, respectively. Ungated AlGaN/GaN HEMT structures, 100 μm-wide and with a contact spacing of 20 μm, were fabricated for on-wafer temperature measurements. In addition two finger 100 μm-wide transistors with a 34 μm gate pitch, 4 μm source drain opening, and 0.25 μm gate length were fabricated on Wafer A.

Raman thermography measurements were performed using a Renishaw inVia spectrometer, 488 nm A^+ laser and 50×0.6 numerical aperture objective lens, with a measured lateral spatial resolution of 0.5 μm. Raman thermography exploits the temperature induced phonon shift in a material, with respect to a reference phonon frequency measured at ambient temperature: More details about the technique can be found in Refs. 6–8, 15, and 16. To obtain the highest temperature accuracy, GaN temperatures were determined using the A_1(LO) phonon peak shift, which is relatively insensitive to stress.[15] The measured GaN temperature represents a volumetric average through the GaN layer. Diamond temperatures were measured using the degenerate 1332 cm^{-1} peak. Wafers were mounted on a thermoelectric vacuum chuck maintained at 25 °C; the chuck and sample position was controlled by a motorized XYZ translation stage with 0.1 μm step size resolution. Three dimensional finite element thermal models were constructed to accurately represent the measured device geometry, including temperature dependent thermal conductivities. A heat load 0.5 μm-long and 0.1 μm-deep was placed adjacent to the drain edge of the gate in the transistor model, whereas a uniform surface heater was placed between the contacts in the ungated transistor model.[7,8] An interfacial thermal resistance was introduced in the model between the GaN layer and diamond. The diamond substrate was modelled with a uniform and isotropic thermal conductivity.

In transparent materials, such as GaN-on-SiC, substrate thermal conductivity and GaN/substrate interface thermal resistance can be determined from temperature depth maps measured by confocal Raman thermography.[7] The temperature gradient inside opaque diamond cannot be measured directly. Instead, equivalent information can be obtained from the surface temperature profile, following the method developed here. High temperature accuracy can be obtained by mapping the highly uniform GaN layer, rather than the diamond which can exhibit local stress induced variations in phonon frequency due to the diamond polycrystallinity.[17] Figure 1 shows the GaN layer temperature profile measured across the surface of ungated HEMTs on Wafers A and B. Outside the active device channel, where there is no heat flow from the GaN into the substrate, the lateral temperature gradient in the GaN layer is in equilibrium with the underlying diamond and predominantly determined by the diamond substrate thermal conductivity. Inside the active region of the device, where power is dissipated, the GaN temperature depends not only on substrate thermal conductivity, but also the GaN/diamond interface thermal resistance and GaN layer thermal conductivity. This enables the unknown diamond

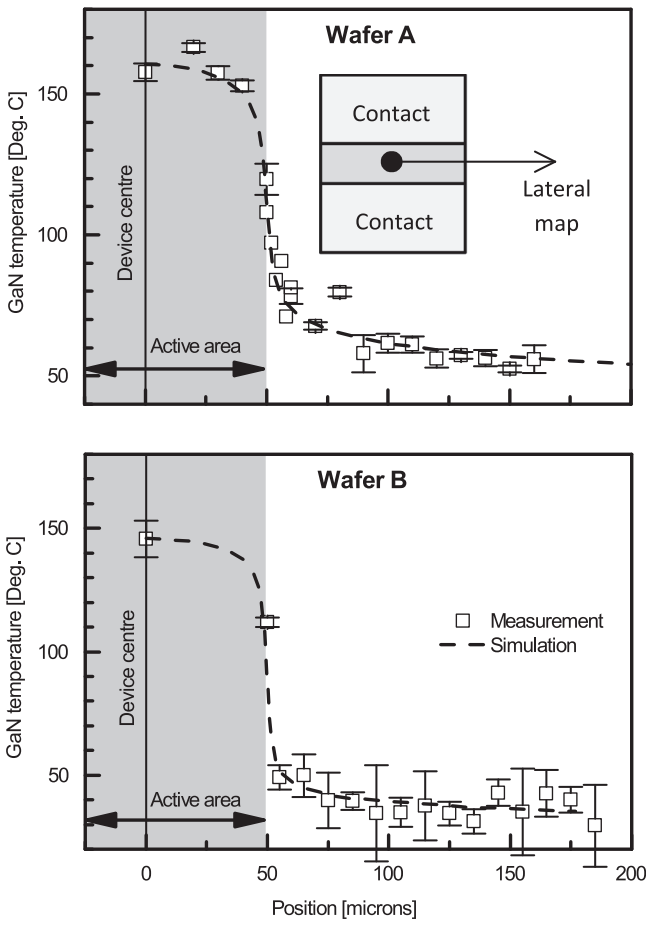

FIG. 1. Lateral GaN temperature profile measured for an ungated 100 μm-wide AlGaN/GaN-on-diamond transistor, with a contact spacing of 20 μm. A source drain bias of 40 V was applied resulting in a power dissipation of 3.36 W and 4.7 W for Wafer A and Wafer B, respectively. The mapped area is shown schematically as an inset plan view. Thermal modelling results are overlaid, including a diamond thermal conductivity of 710 W/mK and 1200 W/mK for Wafers A and B, respectively, and a GaN/diamond interfacial thermal resistance of 2.7×10^{-8} m^2K/W and 3.6×10^{-8} m^2K/W, for Wafers A and B, respectively.

thermal conductivity and GaN/diamond interface thermal resistance values to be obtained by adjusting these parameters iteratively in the thermal model to achieve the best fit over the whole measured surface temperature profile (Fig. 1). In our analysis, a temperature dependent GaN layer thermal conductivity of 160 W/mK ($T^{-1.4}$) was used, consistent with previous work.[6–8,15,16] Based on the analysis of two devices, a thermal conductivity of 710 ± 40 W/mK and GaN/diamond interfacial thermal resistance, of $2.7 \pm 0.3 \times 10^{-8}$ m^{2}K/W were obtained for wafer A, with opaque diamond and a 25 nm dielectric interlayer. AlGaN/GaN devices on the higher grade translucent GaN-on-Diamond wafer with 50 nm interlayer (Wafer B) were also measured, obtaining a diamond thermal conductivity of 1200 W/mK and a GaN/diamond interfacial thermal resistance of 3.6×10^{-8} m^{2}K/W.

In order to check the validity of this measurement approach, GaN and diamond temperatures were measured at the centre of the 100 μm wide ungated HEMT with 20 μm contact spacing on Wafer A (opaque diamond) and compared to the model result using the thermal conductivity values obtained in Fig. 1. The depth probed by the laser below the dielectric/diamond interface was estimated to be <1 μm by comparing the opaque diamond Raman scattering intensity depth profiles to that of silicon, i.e., the temperature discontinuity across the across the GaN/substrate interface is measured (shown schematically as an inset of Fig. 2). A similar approach has previously been used to study the interfacial thermal resistance between GaN and other opaque substrates, for example GaN-on-Si.[7] The sample position was maintained to within <0.2 μm during these measurements to avoid stress variations in the polycrystalline diamond substrate from influencing the diamond Raman temperature measurement. Figure 2 illustrates the good agreement between the model, using diamond and GaN/diamond interface parameters obtained in Fig. 1, and the measured GaN and diamond temperature rise. A similar measurement cannot be performed in the translucent diamond of Wafer B because of stress induced Raman shift variations measured through the wafer ($\sim\Delta 0.5$ cm^{-1}). Although based on the analysis of Wafer A we can have a high confidence in the validity of the thermal conductivity and interfacial thermal resistance values obtained through the surface temperature results shown in Fig. 1.

It is known that the thermal conductivity of polycrystalline diamond is influenced by crystal grain size which increases from its nucleation site;[18] In the case of GaN-on-diamond, close to the GaN interface. Therefore, the diamond thermal conductivity will increase with depth in the devices studied, with increasing grain size along the growth direction. In particular, the nano-crystalline diamond nucleation surface, within ~100 nm of the dielectric layer, will have a substantially lower thermal conductivity than bulk diamond;[19] the dielectric and this initial diamond nucleation layer are included in the GaN/diamond interfacial thermal boundary resistance in our model. The largest lateral and vertical substrate temperature gradient occurs within the first 20–30 μm of the edge of the active region in the ungated transistors (Figs. 1 and 2). The "effective" diamond substrate thermal conductivity probed in device self heating measurement is therefore weighted toward this region and will be

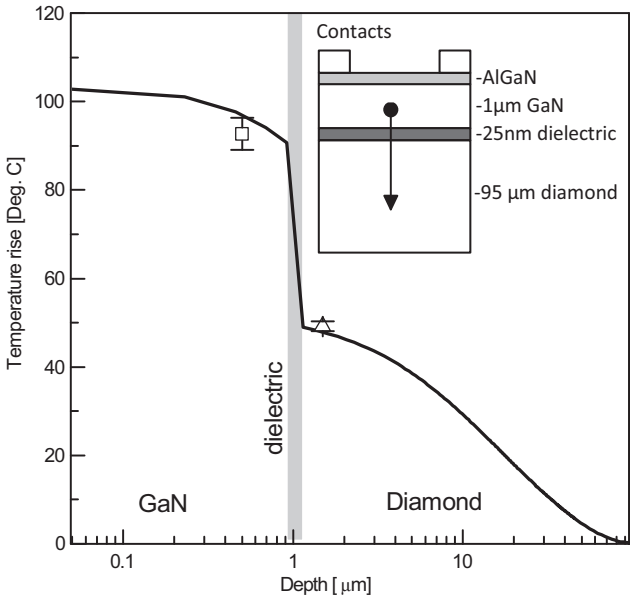

FIG. 2. GaN and diamond temperatures measured at the centre of a 100 μm-wide ungated AlGaN/GaN-on-diamond transistor with a contact spacing of 20 μm. A source drain bias of 40 V was applied, resulting in a power dissipation of 3.36 W. A schematic cross section of the device structure is shown as an inset. The simulated depth temperature profile is overlaid, using a diamond substrate thermal conductivity of 710 W/mK and a GaN/Diamond interfacial thermal resistance of 2.7×10^{-8} m^2 K/W.

lower than the thermal conductivities measured for bulk CVD diamond, in the range 800–1800 W/mK.[11] We note that the diamond thermal conductivity anisotropy, estimated to be 30% at a distance of 15 μm from the diamond nucleation surface,[18] cannot be distinguished from the average isotropic thermal conductivity used in this analysis. However, the effective diamond thermal conductivity obtained in these measurements is relevant for transistor thermal modelling and reproduces the lateral temperature profile and diamond temperature rise beneath the measured device, shown in Figs. 1 and 2, respectively.

Wafer B, with a thicker 50 nm dielectric interlayer has a 30% higher interfacial thermal resistance with respect to Wafer A, which has a 25 nm-thick dielectric layer. This does highlight that the dielectric layer is an important factor in determining the GaN/diamond interface thermal resistance. Assuming that only the dielectric layer contributes to the interfacial thermal resistance (neglecting any contribution from the diamond nucleation layer), we can estimate the thermal conductivity of the dielectric layer to be in the range 0.9–1.4 W/mK, based on the layer thicknesses. These thermal conductivities are close to the high temperature limit for amorphous dielectric materials.[20] In that case, the dielectric layer thermal resistance should scale linearly with thickness and should be minimized to reduce this contribution. However, the nanostructured diamond nucleation layer could have a thermal conductivity <10 W/mK,[21] and will also contribute to the total interfacial thermal resistance, which may account for the observed thermal resistance not being directly proportional to the dielectric interlayer thickness.

The $2.7 \pm 0.3 \times 10^{-8}$ m^{2}K/W interfacial thermal resistance value obtained for Wafer A, which includes the 25 nm-thick dielectric interlayer and diamond nucleation

layer, is comparable to typical values reported for GaN-on-SiC.[7,8] While even for Wafer A, consisting of an opaque diamond substrate, the effective substrate thermal conductivity is 50%–70% higher than SiC. Consequently, we anticipate that the GaN-on-diamond transistors on Wafer A will have a substantially lower thermal resistance than equivalent GaN-on-SiC transistors. To investigate this, temperature measurements have been performed on GaN-on-diamond and GaN-on-SiC HEMTs with an identical layout. The measured GaN-on-SiC wafer consists of a 1.8 μm-thick GaN layer and 100 μm-thick SiC substrate. The Raman measured temperature of the GaN-on-diamond transistor is 25% lower than the GaN-on-SiC device at a power dissipation of 15 W/mm, shown in Fig. 3. Raman thermography measures a volumetric average through the GaN layer thickness, which is lower than the peak channel temperature. In order to make a direct comparison, peak channel temperatures were extrapolated from the measured temperatures with the aid of thermal simulations, taking into account the different thicknesses of the GaN layer in the GaN-on-diamond (1 μm-thick) and GaN-on-SiC (1.8 μm-thick) AlGaN/GaN HEMT devices, originating from the different GaN-on-silicon and GaN-on-SiC growth processes. The GaN-on-SiC thermal model included a best case scenario SiC substrate thermal conductivity of 490 W/mK ($T^{-1.5}$) and a GaN/SiC interfacial thermal resistance of 1.7×10^{-8} m^2K/W, obtained from previous measurements. The thermal resistance of the GaN-on-diamond transistor was found to be 40% lower than the reference SiC transistor, based on peak channel temperatures shown in Fig. 3 at a 15 W/mm power dissipation, corresponding to a channel thermal resistance of 10 K mm/W.

A transistor thermal model can be used to investigate the potential for even further thermal resistance reductions in GaN-on-diamond: By assessing the contribution of diamond thermal conductivity and GaN/diamond interfacial thermal resistance to the total device thermal resistance. Figure 4 shows the GaN and diamond temperatures measured for a transistor on Wafer A, compared with the temperature depth profile generated by the thermal model using the substrate thermal conductivity and GaN/substrate interfacial thermal resistance obtained from the analysis shown in Fig. 1. The agreement observed between simulation and measurement gives confidence in the validity of the model and thermal material parameters used. The thermal resistance contribution of GaN layer, GaN/diamond interface, and diamond substrate can be obtained from the relative temperature rise across each layer temperature in the depth profile shown in Fig. 4: ~45% and ~20% for the GaN/diamond interface and diamond substrate, respectively. Therefore, most benefit in the current technology can be gained by reducing the thermal resistance between the GaN and diamond, rather than improving the diamond thermal conductivity. This could be achieved by decreasing the dielectric thickness and optimising the dielectric and diamond nucleation layer. To illustrate this, the GaN/diamond interfacial thermal resistance was removed in the model resulting in a ~40% reduction in the peak transistor temperature, illustrated in Fig. 4. Doubling the substrate diamond thermal conductivity to 1400 W/mK, without changing the GaN/diamond interfacial thermal resistance, resulted in a more modest 12% reduction in the peak transistor temperature (Fig. 4); this highlights the importance of efficiently transporting heat from the GaN layer into the substrate in order to take the fullest advantage of high thermal

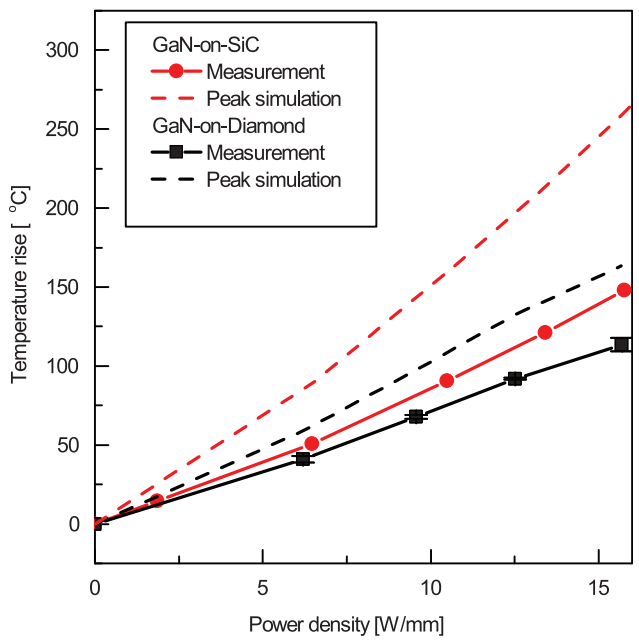

FIG. 3. Raman measured GaN temperature in AlGaN/GaN HEMTs on the drain side at a lateral distance of 0.5 μm from the T-gate cap edge, for transistors on a GaN-on-diamond wafer and a reference GaN-on-SiC wafer. Both devices measured share the same geometry: two fingers, 100 μm-wide and 34 μm gate pitch. Peak channel temperatures were extrapolated from the measured temperatures with the aid of a thermal model.

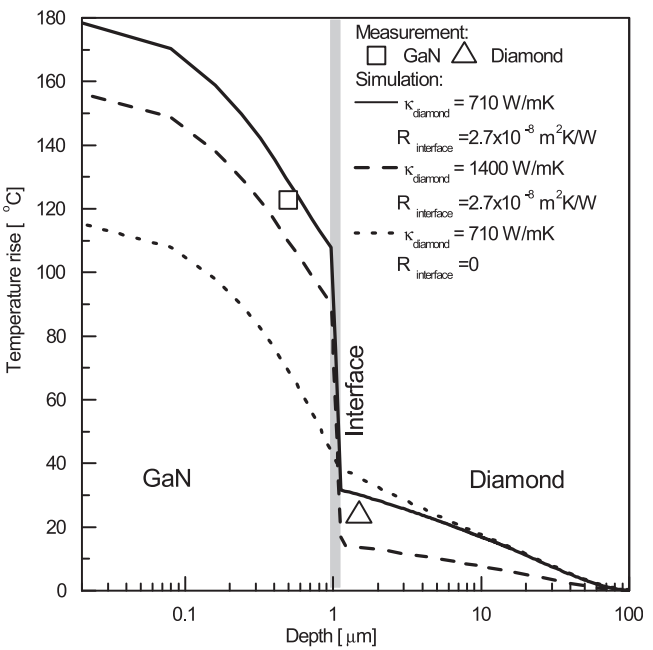

FIG. 4. GaN and diamond temperatures measured by Raman thermography on the drain side at a lateral distance of 0.5 μm from T-gate cap edge in a two finger GaN-on-diamond transistor. The simulated depth temperature profile is overlaid, using the parameters determined by measurements on ungated transistors on an opaque GaN-on-diamond wafer (Wafer A). For comparison, the temperature profiles simulated for an increased substrate thermal conductivity ($\kappa_{diamond} = 1400$ W/mK) and decreased GaN/diamond interfacial thermal resistance ($R_{interface} = 0$) are overlaid.

conductivity diamond. We note that once a low thermal resistance GaN/diamond interface and high thermal conductivity substrate are achieved, the thermal resistance of the GaN layer itself becomes the dominant factor in determining the transistor thermal resistance. The thermal resistance of the GaN layer could be improved by reducing the thickness below the current 1 μm value, bringing the diamond substrate as close as possible to the transistor channel.

In conclusion, the integration of GaN-based high-power transistors with high thermal conductivity substrates enables a significant reduction in transistor thermal resistance: The thermal resistance of a state-of-the-art GaN-on-diamond transistor is 40% lower than an identical GaN-on-SiC device, with the potential for even further reductions through optimisation. The role of diamond substrate thermal conductivity and GaN/diamond interfacial thermal resistance in determining the thermal resistance of GaN-on-diamond devices was assessed by using a combination of Raman thermography measurements and thermal modelling. Based on the analysis of lateral and depth temperature profiles, an effective substrate thermal conductivity of 710 W/mK and 1200 W/mK was obtained for an opaque and a translucent polycrystalline diamond wafer, respectively. The minimum GaN/substrate interfacial thermal resistance determined here was $2.7 \pm 0.3 \times 10^{-8}\,\mathrm{m^2K/W}$, which includes contributions from the dielectric layer and the diamond nucleation layer, and has a three times greater contribution to the total device thermal resistance than the substrate for the device geometry measured here.

We thank F. Ejeckam and D. Francis (Element6 Technologies, formerly at Group4 Labs, Inc.) for their contribution to this work. This work was supported by the DARPA Near Junction Thermal Transport (NJTT) Program, monitored by Dr. Avram Bar Cohen and supported by Dr. Joseph Maurer and Dr. Jonathan Felbinger. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the authors and do not necessarily reflect the views of DARPA.

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