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Low-voltage bulk-driven flipped voltage follower-based transconductance amplifier

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ABSTRACT

A low voltage high performance design of operational transconductance amplifier is proposed in this paper. The proposed architecture is based on bulk driven quasi-floating gate metal oxide semiconductor field effect transistor (MOSFET) which supports low voltage operation and improves the gain of the amplifier. Besides to this the tail current source requirement of operational transconductance amplifier (OTA) is removed by using the flipped voltage follower structure at the input pair along with bulk driven quasi-floating gate MOSFET. The proposed operational transconductance amplifier shows a five-fold increase in direct current (DC) gain and 3-fold increase in unity gain bandwidth when compared with its conventional bulk driven architecture. The metal oxide semiconductor (MOS) model used for amplifier design is of 0.18 um complementary metal oxide semiconductor (CMOS) technology at supply of ± 0.5 V.

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1. INTRODUCTION

With technology shrinkage low voltage operation has been a continuous motivation but it has forced challenges to analog designers to produce circuits with satisfactory performance. The metal oxide semiconductor field effect transistor (MOSFET) threshold voltage limits the supply scaling. However, a number of solutions is reported in literature to encounter this issue at the cost of either cost else degradation of some parameters. So, depending on the user requirement the choice of techniques is done. Few well known frequently adopted techniques are bulk driven technique [1]–[3], floating gate (FG) structure [4], quasi-floating gate (QFG) structure [5]–[7] and bulk driven floating/quasi-floating gate (BDFG/BDQFG) structure [8], [9]. Among stated approach the BDQFG has found potential use when linearity is not a prime objective. Basically, this approach is operating bulk driven MOSFET in a quasi-floating state and so it improves the alternating current (AC) features of bulk driven MOSFET. Like if any bulk driven transconductance amplifier is to be designed then the low transconductance limits its gain and bandwidth. So, BDQFG is one of such method as the effective transconductance is the sum of transconductance of BD and scaled transconductance of QFG MOSFET. The improved transconductance results in high gain circuits and also in improved gain-bandwidth product. Another example can be taken is of current mirror circuit where transconductance decides the basic performance parameters such as bandwidth, input, and output resistances [10], [11].

In this paper, a BDQFG based three current mirror topologies operational transconductance amplifier (OTA) is proposed. The OTA is a voltage controlled current source device having wide application

similar to like operation amplifier. For improvement of OTA parameters along with BDQFG, the proposed OTA use flipped voltage follower (FVF) structure at the input. The FVF is widely adopted for realization of low voltage circuits [12]–[16]. The use of FVF helps in improving the linearity of amplifier and also removal of tail current source used to bias OTA.

The paper is divided in five sections. Following the introduction made on section 1, section 2 details about the conventional BD current mirror OTA followed to proposed high gain improved linearity current mirror OTA in section 3. The simulation results are discussed in section 4 and conclusion in section 5.

2. DESIGN METHODOLOGY

The three current mirror-based OTA [17] using BD technique is shown in Figure 1. The current mirror topologies are (M3, M5), (M4, M6), and (M7, M8). The OTA is biased using constant current source I_{bias}, also referred as tail current source in literature. Analysing OTA the transconductance is given by:

$$V_{id} = V_{in+} - V_{in-} \tag{1}$$

$$V_{id} = V_{GS1} - V_{GS2} = \sqrt{\frac{I_1}{\beta_n}} - \sqrt{\frac{I_2}{\beta_n}} \tag{2}$$

Where $\beta_n = \mu_n C_{ox} \left(\frac{W}{L}\right)_{1,2}$

The M1 & M2 currents is given by:

$$I_1 = \frac{I_{bias}}{2} + \frac{1}{2}\sqrt{\beta_n I_{bias}} V_{id} \sqrt{\left(1 - \frac{\beta_n V_{id}^2}{4I_{bias}}\right)} \tag{3}$$

$$I_2 = \frac{I_{bias}}{2} - \frac{1}{2}\sqrt{\beta_n I_{bias}} V_{id} \sqrt{\left(1 - \frac{\beta_n V_{id}^2}{4I_{bias}}\right)} \tag{4}$$

Since

$$I_{out} = I_1 - I_2 \tag{5}$$

From (3) and (4):

$$I_{out} \approx \sqrt{\beta_n I_{bias}} V_{id} \tag{6}$$

The effective transconductance of OTA:

$$G_m = \frac{\partial I_{out}}{\partial V_{id}} \tag{7}$$

$$G_m \approx \eta \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right)_{1,2} I_{bias}} \tag{8}$$

Where $\eta = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}}$ and output conductance is given by:

$$g_{out} = g_{ds6} + g_{ds8} = \frac{I_{bias}}{2}(\lambda_n + \lambda_p) \tag{9}$$

Combining (1) and (2) yields the DC gain of the amplifier which is given by:

$$A_V = \frac{G_m}{g_{out}} = 2\eta \sqrt{\frac{\mu_n C_{ox}}{I_{bias}} \left(\frac{W}{L}\right)_2} \left(\frac{1}{\lambda_n + \lambda_p}\right) \tag{10}$$

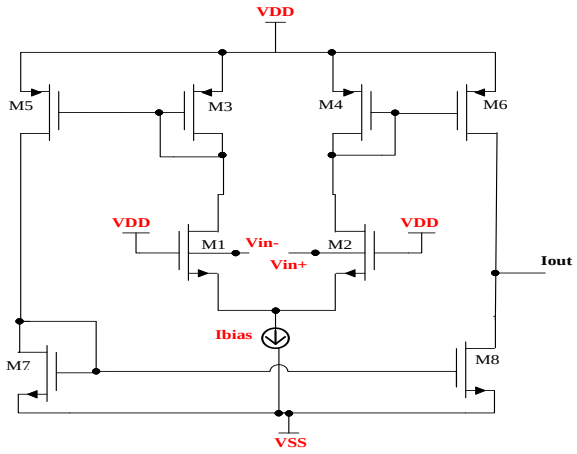

Figure 1. Bulk driven operational transconductance amplifier

As observed from (8) and (10), the effective transconductance is basically the transconductance of input MOSFET. Since bulk driven MOSFET has low transconductance, this puts a limit on the DC gain of the amplifier. The limited transconductance also affects the unity gain bandwidth (UGB) of the amplifier which is given as:

$$UGB = \frac{G_m}{C_L} = \frac{\left(\eta\sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_2 I_{bias}}\right)}{C_L} \tag{11}$$

So, it can be stated that transconductance boosting of input MOSFET will improve the performance of OTA in terms of gain as well the bandwidth. Such improvement can be easily achieved by replacing BD with BDQFG MOSFET which increases the DC gain as well the UGB of the OTA.

3. PROPOSED DESIGN

The performance improvement can be carried in two forms: either at MOSFET structure level like using BDQFG approach otherwise at circuit level like recycling folded cascode and local common mode feedback. The recycling folded cascode OTA [18] is based on concept of use of adaptive biasing at the input differential pair which improves the dynamic current range. However, the additional circuitry required brings out the chances of area and extra power requirements. In the proposed work, the BDQFG approach has been adopted to improve the DC gain through boosted transconductance. The proposed OTA is shown in Figure 2. As it can be seen the input MOSFETs M1 and M2 is configured as BDQFG MOSFETs. The MOSFET M1 and M2 is configured in QFG with the help of capacitor C1 and C2 along with cut-off region MOSFETs MP1 and Mp2 respectively. The boosted transconductance is given as:

$$G_{m,BDQFG} = (\eta + k)\sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_2 I_{bias}} \tag{12}$$

where k is the ratio of input to total associated parasitic capacitances. This increase the DC gain as well the UGB of the OTA. It also improves the transient response as the magnitude of current through input MOSFETs increases. Though response can be also improved by increasing the value of I_{bias} but this approach leads to increased power dissipation. To overcome this flipped voltage follower is used along with BDQFG MOSFET. This increases the magnitude of total current flowing through M1 and M2. In the proposed OTA, the pair (M1, M1a) and (M2, M2a) forms a FVF structure to process input signal. Due to FVF the tail current source, a power-hungry unit of OTA is no more required due to presence of M1a and M2a. The circuit becomes self-biased. The pair (M1, M1a) and (M2, M2a) forms a FVF structure to process input signal of bulk. Also, a source degenerated resistor 'R' is used which provides negative feedback [19]. As the input section is a source follower, the input voltages of M1 and M2 is replicated to source terminals where voltage-to-current conversion is carried through R. The overall DC gain and bandwidth increases without need of any external bias current source. Analyzing the OTA:

$$I_{out} \approx \sqrt{\beta_n I_{bias}}\,(V_{id} - RI_{out}) \tag{13}$$

$$G_m = \frac{\partial I_{out}}{\partial V_{id}} \approx \frac{g_m}{1+g_m R} \quad (14)$$

Where $g_m = \sqrt{\beta_n I_{bias}}$ is the transconductance of MOSFET M1 and M2. So, using source degeneration technique [20], [21] the input dynamic range is easily improved at low supply.

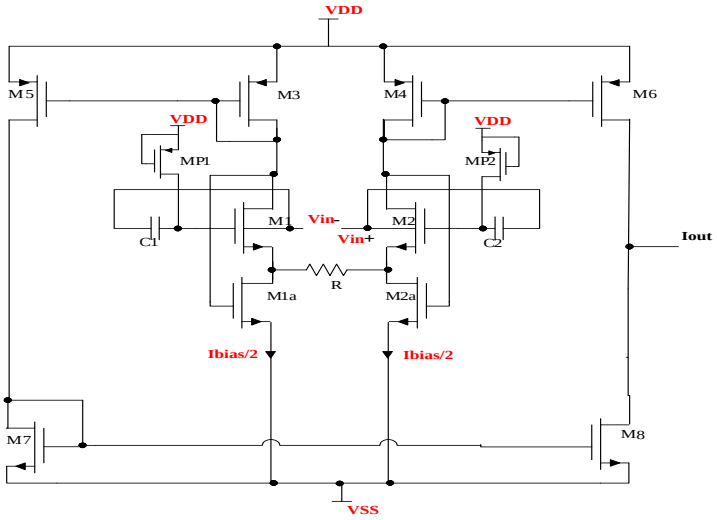

Figure 2. Proposed BDQFG FVF OTA

4. RESULTS AND DISCUSSION

The conventional and proposed OTA are simulated on 0.18 µm CMOS process at ± 0.5 V supply using spice simulator. The device dimensions are shown in Table 1 along with other assumed parameters for circuit simulations. The transconductance plots of OTAs is shown in Figure 3 where it can be observed that BD OTA offers poor transconductance of 14.9 µA/V whereas when OTA it is modified using BDQFG as a part of FVF, the effective transconductance gets boosted to a value 92.9 µA/V. The transconductance directly affects the DC gain as well the unity gain frequency for which the plot is shown in Figure 4.

Table 1. W and L of MOSFETs

Transistors	Width (µm)	Length (µm)	Transistors	Width (µm)	Length (µm)
M1, M1a	15	1.2	M6	15	2.0
M2, M2a	15	1.2	M7	15	1.2
M3	25	0.8	M8	15	1.2
M4	25	2.0	MP1	0.36	0.36
M5	15	0.8	MP2	0.36	0.36
R=100 Ω, C1=C2=C3=1 pf, CL=0.1 pf, supply=±0.5 V, I bias=10 µA					

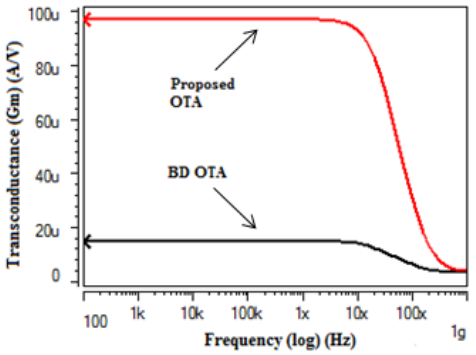

Figure 3. Transconductance plots

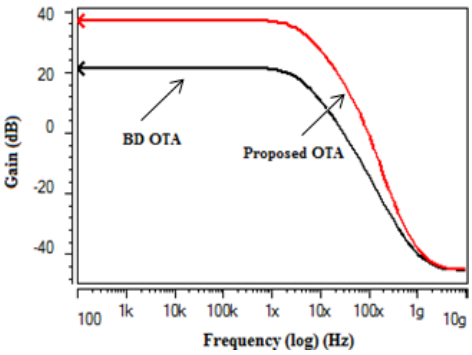

Figure 4. Gain plots

As can be seen in Figure 4, the DC gain of BD OTA is boosted from 21.5 dB to 37.1 dB by incorporating BDQFG FVF. The unity gain frequency also increases accordingly. For BD OTA, the UGB value is 29.7 MHz whereas for proposed OTA it is 95.3 MHz.

The transient response is shown in Figure 5 where the BD shows a degraded characteristic. This gets improve by BDQFG due to increase of I_{bias} and the best response with minimum offset is seen for proposed OTA due to linearization technique used. So, a low voltage high gain, large bandwidth and fast OTA can be achieved with proposed approach without any significant contribution in terms of power. The performance analysis of OTAs as obtained by simulations is summarized in Table 2.

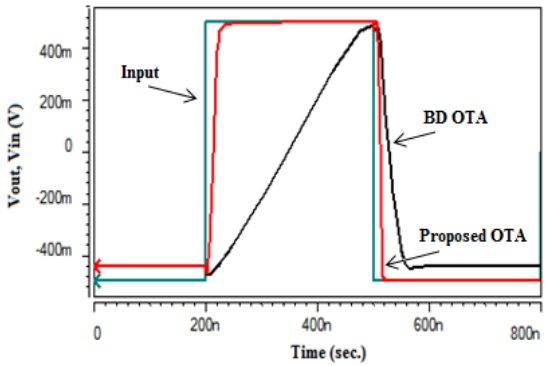

Figure 5. Transient plots

Table 2. Performance analysis of OTAs

Parameters	[17]	[19]	[22]	[23]	[24]	[25]	OTA (Figure 1)	Proposed FVF OTA (Figure 2)
Driving method	GD	BDQFG	BD	BD	BD	BD	BD	BDQFG
Transconductance (Gm) (uA/V)	0.076	67.88	----	----	----	----	14.9	92.9
DC gain (dB)	45.3	21.09	78	64.7	70	65.8	21.5	37.1
-3 db frequency (MHz)	----	----	---	----	---	---	3.1	3.5
GB (MHz)	0.065	----	7.5	2.96	9.5	2.78	29.7	95.3
PM	----	86	59	52	88	61	91	67
FOM ((KHz*pF)/nA)	----	----	1.23	2.11	1.37	1.08	1.007	3.37
Power (uW)	----	----	----	----	----	----	23.79	25.14
Supply (±)	0.5 V	0.5 V	0.5	0.3	0.25	0.3	0.5 V	0.5 V
Technology (nm)	90	180	180	180	65	180	180	180

5. CONCLUSION

A low voltage high gain OTA has been presented. The approach followed includes hybrid form of bulk driven technique which is BDQFG along with FVF structure. The BDQFG improves the AC characteristics and being a cpacitive network it does not affect the DC power while FVF helped in removal of tail current source from the OTA. The achieved performance encourages it application for high performance high speed VLSI circuits.

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