

Book Review:

Low-Voltage CMOS VLSI Circuits

James B. Kuo and Jea-Hong Lou

Wiley-Interscience, NY, 1999, 439 pp., ISBN 0-471-32105-2

Reviewer: Kim, Kyungseok

In these days, there are many digital products, which are implemented by CMOS VLSI technology, in the market. Currently, CMOS VLSI is progressing at fast rate for decades and dominating most of markets in digital circuit areas. In a constant voltage scaling, the vertical and later electric fields are increased, which reduced to oxide reliability. Low power supply voltage is required necessarily. For the design of CMOS VLSI systems using low power supply voltage, the implementation of chips is directly limited by processing technology and devices. The objective of this book is to demonstrate the useful techniques in the designing of logic level and system building blocks in low-voltage CMOS VLSI technology.

The book is composed of six chapters with introducing briefly the evolution of the low-voltage CMOS VLSI systems in first chapter. In chapter 2, the trend of CMOS technology and devices related to low-power subjects are described from 1.8V 0.25 μm to 0.1 μm . For deep submicron CMOS devices, it is useful to mention shallow trench isolation (STI) to increase device density, lightly-doped drain (LDD) structure to reduce the hot carrier effects causing aging and avalanche breakdown under the high electric field, and a buried channel to maximize the current driving capability with the enhance-mode CMOS device. Another device technology of BiCMOS and SOI (silicon-on insulator) is reviewed. The modeling of CMOS device behaviors are analyzed with the equations including threshold voltage, body effect, short channel effect, narrow channel effect, electron temperature effect, hot carrier effect and capacitance model. Finally, the BSIM SPICE models are summarized for deep-submicron CMOS transistor.

Chapter 3 describes the evolution of innovative static logic circuits starting from the voltage transfer characteristic of a CMOS inverter as a basic circuit. The power dissipation of the CMOS inverter is linearly proportional to its operating frequency, which is caused by switch activities. Next, CMOS architectures for differential logic circuits and pass transistor logics are introduced. Three types of the differential static logic circuits, the differential cascade voltage switch (DCVS), the differential split-level (DSL) logic circuits and the differential cascade voltage switch with pass-gate (DCVSPG) logic circuits, are described, followed by push-pull cascade logic (PPCL) circuits. CMOS pass-transistor logic circuits, BiCMOS static

logic circuit, and SOI CMOS static are also introduced. The later parts in this chapter give very useful techniques for low-voltage CMOS static logic circuits mentioning bootstrapped CMOS driver, multi-threshold standby/active techniques, and for low-power CMOS circuits by reduction of dynamic power dissipation using the bus architecture approach and the adiabatic logic.

In chapter 4, the authors present CMOS dynamic logic circuits from the basic techniques to the logic families including NORA, Zipper, domino, latched domino, multiple output domino, skew-tolerant domino, and true-single-phase clocking (TSPC) dynamic logic. Compared to CMOS static logic circuits, CMOS dynamic logic circuit is more precise than the static CMOS logic circuit and usually controlled by two-phase clock signals. The BiCMOS dynamic logic circuits and the techniques to decrease the effect of charge sharing problem are mentioned. In final portion of the chapter, CMOS dynamic logic circuit techniques are presented for low-voltage by analyzing bootstrapped dynamic logic (BDL) circuits, bootstrapped all-N-logic TSPC dynamic logic circuits, and semi-static DCVSPG-domino logic circuits.

Chapter 5 is focus on the memory architecture and the analysis of characteristics in different kinds of memory structures. SRAM memory is used as an embedded cache, while DRAM memory as a data storage. The key parameter of SRAM is speed, compared with DRAM of which the size and cost is the key parameter. Data of volatile memories like SRAM and DRAM is lost when the power supply is turned off. But, Non-volatile memories keep data without the power supply including ROM (read only memory), PROM (program ROM), EPROM (erasable PROM), EEPROM (electrically EPROM), flash, and FRAM (ferroelectric RAM). The trade-offs with respect to power, speed, and chip area in memory architectures are explained with low-voltage circuit techniques. In addition, BiCMOS SRAM and DRAM are analyzed. The chapter includes the recent SOI CMOS technology used to integrate SRAM and DRAM.

Finally, the last chapter is first concerned with the implementation of the fundamental basic building blocks for VLSI systems such as adder and multiplier circuits. Then, the basic circuit techniques are demonstrated in register files, cache memory, programmable logic arrays (PLA), and phase-locked loop (PLL). The fundamental structures such as floating-point unit (FPU), central processing unit (CPU), and digital signal processor (DSP) are examined, followed by the circuit techniques for BiCMOS and SOI systems.

The book completely covers from low-voltage CMOS technology and devices to low-voltage CMOS static and dynamic logic circuits, then goes through low-voltage CMOS memory circuits and CMOS VLSI systems hierarchically. It presents in detail on the transistor level with simulation and the semiconductor processes, followed by various circuit techniques for the same function with respect to performance and reliability. Even though the book didn't include whole subjects related to low-voltage and low-power techniques, this book is valuable for senior undergraduates and first-year graduates interested in CMOS circuit designs. The technology in CMOS is advancing at very fast rates every year. The fundamental knowledge of technology is usually not changed, but the reader needs to keep referring the articles of journals and conference papers for the trends in detail.