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Low-Voltage, Full-Swing InGaZnO-Based Inverters Enabled by Solution-Processed, Ultra-Thin Al_xO_y

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***Abstract*—High-performance, full-swing inverters implemented with InGaZnO thin-film transistors (TFTs) have been demonstrated capable of operating at a very low voltage. The threshold voltage of the load and drive TFTs were modified through careful change of the gate dielectric anodization voltage. Both the load and drive TFTs show excellent electrical properties including a current on/off ratio > 10^6 and a subthreshold swing close to the theoretical limit. As a result, the inverters show high voltage gains up to 34 at a supply voltage of only 1 V as well as high noise margins > 92% of the theoretical maximum. The devices and the fabrication process might have potential applications in future wearable and disposable electronics where low cost and low power are vital.**

***Index Terms*—full-swing inverters, InGaZnO, one-volt operation, high voltage gain and noise margins**

I. Introduction

OXIDE-SEMICONDUCTOR-BASED thin-film transistors (TFTs) have been shown to be one of most promising candidates for large-area, wearable, and disposable electronics [1, 2]. InGaZnO (IGZO) in particular, has been regarded as an emerging material for active-matrix backplane technology due to its high electron mobility and excellent uniformity over large areas [1]. For battery powered portable electronics, such as wearable devices, low operating voltage and low power consumption are crucial due to the limited lifespan of batteries [3]. For a circuit to operate at an ultralow voltage, i.e., within 1 V, it requires all the integrated components to operate at such a voltage. However, it is still challenging to achieve oxide TFTs with both an ultralow operating voltage and excellent electrical performances at the same time. Hence, to date, the supply voltages of the reported oxide-TFT-based circuits are generally ≥ 5 V [4-7].

Due to the difficulties in accomplishing high performance *p*-type operation in oxide TFTs, especially under an ultralow operating voltage, most oxide-TFT-based logic circuits have been implemented with only *n*-type oxide TFTs. Two types of inverters can be designed based on *n*-type TFTs, i.e., enhancement-mode load and depletion-mode load inverters. Depletion-mode load inverters are preferable owing to their higher voltage gain and larger output voltage swing than enhancement-mode ones [8]. To realize an IGZO-based depletion-mode inverter, TFTs with different threshold voltages are required. Several techniques can be used to achieve different threshold voltages for two TFTs in one inverter, such as by varying the channel thickness [9], and by treating the top surface with different methods [7, 10]. However, increase of channel layer thickness may result in worsening of subthreshold swing, and different treatments for the top surface might complicate the deposition and potentially damage the channel layer underneath.

The threshold voltage difference can also be created using gate dielectrics with different thicknesses for the load and drive TFTs. However, this typically requires vacuum-based methods, such as sputtering and atomic-layer deposition (ALD), including a break of vacuum and an additional step of patterning, which are not cost-friendly and inefficient. Alternatively, one can use anodization, which is a solution-processed, vacuum-free method that can deposit conformal, reliable, ultra-thin oxide layers at room temperature in a very short time [11]. Recently, one-volt IGZO TFTs have been demonstrated by us using anodized, ultra-thin Al_xO_y as gate dielectrics [11, 12]. With our anodization method, the thickness of the gate oxide layers can be easily controlled by varying the anodization voltage on the same substrate, enabling the creation of inverters based on solution-processing.

Unlike our previous publications on individual TFTs, in this letter, we report full-swing amorphous IGZO (a-IGZO)-based inverters that are capable of operating at low voltages (1 and 0.8 V). Different threshold voltages for the load and drive TFTs were achieved through the modification of anodization

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voltages on the same substrate. The excellent electrical properties of both the load and drive TFTs ensure a voltage gain up to 34 at a supply voltage of 1 V with very high noise margins. Such a simple and time efficient method might have potential applications in future low-cost, low-power electronic applications.

II. Experimental Procedures

Figs. 1(a) and (b) show schematic diagrams of an IGZO inverter circuit. First, a 200 nm thick layer of Al was thermally evaporated onto a glass substrate through a shadow mask as the gate electrode. Then, the Al gate lines were immersed into a 1 mM citric acid solution to be anodized at 2.3 V, followed by rinsing with IPA and careful drying using a N_2 jet. After that, the gate lines on the bottom half of the substrate were re-immersed into the same solution to be anodized at 3.84 V, followed by the same drying process. With an anodization ratio of 1.3 nm/V for Al [13], approximately 3 and 5 nm thick Al_xO_y films were formed on the top and bottom halves of the substrate respectively. The gate lines were then wet etched to break the connection between top and bottom sections.

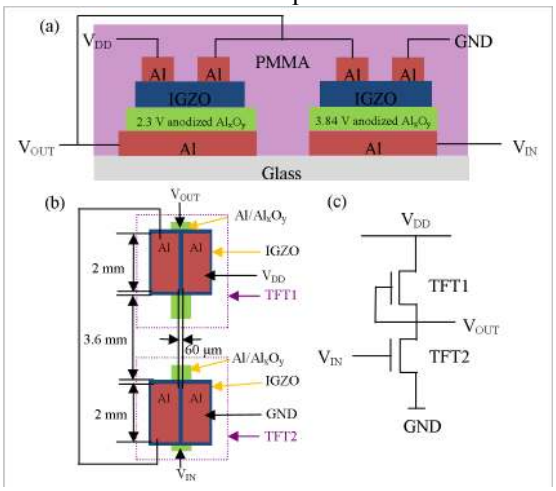

Fig. 1. Schematic diagrams of (a) cross-sectional and (b) top-view of an IGZO inverter on a glass substrate. (c) Schematic circuit diagram of the inverter. The anodization voltages of the Al_xO_y in TFT1 and TFT2 are 2.3 and 3.84 V, respectively.

To fabricate the TFTs, a 30 nm thick a-IGZO layer was sputtered on top of the Al_xO_y using RF magnetron sputtering with a power of 50 W in a pure argon atmosphere followed by thermal evaporation of 200 nm thick Al source/drain electrodes. Both layers were patterned using shadow masks, and the channel width and length were 2 mm and 60 μm, respectively. A distance of 3.6 mm was kept between the top and bottom transistors. Finally, a 200 nm thick PMMA layer was spin-coated and baked in N_2 at 90 ˚C for 30 minutes to form the top encapsulation layer. The electrical performance of the devices was measured in dark at room temperature using an Agilent E5270B semiconductor analyzer and an Agilent E4980A LCR meter. The inverters were measured by connecting the drive and load TFTs externally. The schematic circuit diagram of the inverter is shown in Fig. 1(c).

III. Results and Discussions

The gate capacitances of the 2.3 and 3.84 V anodized Al_xO_y were measured using an Al/anodized Al_xO_y/Al structure and found to be ~ 1000 and ~ 775 nF/cm^2, respectively.

Figs. 2(a) and (b) show the output characteristics of the IGZO TFTs gated with 2.3 V (TFT1) and 3.84 V (TFT2) anodized Al_xO_y. Both devices work in *n*-type mode with linear, pinch-off and saturation regimes clearly seen, suggesting a good Ohmic contact between IGZO and Al source/drain electrodes.

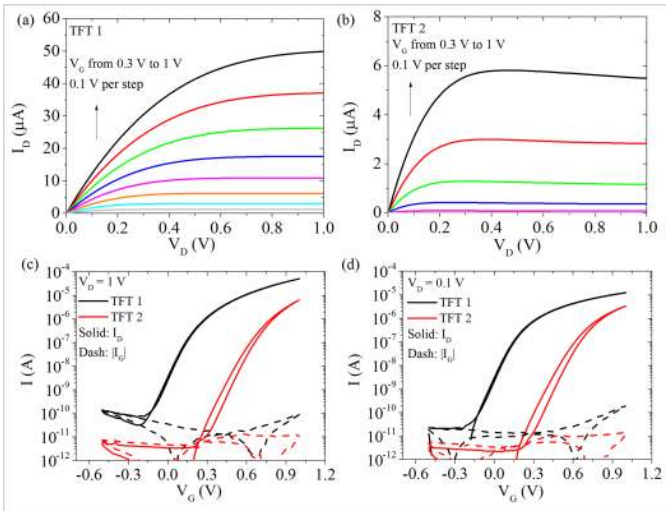

Fig. 2. Electrical properties of IGZO TFTs. Output characteristics of (a) TFT1 and (b) TFT2. Transfer characteristics of TFT1 and TFT2 at (c) V_D = 1 V and (d) V_D = 0.1 V. The anodization voltages of the Al_xO_y in TFT1 and TFT2 are 2.3 and 3.84 V, respectively.

The corresponding transfer characteristics of TFT1 and TFT2 at different drain voltages are shown in Figs. 2(c) and (d). Both devices exhibit a high current on/off ratio > 10^6 at both V_D = 1 V (saturation regime) and V_D = 0.1 V (linear regime). A lower gate leakage current, I_G, is found for TFT2, which is due to the slightly thicker Al_xO_y formed through anodization (approximately 3 and 5 nm thick Al_xO_y films for TFT1 and TFT2, respectively). The subthreshold swing, *SS*, is found to be 82 and 87 mV/dec for TFT1 and TFT2, respectively, both of which are close to the theoretical limit of *SS* at 300 K [14]. A small clockwise hysteresis is found in the transfer characteristics of TFT2, which is likely due to the charge trapping effects at the dielectric/channel interface [15] and is considered as the reason for the slightly drop of drain current, I_D, in the output characteristics shown in Fig. 2(b). The turn-on voltage, V_{ON}, is −0.2 V for TFT1 and 0.2 V for TFT2. The threshold voltage difference between TFT1 and TFT2 is found to be ~ 0.4 V. The linear mobility, μ_{lin}, and saturation mobility, μ_{sat}, are calculated to be 6.6 and 6.1 cm^2/Vs for TFT1, and 5.4 and 5 cm^2/Vs for TFT2. The electrical properties of both devices are comparable to or even better than most of the low-voltage IGZO TFTs reported previously [11, 16-19], demonstrating the potential for embedding in circuits with low-voltage operations.

Voltage transfer characteristics of the inverter are shown in Fig. 3(a). For both supply voltages, output voltage at low-states, V_{OL}, is always 0 V and output voltage at high-states, V_{OH}, is always the same as the supply voltage, V_{DD}, suggesting that this is a full swing inverter. The input high voltage (V_{IH})

and input low voltage (V_{IL}) are defined as the voltages where the input/output curve has a slope of −1. For V_{DD} = 1 V, V_{IL} and V_{IH} are found to be 0.48 and 0.54 V, respectively, showing a narrow transition width ($V_{IH} - V_{IL}$) of 0.06 V. Narrow transition widths, such as this, can enable improved response times in logic circuits. The noise margin high, N_{MH}, is 0.46 V by using ($V_{OH} - V_{IH}$), and the noise margin low, N_{ML}, is 0.48 V which equals $V_{IL} - V_{OL}$. For a circuit operation, ideally a balanced noise margin, $N_{MH} = N_{ML} = V_{DD}/2$, is achieved. Hence, the achieved values are 92% of the optimal value of N_{MH} and 96% of the optimal value of N_{ML}, indicating that the inverter could withstand a high noise level. The switching threshold voltages, V_M, of the inverter, where $V_{OUT} = V_{IN}$, are found to be 0.48 and 0.51 V, at V_{DD} of 0.8 and 1 V, respectively, which are both very close to their ideal value, $V_{DD}/2$. As shown in Fig. 2 (c), the bias current gave by the depletion load (I_D of TFT1 at V_G = 0 V) matches the current of the drive transistor (TFT2) at $V_G \approx 0.5$ V. Therefore, it is expected that the peak gain occurs at a V_{IN} of around 0.5 V, which is in agreement with the results shown in Fig. 3(b).

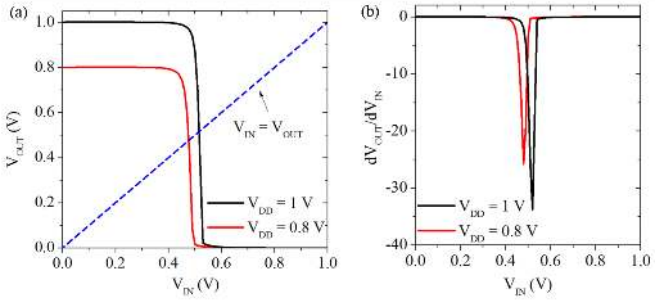

Fig. 3. (a) Measured output voltage (V_{OUT}) and (b) voltage gains as functions of input voltage (V_{IN}) at different supply voltages (V_{DD}).

Fig. 3(b) also shows that high voltage gains of 26 and 34 are achieved at V_{DD} = 0.8 and 1 V respectively, even if the load and drive TFTs have the same channel width to length ratio. These voltage gains are comparable to or even surpass the values reported previously in *n*-type oxide-TFT-based inverters under similar supply voltages (Table I). The electrical performance of the inverter might be further optimized by modifying the width to length ratio of the load and drive TFTs [20].

A comparison with previously reported *n*-type oxide-TFT-based, low-voltage inverters is shown in Table I. Clearly, all the key parameters of our devices are among the best to date.

TABLE I: PERFORMANCE OF LOW-VOLTAGE INVERTERS BASED ON *N*-TYPE OXIDE TFTS

Ref.	Channel Load/Drive	Gain	V_{DD} (V)	V_M (V)	N_{MH}/V_{DD}	N_{ML}/V_{DD}	$V_{IH} - V_{IL}$ (V)
This work	**IGZO/IGZO**	**34**	**1**	**0.51**	**46%**	**48%**	**0.06**
		26	**0.8**	**0.48**	**38%**	**53%**	**0.07**
[8]	IGZO/IGZO	24	1	/	59%	29%	0.12
[21]	IZO/IGZO	43.9	2	/	/	/	<0.2
[22]	ZnO/ZnO	32	5	1.57	63%	23%	0.69
[23]	SZTO/ZTO	6	5	/	/	/	/
[24]	ZnO/ZnO	2	5	/	/	/	/
[25]	IGZO/IGZO	15.5	5	15.2	/	/	/
		5.9	5	4.25	/	/	/
[26]	IGZO/IGZO	14	5	/	71%	12%	0.85

Fig. 4 shows a comparison between the inverters loaded by TFT1 (Inverter 1) and inverters loaded by a 100 MΩ resistor (Inverter 2). Although both types of inverters show full voltage swings, the comparisons in terms of voltage gains, transition widths and noise margins clearly show that the proposed depletion-load inverters exhibit huge advantages over resistor-load inverters.

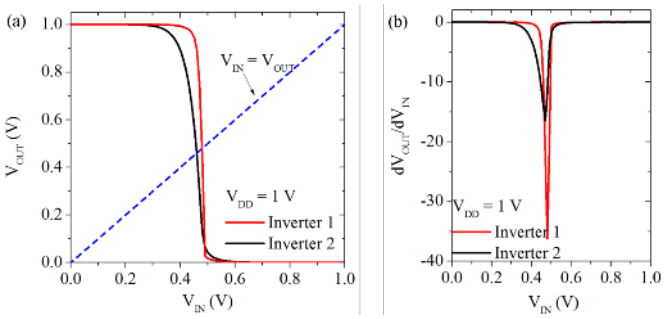

Fig. 4. (a) V_{OUT} and (b) voltage gains as functions of V_{IN} at V_{DD} = 1 V.

To investigate the long-term stability of the inverter, the devices were measured again after storing in air for 90 days. The superb air stability of the anodized Al_xO_y/IGZO TFTs ensures the fabricated inverters to exhibit very small changes of voltage swings, voltage gains, transition widths and switching threshold voltages after the storage, as can be seen in Fig. 5.

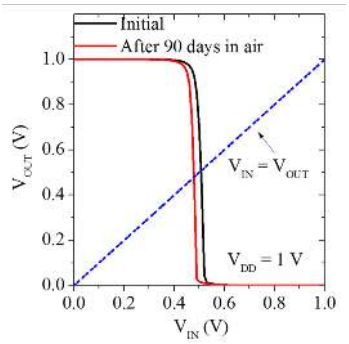

Fig. 5. (a) V_{OUT} as functions of V_{IN} at V_{DD} = 1 V before and after the storage.

In conclusion, high-performance, full-swing IGZO inverters have been demonstrated to be capable of operating at a very low voltage. The threshold voltage difference for the load and drive IGZO TFTs was achieved by simply varying the anodization voltages for the Al_xO_y gate dielectrics on different parts of the substrate. The inverters show a voltage gain of up to 34 and a noise margin close to the ideal value at a low supply voltage of 1 V. Such a method might have potential applications in future low-cost, low-power electronics.

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