Low-Voltage High-Transconductance Dinaphtho-[2,3-b:2',3'-f]thieno [3,2-b]thiophene (DNTT) Transistors on Polyethylene Naphthalate (PEN) Foils

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I. Summary And Motivation

Low threshold voltage, high transconductance DNTT transistors (OTFTs) with interdigitated source/drain contacts can provide low-voltage transistor amplifiers with a.c. cut-off frequency in excess of 10 kHz [1], making them suitable for wearable sensors. This paper presents an in-depth study of the geometry of such transistors fabricated on PEN. Changes in channel width-to-length ratio *W*/*L* were achieved by varying the *W* from ~12 to ~18 mm and *L* from 20 to 50 µm, leading to *W*/*L* of ~300 to ~900. The OTFTs exhibit threshold voltage from −0.33 to −0.74 V, field-effect mobility from 0.17 to 0.42 cm^2/V·s, on-current from 28 to 67 µA (at $V_{GS} = V_{DS} = -2$ V), off-current from 6×10^{-12} to 7×10^{-8} A, and subthreshold slope from 65 to 266 mV/decade. While the OTFTs exhibit large on-state drain current and a.c. transconductance, smaller *L* leads to a slightly reduced mobility. In addition, the OTFTs with the largest *W* of 18.23 mm possess the lowest off-state drain current and subthreshold slope.

II. Advances over Previous Works

The implementation of OTFTs in flexible electronics and sensors has grown exponentially in recent years. Examples include disposable sensors [2], flexible displays [3], biosensors [4] and radio frequency identification tags [5]. Traditionally, OTFTs have a 'standard' geometry where the rectangular source and drain contacts are separated by a gap. The typical *W*/*L* of 10 to 30 and the field-effect mobility of 0.5 to 1 cm^2/V·s lead to transistor on-current of a few microamps. Low-voltage DNTT transistors on PEN with such a standard source/drain contact geometry have shown transconductance of 12 µS and operation up to 1 MHz. [6] The use of inter-digitated source/drain contacts allows increasing the channel width of the transistor while keeping the transistor area small. As a result, the transconductance of the transistors can be further increased; making them suitable for applications where moderate switching speeds, low supply voltage and voltage gains are required. This current work reports flexible OTFTs on PEN foils (Optfine, DuPont Teijin) whose trans-conductance far exceeds that reported in [6], while providing the understanding of such transistor geometries.

III. Results and Methodology

P-type OTFTs based on dinaphtho-[2,3-b:2',3'-f]thieno [3,2-b]thiophene (DNTT) were fabricated on PEN following a procedure described in [1,7]. The material and thickness of each layer from bottom to top is as follows: the gate electrode is made of 30-nm-thick Al, gate dielectric is a bi-layer of AlO_x (13.8 nm) coated with a monolayer of octadecyl phosphonic acid (C_{18}PA, 2 nm), organic semiconductor is a 20-nm-thick DNTT and the source/drain contacts are made of 50-nm-thick Au. A top view of two OTFTs demonstrating the varying channel width, cross-sectional transistor view, and transfer characteristics are shown in Figure 1.

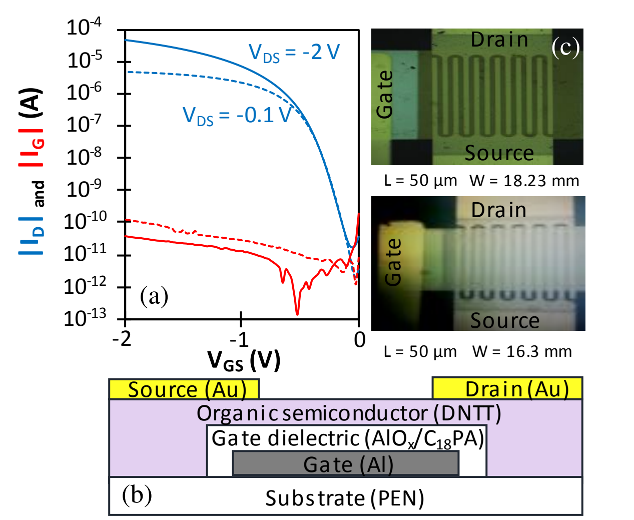

Fig. 1: Transfer characteristics for OTFT with *L* ~ 46 µm, *W* = 17.12 mm (a), cross-sectional view (b), and top views of two OTFTs with different *W* (c).

For the purpose of analysis, the transistors were divided into 3 groups based on their channel lengths, i.e. 20 to 30 µm, 30 to 40 µm and 40 to 50 µm. The channel width was varied between 12.10 and 18.23 mm by adjusting the width of the gate electrode (see Figure 1). As a result, the *W*/*L* varied from 290 to 910. The drain current and a.c. transconductance of the transistor in saturation operation is given by Eq. (1) and (2) respectively, where *C* is the gate dielectric capacitance, μ is the field-effect mobility, V_{GS} and V_{DS} are the gate-source and drain-source voltages, V_{TH} is the threshold voltage, I_D is the drain current, and g_m is the a.c. transconductance. For the a.c. transconductance measurement, a 0.2 V peak-to-peak sinusoidal wave function with a d.c. offset of −2 V and frequency of 1 Hz was applied to the gate of the transistor and the drain current modulation $I_{D_{PP}}$ was measured.

$$I_D = \mu C \left(\frac{W}{2L}\right)(V_{GS} - V_{TH})^2 \tag{1}$$

$$g_m = \mu C \frac{W}{L}(V_{GS} - V_{TH}) = \frac{I_{D_{PP}}}{0.2\ V} \tag{2}$$

Figure 2 shows the effect of *W*/*L* on the field-effect mobility, threshold voltage, on-current, off-current, and inverse subthreshold slope. At low *W*/*L*, OTFTs with the highest channel lengths (L = 40 to 50 µm; W/L = 290 to 440) display

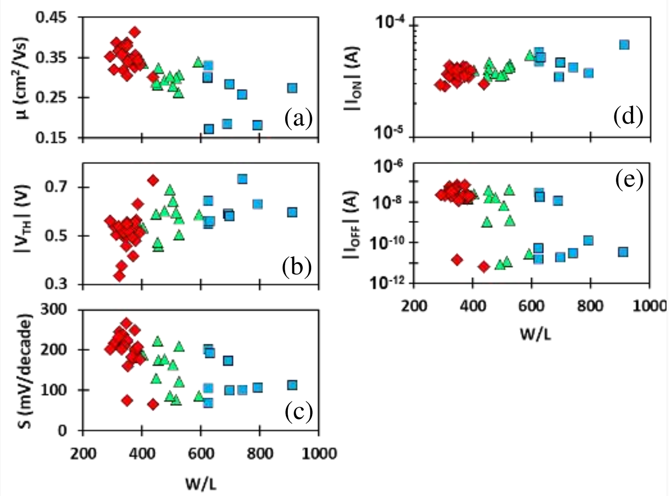

Fig. 2: Field-effect mobility (a), threshold voltage (b), subthreshold slope (c), and on- (d) and off-currents (e) as functions of *W*/*L* (legend of Fig. 3 applies). $|I_{ON}|$ is extracted for $V_{DS} = V_{GS} = -2$ V. $|I_{OFF}| = \min(|I_D|)$ for $V_{GS} = -2$. V.

the highest mobility of 0.35±0.03 cm^2/V·s. For OTFTs with medium channel lengths (L = 30 to 40 µm; W/L = 380 to 590) the mobility reduces slightly to 0.30±0.02 cm^2/V·s. Finally, OTFTs with the shortest channel lengths (L = 20 to 30 µm, W/L = 620 to 910) displayed the lowest mobility of 0.25±0.06 cm^2/V·s. Figure 2(b) shows an increase in the threshold voltage from –0.33 to –0.74 V as *W*/*L* increases and channel length decreases. An average of –0.52 V, –0.57 V and –0.60 V for channel lengths of 40 to 50 µm, 30 to 40 µm, and 20 to 30 µm is observed, respectively. The subthreshold slope S in Figure 2(c) reduces as *W*/*L* increases and channel length decreases. OTFTs with channel lengths between 20 and 30 µm exhibit subthreshold slope of 125±48 mV/decade, while transistors with L between 30 and 40 µm and 40 to 50 µm show values of 147±57 and 198±49 mV/decade respectively. The on-current of Figure 2(d) increases with rising *W*/*L*. OTFTs with L between 20 and 30 µm have an average on-current of 4.9×10^{-5} A, L between 30 and 40 µm leads to an average of 4.0×10^{-5} A and L between 40 and 50 µm to an average of 3.9×10^{-5} A. Finally, Figure 2(e) shows the off-current as a function of *W*/*L*. The off-current is observed to be split into two distinct regions regardless of the channel length. This warrants further analysis that is presented next.

Figure 3(a) shows the on-current normalised with respect to the channel dimensions W and L. Based on Eq. (1) such normalised drain current should remain constant. However, the results show a gradual linear reduction in the on-state drain current as the channel length decreases and *W*/*L* increases. This reduction suggests a presence of contact resistance between the source/drain contacts and DNTT. Such contact resistance will become more dominant with decreasing L. Figure 3(b) shows the normalised off-current as a function of W. Transistors with channel widths less than 18.23 mm display an average off-state drain current of 6.6×10^{-11} A. On the other hand, OTFTs with W = 18.23 mm exhibit an average of 3.5×10^{-14} A, a reduction of ~3.3 orders of magnitude. Similarly, Figure 3(c) indicates consistently reduced subthreshold slope for OTFTs with W = 18.23 mm, exhibiting values between 54 and 114 mV/decade.

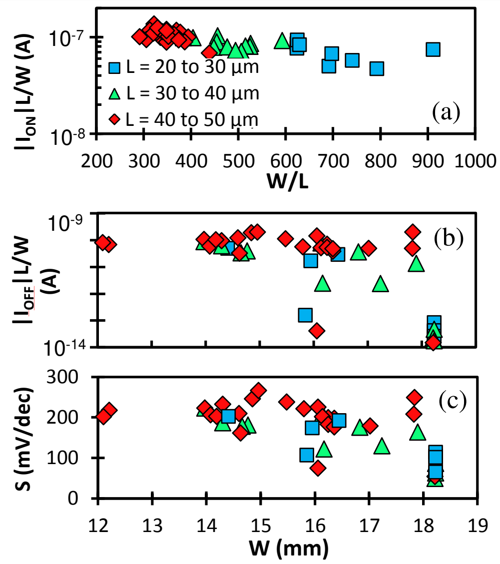

Fig. 3: Normalised transistor on-current ($|I_{ON}|\times\frac{L}{W}$) versus *W*/*L* (a), normalised off-current ($|I_{OFF}|\times\frac{L}{W}$) versus W (b), and subthreshold slope S versus W (c).

An example of a.c transconductance measurement is shown in Figure 4 for three OTFTs. Drain voltage of –2 V, source voltage of 0 V and gate voltage of –0.2 V_{PP} (–2 V d.c. offset) at 1 Hz were used. Transistor T1 showed the largest trans-conductance of 53.2 µS, followed by T2 and T3 with 41.3 and 37.9 µS respectively. The transistor cut-off frequency in excess of 1 kHz has been reported previously. [1]

In summary, optimisation of organic thin-film transistors with interdigitated source/drain contact is presented. The results confirm that the contact geometry plays an important role, predominantly affecting the off-state drain current and the subthreshold slope. The transistors with the largest L and W show the best performance.

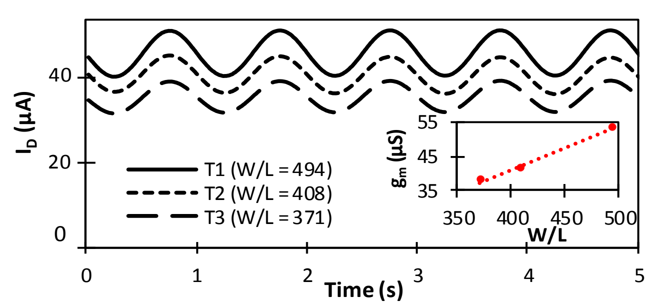

Fig. 4: A.c. drain current as a function of time (f = 1 Hz, V_G = –0.2 V_{pp} with –2 V d.c. offset, V_D = –2 V, and V_S = 0 V).

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