

# Low-Voltage Hot-Electron Currents and Degradation in Deep-Submicrometer MOSFET's

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**Abstract**—Hot-electron currents and degradation in deep submicrometer MOSFET's at 3.3 V and below are studied. Using a device with  $L_{\text{eff}} = 0.15 \mu\text{m}$  and  $T_{\text{ox}} = 7.5 \text{ nm}$ , substrate current is measured at a drain bias as low as 0.7 V; gate current is measured at a drain bias as low as 1.75 V. Using the charge-pumping technique, hot-electron degradation is also observed as drain biases as low as 1.8 V. These voltages are believed to be the lowest reported values for which hot-electron currents and degradation have been directly observed. These low-voltage hot-electron phenomena exhibit similar behavior to hot-electron effects present at higher biases and longer channel lengths. No critical voltage for hot-electron effects (such as the Si-SiO<sub>2</sub> barrier height) is apparent. Established hot-electron degradation concepts and models are shown to be applicable in the low-voltage deep submicrometer regime. Using these established models, the maximum allowable power supply voltage to insure a 10-year device life-time is determined as a function of channel length (down to 0.15  $\mu\text{m}$ ) and oxide thicknesses.

## I. INTRODUCTION

BECAUSE of hot-electron reliability limitations, the power supply voltage for future VLSI systems will have to be reduced. However, as channel lengths approach the deep submicrometer regime and as the power supply voltage approaches the Si-SiO<sub>2</sub> barrier height, the validity of established hot-electron models and concepts must be re-examined. It has been hoped that for drain biases lower than some critical value (e.g., 2.7 V), electrons would not be able to gain sufficient energy to generate gate current or to cause interface damage and device degradation regardless of the amount that the channel length is reduced [1]. However, studies have shown that measurable device degradation occurs at  $V_{\text{Drain}} = 2.5 \text{ V}$  at room temperature for a device with  $L_{\text{eff}} = 0.3 \mu\text{m}$  [2] and at  $V_{\text{Drain}} = 2.2 \text{ V}$  at 77 K for a device with  $L_{\text{eff}} = 0.8 \mu\text{m}$  [3]. Because no gate current was detected below the Si-SiO<sub>2</sub> barrier height in either of these two studies, it was concluded that the interface damage was caused by electrons with energies below the Si-SiO<sub>2</sub> energy barrier. However, for a device with  $L_{\text{eff}} = 0.14 \mu\text{m}$ ,  $I_{\text{Gate}}$  has been directly measured at drain biases as low as 2.35 V [4];

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this suggests that electrons can gain energy larger than  $qV_{\text{Drain}}$ . In this paper, a comprehensive study of low-voltage hot-electron currents and degradation is presented. Established hot-electron concepts [6] are shown to be applicable in the low-voltage deep-submicrometer regime. No critical energy for hot-electron effects is apparent.

## II. DEVICE FABRICATION

The deep-submicrometer MOSFET's used in this study were fabricated using an NMOS technology for which the temperature cycle after source/drain implantation (As,  $3 \times 10^{15} \text{ cm}^{-2}$ , 50 keV, 0° inclination) was limited to 30 min at 900°C in order to reduce the junction depth. Conventional g-line optical lithography ( $\lambda = 436 \text{ nm}$ ) was used to define all levels, including that for the gate. The deep-submicrometer gates were obtained by calibrated thinning of the optical defined photoresist patterns in oxygen plasma [7]. Gate oxides ranging from 5.6 to 15.6 nm in thickness were grown. Threshold voltage implants were chosen to adjust the long-channel  $V_T$  between 0.4 and 0.6 V for all oxide thicknesses; the average surface substrate doping ranged from  $4 \times 10^{17}$ – $10^{18} \text{ cm}^{-3}$ . The junction depth, as determined by spreading resistance measurements, is 0.16  $\mu\text{m}$ .

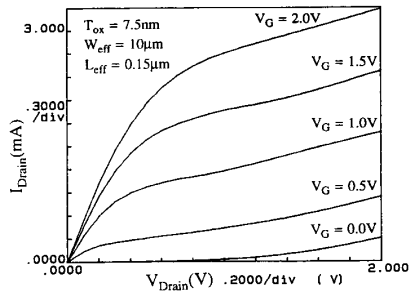
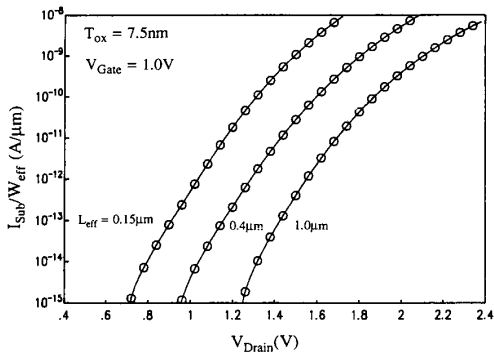
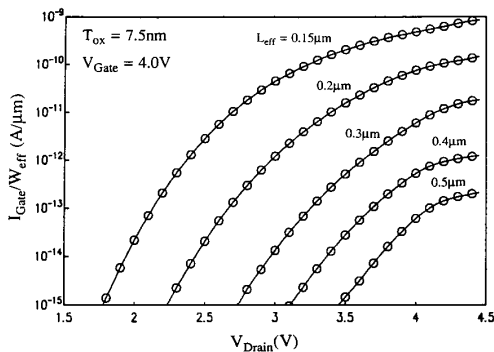
Different electrical techniques [8]–[10] were used to determine the effective channel length. There exists at least a 0.05- $\mu\text{m}$  uncertainty in the value of  $L_{\text{eff}}$  calculated using these electrical methods. In this study, the mean value of the various techniques is used. Fig. 1 displays the drain-current characteristics for an  $L_{\text{eff}} = 0.15 \mu\text{m}$  device.

## III. LOW-VOLTAGE HOT-ELECTRON CURRENTS

### A. Low-Voltage Substrate and Gate Current Characteristics

Figs. 2 and 3 display substrate and gate current as a function of drain voltage for different channel lengths. For the  $L_{\text{eff}} = 0.15 \mu\text{m}$  device,  $I_{\text{Sub}}$  is observed at  $V_{\text{Drain}} = 0.7 \text{ V}$ ;  $I_{\text{Gate}}$  is observed at  $V_{\text{Drain}} = 1.75 \text{ V}$ . These values are considerably lower than previous voltages for which  $I_{\text{Sub}}$  and  $I_{\text{Gate}}$  have been directly measured [4].

In Figs. 2 and 3, the device width is 10  $\mu\text{m}$ . Thus the minimum current value that is reported in this study ( $10^{-14} \text{ A}$ ) is well within the measurement sensitivity of existing equipment (HP 4140B pico-ammeter). Care was

Fig. 1. Drain current characteristics of a 0.15- $\mu\text{m}$  device.Fig. 2. Substrate current versus drain bias for different  $L_{\text{eff}}$ .  $T_{\text{ox}}$  is 7.5 nm,  $V_{\text{Gate}}$  is 1.0 V.Fig. 3. Gate current versus drain bias for different  $L_{\text{eff}}$ .  $T_{\text{ox}}$  is 7.5 nm,  $V_{\text{Gate}}$  is 4.0 V.

taken to insure that parasitic current components from either junction leakage or Fowler-Nordheim tunneling were negligible.

From Figs. 2 and 3, it is important to note that no major difference in the  $I_{\text{Sub}}$  or  $I_{\text{Gate}}$  characteristics is apparent between low and high drain voltages or between short and long channel lengths. There is no evidence of any critical drain voltage for the hot-electron currents such as  $V_{\text{Drain}} \approx 2.7$  V (the minimum Si-SiO<sub>2</sub> barrier height including the effects of maximum barrier lowering). Fig. 3 also agrees with studies which have indirectly observed gate

current at drain biases as low as 1.4 V from the threshold-voltage shift of floating-gate devices with an  $L_{\text{eff}}$  of 0.3  $\mu\text{m}$  and a bottom oxide thickness of 40 nm [11].

Based on the effective-temperature model, analytical expressions for substrate and gate current have been developed [4], [5].

$$I_{\text{Sub}} \propto I_{\text{Drain}} e^{-\Phi_i/kT_c} \quad (1)$$

$$I_{\text{Gate}} \propto C_1(E_{\text{ox}}) I_{\text{Drain}} e^{-\Phi_B/kT_c} \quad (2)$$

where  $C_1(E_{\text{ox}})$  is a weak function of the gate-drain oxide field  $E_{\text{ox}}$ ,  $T_c$  is the effective electron temperature,  $\Phi_i$  is the critical energy required for impact ionization, and  $\Phi_B$  is the effective barrier height (a function of  $E_{\text{ox}}$  due to the barrier lowering). Expressions similar to (1) and (2) can also be derived based on the lucky-electron model [12]. The quantity  $T_c$  is modeled as a function of the peak lateral electric field  $E_m$ .

$$T_c = \left[ \frac{q\lambda}{k} \right] E_m \quad (3)$$

where  $\lambda$  is the electron mean-free path length.

From (1) and (2), by eliminating the exponential  $T_c$  (or  $E_m$ ) term, one can derive the following correlation between the gate and substrate currents [12]:

$$\frac{I_{\text{Gate}}}{I_{\text{Drain}}} = C_2(E_{\text{ox}}) \left[ \frac{I_{\text{Sub}}}{I_{\text{Drain}}} \right]^{(\Phi_B/\Phi_i)} \quad (4)$$

where  $C_2(E_{\text{ox}})$  is a weak function of  $E_{\text{ox}}$ . As shown in Fig. 4, the correlation in (4) exists for a device with  $L_{\text{eff}} = 0.15$   $\mu\text{m}$  and for drain biases as low as 2.1 V. The slope of the data in Fig. 4 shows that  $\Phi_B/\Phi_i = 2.5$  for  $E_{\text{ox}} = 0$ . Using a value  $\Phi_B = 3.2$  V (at  $E_{\text{ox}} = 0$ ), one obtains  $\Phi_i = 1.3$  eV which is in good agreement with previous estimates of this energy [12]. The decrease in slope in Fig. 4 as  $E_{\text{ox}}$  increases is due to the reduction in  $\Phi_B$  from barrier lowering.

In Figs. 2 and 3, there appears to be no abrupt change in the substrate or gate current characteristics as the effective channel length is reduced down to 0.15  $\mu\text{m}$ ; likewise, there appears to be no abrupt change as the drain bias is reduced. In Fig. 4, no change in the correlation between substrate and gate current is observed even at low  $V_{\text{Drain}}$ . These observations suggest that the physical mechanisms responsible for hot-electron currents at long  $L_{\text{eff}}$  and at high  $V_{\text{Drain}}$  are also likely to be present in the low-voltage deep-submicrometer regime.

### B. Mechanisms for Energy Gain Beyond $qV_{\text{Drain}}$

From Fig. 2, it is evident that substrate current is present at drain voltages well below what is considered the threshold energy for impact ionization ( $\approx 1.65$  eV) [13] as well as the silicon bandgap energy at room temperature (1.1 eV). From Fig. 3, it is also evident that gate current is present at drain voltages well below the Si-SiO<sub>2</sub> barrier height even including the effects of barrier lowering ( $\approx 2.7$  eV) [12]. A simple lucky-electron model [1], in

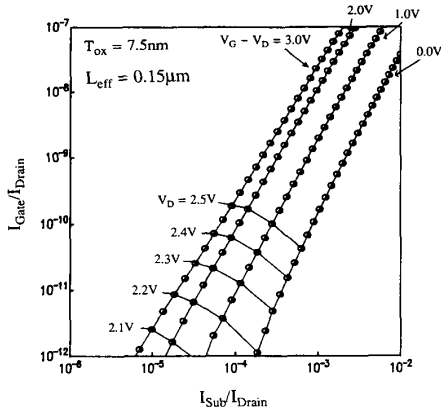


Fig. 4. Correlation between gate and substrate current for different values of  $V_G - V_D$ .  $L_{eff}$  is  $0.15 \mu\text{m}$ ,  $T_{ox}$  is  $7.5 \text{ nm}$ . Contours of constant  $V_D$  and  $V_G - V_D$  are shown.

which carriers gain all their kinetic energy from the applied external potential, is not adequate to explain this low-voltage behavior.

There exist several possible explanations for the existence of low-voltage hot-electron currents. The quasi-equilibrium model proposes that the hot-electron gas in the channel exists in quasi-equilibrium at an elevated electron temperature due to heating from frequent electron-electron and/or electron-phonon collisions. The electron temperature is a strong function of the lateral electric field. Additional electron heating can also occur due to the thermionic emission of hot electrons in the presence of vertical electric fields (real space transfer) [14]. The heated electron gas can be characterized by either a Maxwellian [15] or a non-Maxwellian [16] energy distribution. The low-voltage substrate and gate currents are due to electrons, existing in the high-energy region of the energy distribution, which require only minimal additional energy from the applied external electric field to either undergo impact ionization or overcome the oxide potential barrier.

Next, Auger recombination, where an electron and hole recombine transferring their energy to another electron, has also been proposed as a possible mechanism for supplying the additional required energy for the hot-carrier currents [11]. Finally, Monte Carlo simulations and theoretical considerations suggest that electron-phonon interactions at high energies in the silicon conduction band can lead to quantum-mechanical collision broadening which results in a dispersion of the electron energy levels [17].

#### IV. LOW-VOLTAGE HOT-ELECTRON DEGRADATION

##### A. The Charge-Pumping Measurement Technique

Because of its increased sensitivity over conventional  $I-V$  measurements, the charge-pumping technique [18] is used to monitor low-voltage hot-electron degradation. Fig. 5 displays the experimental setup used in this study. When periodic voltage pulses are applied to the gate of a

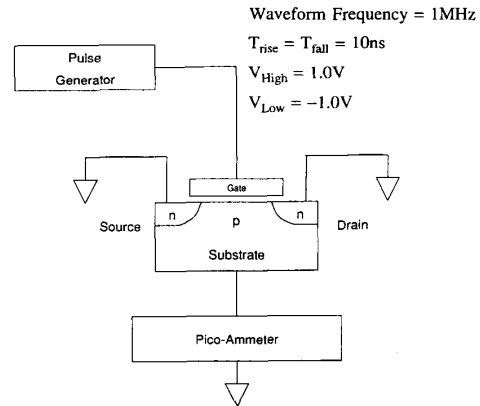


Fig. 5. Charge-pumping experimental setup.

MOSFET whose source and drain are grounded, the surface is alternately biased between inversion and accumulation. During inversion, interface states are filled by conduction-band electrons supplied by the source and drain. During accumulation, this trapped charge recombines with substrate holes producing substrate current.

In this study, the charge pumping measurements were performed using a square-shaped gate-voltage waveform with a frequency of 1 MHz and a rise and fall times of 10 ns. The source and drain were grounded. The gate bias was changed between  $-1$  and  $1$  V. This bias was high enough to insure that the channel was swept between accumulation and inversion, but low enough to prevent any measurement-induced degradation.

##### B. Correlation Between Charge-Pump Degradation and $I-V$ Degradation

Fig. 6 displays the dependence of  $I-V$  and charge-pump degradation and  $I_{Sub}/W_{eff}$  on gate bias. The linear current was measured at  $V_{Drain} = 0.1 \text{ V}$  and  $V_{Gate} = 1.0 \text{ V}$ ; transconductance was measured at the gate bias where  $g_m$  peaks and at  $V_{Drain} = 0.1 \text{ V}$ . The  $I-V$  measurements were performed in the forward mode. From Fig. 6, it is evident that similar to  $I-V$  degradation, charge-pump degradation correlates with the substrate current; maximum degradation for both quantities occurs close to peak  $I_{Sub}/W_{eff}$ . Upon closer examination of Fig. 6, one observes that the  $\Delta I_{cp}/I_{cp0}$  peak occurs at slightly lower  $V_{Gate}$  than does the  $I_{Sub}$  peak. This is because  $\Delta N_{it}$  (which is proportional to  $\Delta I_{cp}/I_{cp0}$ ) is actually expected to correlate with  $I_{Sub}^3/I_{Drain}^2$  rather than  $I_{Sub}/W_{eff}$  [6]. From Fig. 6, it is not clear whether the peak  $\Delta I_D/I_{D0}$  degradation, which is also expected to correlate with  $I_{Sub}^3/I_{Drain}^2$ , occurs at a lower  $V_{Gate}$  than does the  $I_{Sub}/W_{eff}$  peak. From theoretical considerations,  $I_{Sub}^3/I_{Drain}^2$  can be shown to be a more accurate indicator of the electron temperature than  $I_{Sub}/W_{eff}$  [6]. However, it has been shown that for short-channel devices,  $I_{Sub}/W_{eff}$  and  $I_{Sub}^3/I_{Drain}^2$  are comparable degradation monitors [19]. Because the peak  $I_{Sub}/W_{eff}$  condition is more commonly used in typical stressing experiments, in subsequent degradation measurements, devices were

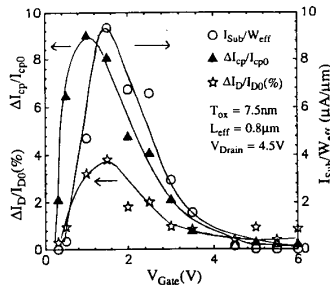


Fig. 6. Correlation between  $\Delta I_{cp}/I_{cp0}$ ,  $\Delta I_D/I_{D0}$ , and  $I_{Sub}/W_{eff}$ . Devices were stressed at  $V_{Drain} = 4.5$  V for varying  $V_{Gate}$  ( $T_{stress} = 50$  min).

stressed at a fixed gate bias at the point of maximum charge-pump degradation which is close to the peak substrate current ( $V_{Gate} = 1.0$  V).

Fig. 7(a) and (b) displays the correlation between linear current and transconductance degradation and charge-pump degradation. A linear relation between  $\Delta I_D/I_{D0}$ ,  $\Delta g_m/g_{m0}$ , and  $\Delta I_{cp}/I_{cp0}$  is observed. Because charge pumping is sensitive only to interface states, Figs. 6 and 7 agree with the theory that interface-state generation is the primary cause of hot-electron-induced degradation [4], [20], [21].

C. Low-Voltage Hot-Electron Degradation Concepts

In Fig. 8, the percent change in the charge-pump current is plotted as a function of time for different stress voltages. No change in the time dependence is observed for stress voltage as low as 1.8 V. A slope of  $n \approx 0.5$  is observed which is in agreement with previously reported values for both  $I-V$  [4], [20], [21] and charge-pump [21], [22] degradation. The quantities  $\Delta I_D/I_{D0}$  and  $\Delta g_m/g_{m0}$  also exhibit a similar time dependence to that of  $\Delta I_{cp}/I_{cp0}$ .

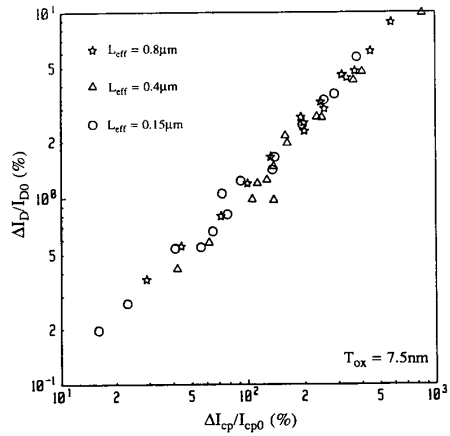
In Fig. 9,  $\Delta I_{cp}/I_{cp0}$  is shown to correlate with substrate current over a wide voltage range of drain voltages (even down to 1.8 V). A hot-electron degradation model relating hot-electron-induced interface states with substrate current has been developed [6]. The number of hot-electron-induced interface states can be expressed as a function of the electron temperature [6].

$$\Delta N_{it} \propto I_D^n e^{-n\Phi_{it}/kT_c} \propto e^{-n\Phi_{it}/kT_c} \quad (5)$$

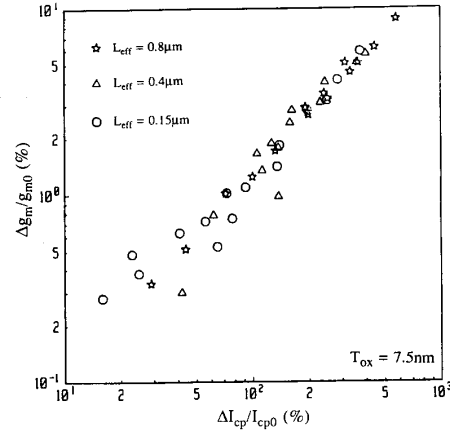
For a fixed-gate bias and oxide thickness, the drain current does not change significantly over the range of drain biases normally used during hot-electron stressing. Thus the term  $I_D$  can be considered a constant. From (1) and (5), one obtains [6]

$$\Delta N_{it} \propto \frac{\Delta I_{cp}}{I_{cp0}} \propto \frac{\Delta I_D}{I_{D0}} \propto \left[ \frac{I_{Sub}}{I_{Drain}} \right]^{(\Phi_{it}/\Phi_i)n} \approx \left[ \frac{I_{Sub}}{W_{eff}} \right]^{(\Phi_{it}/\Phi_i)n} \quad (6)$$

where  $\Phi_{it}$  is the critical energy for interface-state formation, and the quantity  $n$  describes the time dependence of the degradation. From Fig. 9, the slope is approximately equal to 1.25. Using a value of  $\Phi_i \approx 1.3$  V [12] and a



(a)



(b)

Fig. 7. Correlation between charge-pump current degradation and (a) linear drain current degradation ( $\Delta I_D/I_{D0}$ ) (b) linear peak transconductance degradation ( $\Delta g_m/g_{m0}$ ).  $T_{stress}$  ranges from 1 to 500 min.

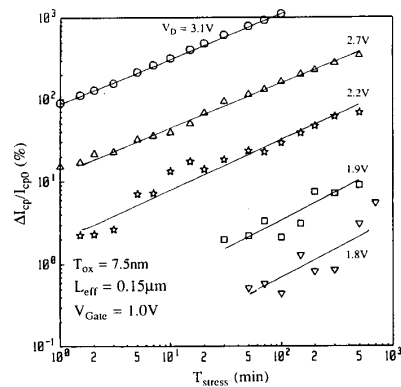


Fig. 8. Charge-pump current degradation ( $\Delta I_{cp}/I_{cp0}$ ) as a function of time for different drain voltages.  $V_{Gate}$  is 1.0 V,  $L_{eff}$  is 0.15  $\mu\text{m}$ ,  $T_{ox}$  is 7.5 nm.

value of  $n \approx 0.5$  (from Fig. 8), one obtains  $\Phi_{it} \approx 3.3$  V which is comparable to previous estimates of this quantity [6]. Thus using  $I_{Sub}/W_{eff}$  (or the more accurate  $I_{Sub}^3/I_{Drain}^2$ ) as a degradation monitor appears to be ap-

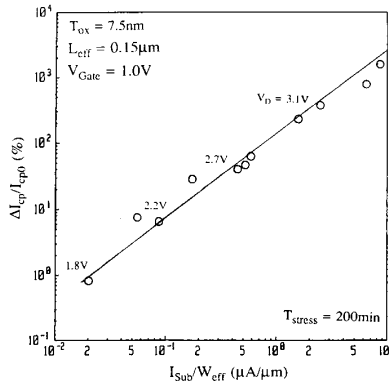


Fig. 9. Correlation between  $\Delta I_{cp}/I_{cp0}$  and  $I_{Sub}/W_{eff}$ .  $L_{eff}$  is 0.15  $\mu\text{m}$ ,  $T_{ox}$  is 7.5 nm.

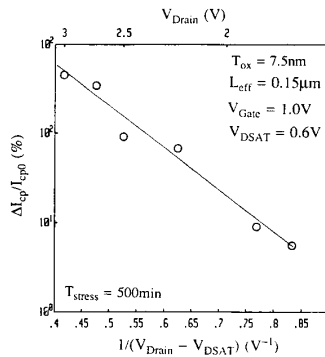


Fig. 10. Correlation between  $\Delta I_{cp}/I_{cp0}$  and  $1/(V_{Drain} - V_{DSAT})$ .  $L_{eff}$  is 0.15  $\mu\text{m}$ ,  $T_{ox}$  is 7.5 nm.

plicable even for drain voltages much below the Si-SiO<sub>2</sub> barrier height and  $\Phi_{it}$ .

Substrate current has been shown to be proportional to  $e^{\Phi_{it}/q\lambda E_m}$  [6]. Using quasi-two-dimensional analysis, the maximum lateral electric field at the drain can be modeled as  $E_m = (V_{Drain} - V_{DSAT})/l_0$  [23] where the quantity  $l_0$  is a characteristic length of the lateral electric field and is a function of channel length, oxide thickness, and junction depth. This electric field model has been shown to be valid for devices with  $L_{eff}$  as small as 0.2  $\mu\text{m}$  [24]. Fig. 10 shows that the correlation between hot-electron degradation and  $1/(V_{Drain} - V_{DSAT})$ , which has been shown to exist for longer  $L_{eff}$  and higher  $V_{Drain}$  [2], [3], also exists in the low-voltage deep-submicrometer regime. This result suggests that  $E_m$  can still be considered the driving force behind hot-electron degradation. Thus established hot-electron degradation concepts and lifetime prediction models appear to be applicable in the low-voltage deep-submicrometer regime.

### V. HOT-ELECTRON RELIABILITY

#### A. Length and Oxide Thickness Dependence of Hot-Electron Degradation

Having shown that existing degradation models are valid in the low-voltage deep-submicrometer regime,

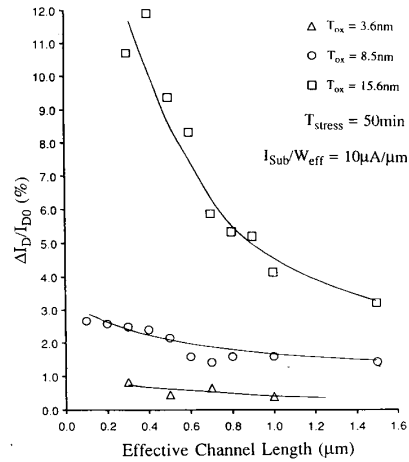


Fig. 11. Linear drain current degradation as a function of channel length for different oxide thicknesses. The devices were stressed as  $I_{Sub}/W_{eff} = 10 \mu\text{A}/\mu\text{m}$ .

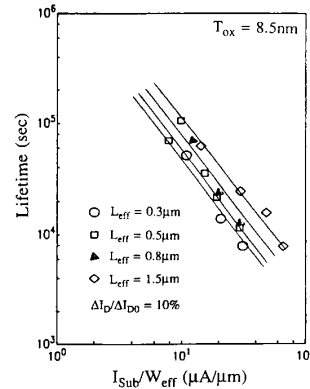


Fig. 12. Device lifetime versus  $I_{Sub}/W_{eff}$  for different channel lengths. Lifetime is defined as 10% linear current degradation.

these models [6] are now applied to determine the maximum allowable power supply voltage. In Fig. 11, linear current degradation is plotted as a function of channel length for different oxide thicknesses; all devices have been stressed under the condition of  $I_{Sub}/W_{eff} = 10 \mu\text{A}/\mu\text{m}$  for 50 min. In Fig. 12, device lifetime is plotted as a function of  $I_{Sub}/W_{eff}$ ; device lifetime is defined as the stress time required to reach a 10% reduction in the forward linear current drive for a bias of  $V_{Gate} = 3 \text{ V}$  and  $V_{Drain} = 0.1 \text{ V}$ .

In both Figs. 11 and 12, even at the same substrate current, hot-electron degradation worsens as  $L_{eff}$  is reduced. This phenomenon is believed to be due to the nonscalability of the degraded region [25]; as the channel length is reduced, the ratio of the length of the degraded region to  $L_{eff}$  increases. In Fig. 11, for the same  $I_{Sub}/W_{eff}$ , less device degradation is observed as the oxide thickness is reduced. It has been proposed that less electron trapping/interface-state generation occurs due to the reduced time

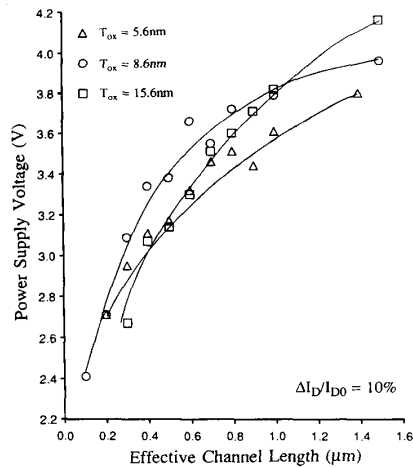


Fig. 13. Voltage required to insure 10-year device lifetime for different oxide thicknesses.

the hot electrons spend in the oxide [26]. In addition, for a fixed measurement bias condition, the  $I$ - $V$  characteristics of thin-oxide devices have been shown to be less affected by a given amount of damage compared with thicker oxide devices [27].

#### B. Deep-Submicrometer Power-Supply Voltage Limitations

Fig. 13 shows the extrapolated maximum allowable power supply voltage to insure a 10-year lifetime as function of  $L_{eff}$  for devices biased at peak  $I_{Sub}$ . For a given substrate current and degradation measurement bias condition, MOSFET's with thinner oxides exhibit less drain-current degradation than those with thicker oxides (see Fig. 11). However, for a given drain bias, MOSFET's with thinner gate oxides also exhibit greater peak  $I_{Sub}$  [6]. These two counteracting trends explain why the hot-electron power-supply values in Fig. 13 are roughly independent of  $T_{ox}$ . The transistors analyzed for Fig. 13 are non-lightly doped drain (LDD) devices and have conventional arsenic drains ( $x_j \approx 0.16 \mu\text{m}$ ). The effect of employing LDD devices is expected to raise vertically the allowable power supply curve by 1 to 2 V depending upon the LDD optimization utilized.

#### VI. CONCLUSIONS

In this study, hot-electron currents and degradation in deep-submicrometer MOSFET's at low voltages have been studied. It is observed that no critical voltage for hot-electron effects is apparent and that the physical mechanisms responsible for hot-electron currents and degradation at long channel lengths and at high drain biases are also likely to be present in the low-voltage deep-submicrometer regime.

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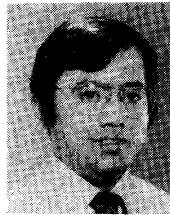
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