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Low-Voltage Operating Ferroelectric FET with Ultrathin IGZO Channel for High-Density Memory Application

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ABSTRACT We have fabricated and demonstrated ultrathin In-Ga-Zn-O (IGZO) channel ferroelectric HfO_2 field effect transistor (FET) with memory operation. Ultrathin-body IGZO ferroelectric FET (FeFET) shows high mobility and nearly ideal subthreshold slop with minimum 8 nm channel thickness, thanks to the properties of IGZO material, junctionless FET operation, nearly-zero low-k interfacial layer on metal-oxide channel and effective capping for realizing ferroelectric phase formation with $HfZrO_2$ (HZO). The controllable memory operations are achieved with the use of back gate. The design guideline of IGZO FeFET is proposed by discussing the thickness of front gate oxide HZO and back gate oxide SiO_2 using TCAD simulation. The material and electrical properties of metal/HZO/IGZO/metal capacitor are also investigated. Metal/HZO/IGZO/metal capacitor has up to 10^8 endurance and over one-year retention. IGZO FeFET shows a potential for high-density and low-power memory application.

INDEX TERMS Junctionless, ferroelectric field effect transistor, non-volatile memory, ferroelectric HfO_2, indium-gallium-zinc-oxide (IGZO).

I. INTRODUCTION

In current highly information-oriented society, artificial intelligent (AI) and Internet of Things (IoT) are driving new innovations, which need to communicate, load and store big data. Data-intensive algorithms such as machine learning are used for edge computing. Therefore, high density and low power consumption non-volatile memories (NVMs) play a key role for developing IoT and AI devices with limited battery capacity and energy-harvesting power supply.

Recently, ferroelectric field effect transistors (FeFET) have attracted more attentions [1]–[3], because ferroelectricity has been discovered in doped HfO_2 [4] which is CMOS-compatible and highly scalable. Due to the field-driven operation of ferroelectric devices, FeFET has several advantages such as non-destructive readout, high program/erase speed, and low power consumption. 3D vertical structure [5]–[9] has been proved to achieve high density in 3D NAND flash memories. Inspired by 3D NAND flash memories, a 3D vertical FeFET has been recently proposed and demonstrated [10]. Poly-Si is used as channel material for vertical structure. However, there are several challenges with poly-Si channel such as low mobility of very thin poly-Si channel and high thermal budget. Moreover, between poly-Si and gate oxide, low-k interfacial layer is formed, which causes voltage loss and subthreshold slope (SS) degradation by charge trapping.

IGZO is a promising channel material for transistor, which was first reported in 2004 [11]. Due to high mobility of very thin body [12], [13], IGZO can be a suitable material for 3D vertical FeFET as illustrated in Fig. 1. Moreover, as shown in Fig. 2, thanks to the junctionless operation of IGZO-based transistor, the interface charge trapping may not be severely involved by comparing to inversion mode transistor. There is much less voltage loss due to the

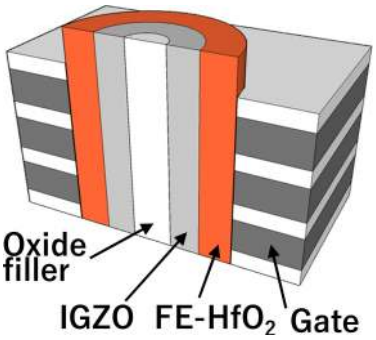

FIGURE 1. Schematic illustration of 3D vertical FeFET of one pillar with ultrathin IGZO channel.

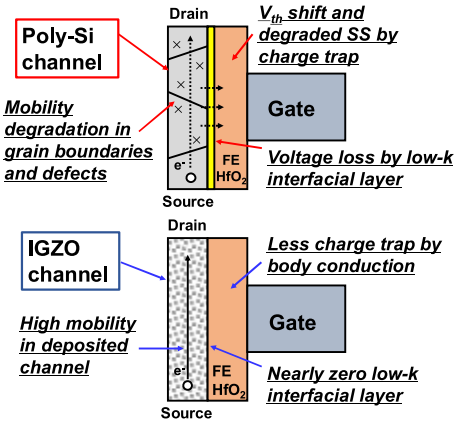

FIGURE 2. Difference between poly-Si channel (upper) and IGZO channel (lower) FeFET.

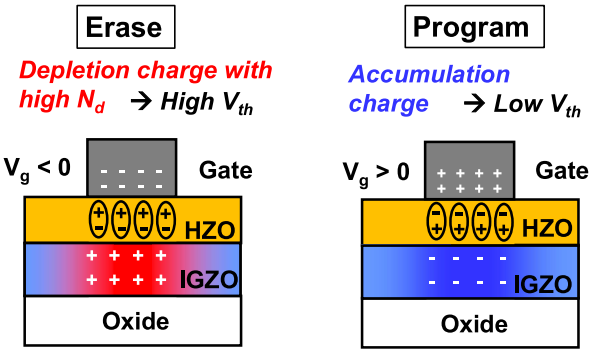

FIGURE 3. Operation of an ultrathin-body IGZO channel FeFET in erase mode (left) and program mode (right).

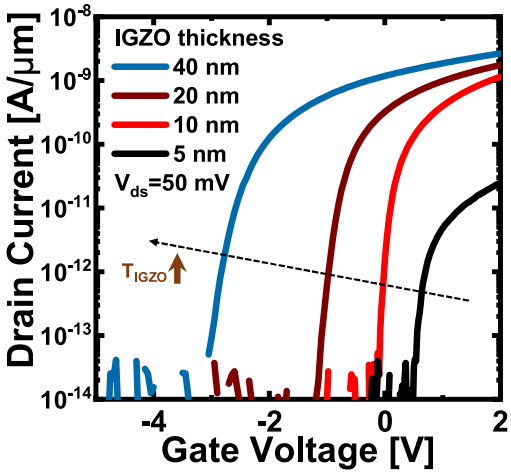

FIGURE 4. Measured $I_d - V_g$ curves of IGZO FETs with SiO_2 gate insulator for different thickness of IGZO channel.

nearly-zero low-k interfacial layer between channel and gate oxide. Therefore, IGZO channel based FeFET [14]–[17] is a promising candidate for high density low power memory application by tackling the challenges. However, the property of metal/HZO/IGZO/metal structure and the device design of IGZO channel based FeFET with ferroelectric-HfO_2 thin film have not been fully investigated, yet.

In this work, we design an ultrathin body IGZO channel ferroelectric-HfO_2(FE-HfO_2) FET with top gate. The device design is proposed to obtain relatively large memory window (MW) by discussing the IGZO, HZO and SiO_2 thickness. Next, we develop the process of ferroelectric-HfO_2 FET with IGZO channel and investigate the property of metal/IGZO/HZO/metal structure. Reliability of metal/IGZO/HZO/metal structure is studied. Finally, we demonstrate IGZO FeFET memory functionality as high density and low power memory device.

II. DEVICE OPERATION AND DESIGN

Fig. 3 shows IGZO FeFET operation. Since IGZO is N^+-type semiconductor, IGZO FeFET operates as junctionless FET. In erase mode, negative V_g induces high density of depletion charge. In program mode, positive V_g induces accumulation charge. Spontaneous polarization can be flipped by electric field and sustained by these charges.

For high density memories, especially, for vertical structure memories, channel thickness should be as thin as possible but without performance degradation. Moreover, the threshold voltage should be near 0 V for memory application. Thus, in our preliminary experiment, bottom gate (front gate) IGZO FET with 15 nm SiO_2 gate insulator was fabricated to investigate the IGZO thickness dependence. Fig. 4 shows the $I_d - V_g$ curves of IGZO FETs with 5∼40 nm IGZO channel. Extracted V_{th} and SS of IGZO FETs are shown in Fig. 5. As the IGZO thickness decreases, V_{th} increases and SS decreases. This is because thinner IGZO means thinner depletion layer, a smaller negative voltage is needed to turn off the channel, and SS becomes steeper [12]. Note that the 5 nm channel IGZO FET has significantly low drain current due to the nonuniformity of IGZO film and the mobility degradation. 8 nm IGZO is chosen for device design with good SS, no drain current degradation and nearly 0 V V_{th}.

In order to check the device concept, we simulate IGZO FeFETs by TCAD. The device structure is a bottom gate structure, which consists of bottom (front) gate, HZO gate insulator, IGZO, SiO_2 layer, top (back) electrode, and source/drain electrodes, as shown in Fig. 10. IGZO thickness is 8nm as determined above. We assume FE-HfO_2 is

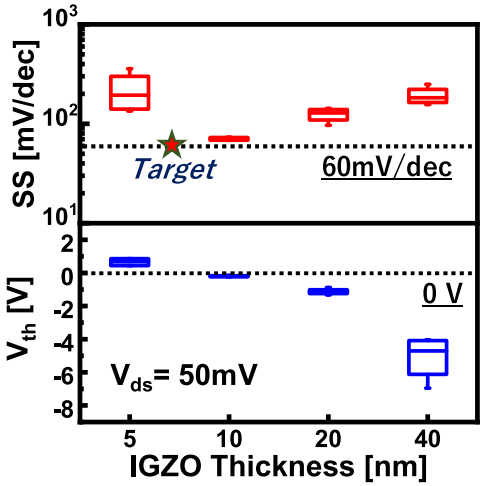

FIGURE 5. Extracted V_{th} and SS from the measured $I_d - V_g$ curves of IGZO FETs with SiO_2 gate insulator.

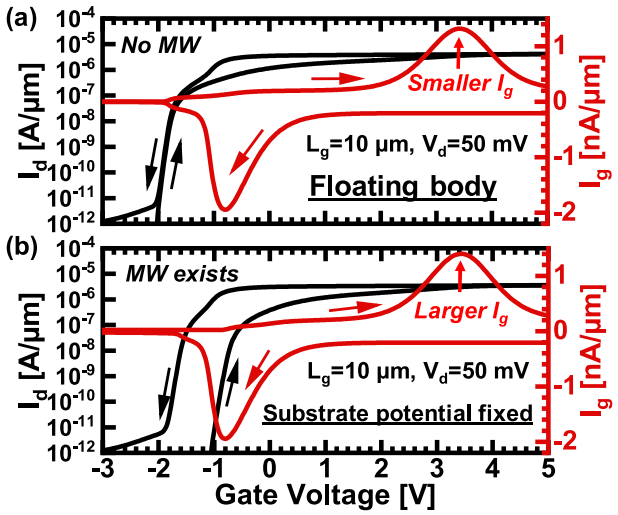

FIGURE 6. Simulated $I_d - V_g$ curve and $I_g - V_g$ curve of IGZO FeFET w/o top gate (a) and w/ top gate (b).

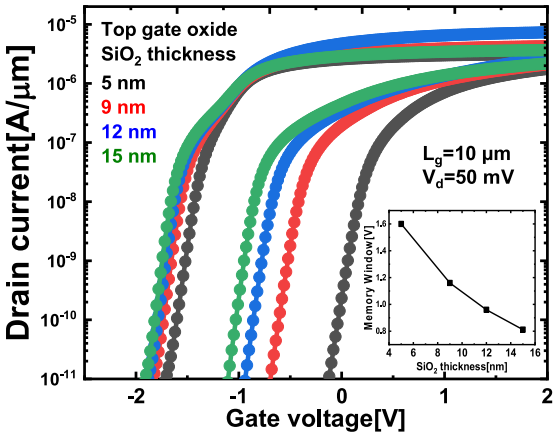

FIGURE 7. Simulated $I_d - V_g$ curves of IGZO FeFET with different thickness of the top gate insulator. The inset is MW.

HZO and the ferroelectric parameters are extracted from our previous work [18]. The dielectric constant (ε), remanent polarization (P_r) and coercive field (E_c) of HZO are 35, 20μC/cm^2 and 1.16MV/cm, respectively. We investigate the impact of the back gate and the thickness dependence of HZO and SiO_2 as critical design parameters. MW is defined as the V_{th} difference between program state and erase state.

Firstly, we study the impact of the back gate. Fig. 6 (a) shows the simulated $I_d - V_g$ and $I_g - V_g$ curves with floating body of IGZO. HZO thicknesses is 15nm. MW is not observed. If the IGZO body is floating, gate voltage is not effectively applied to HZO. Note that simulated $I_g - V_g$ curve shows polarization switching current, which is caused under source and drain pad regions because top source and drain pad overlap with bottom gate. Then, we aim to fix the body potential by back gate through SiO_2 layer. Fig. 6 (b) shows the simulated $I_d - V_g$ and $I_g - V_g$ curves of IGZO FeFETs with the back gate fixed at 0V. SiO_2 and HZO thicknesses are 12nm and 15nm, respectively. MW appears and the gate current increase is observed which indicates polarization switching of FE-HfO_2 under the channel. This is because IGZO body potential is fixed and large electric field can be effectively applied to HZO layer in erase mode.

Secondly, we study the SiO_2 thickness dependence as SiO_2 thickness changes the electrical coupling between the back gate and IGZO body. Fig. 7 shows the simulated $I_d - V_g$ curves with 5∼15 nm SiO_2 layer. HZO thickness is 15nm. The back gate voltage is 0V. As SiO_2 thickness decreases, V_{th} of erase state increases and MW increases because the top gate is close to the channel and fix the body potential close to zero. Thus, large voltage is applied to HZO. We decide to use 12 nm SiO_2 layer to obtain large MW but prevent leakage current from top gate.

Thirdly, we study the HZO thickness dependence. Fig. 8 shows the simulated $I_d - V_g$ curves with different HZO thickness. SiO_2 thickness is 12nm. Back gate voltage is 0V. The property of HZO thin film is related to its thickness [19]. For simplicity, however, we assume ε, E_c and P_r of HZO are constant with different thickness. This assumption can be valid as our simulation is limited to the relatively thick HZO region above 10nm, in which ferroelectric property of HZO does not vary much [20]. As HZO thickness increases, MW increases as shown in the inset of Fig. 8. This is because maximum MW is to be the twice of coercive voltage (V_c) and thicker HZO has larger V_c which is proportional to HZO thickness. Note that, as HZO thickness increases, the capacitance of bottom gate oxide decreases and larger (smaller) voltage is applied to HZO (IGZO) layer. Thus, with thicker HZO layer, more negative V_g is required to turn off the device. 15 nm HZO is chosen due to its close $V_{th} = 0$V and relatively large MW without causing leakage current between the bottom gate and source/drain pads.

III. DEVICE FABRICATION

To study the ferroelectricity in HZO with IGZO layer, a metal-HZO-IGZO-metal stack is fabricated on an N^+ Si

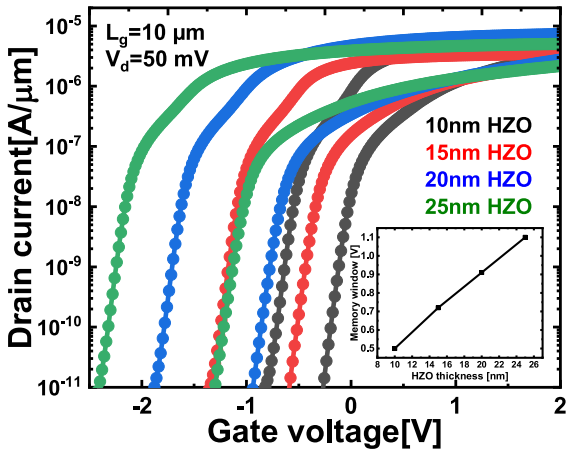

FIGURE 8. Simulated $I_d - V_g$ curves of IGZO FeFET with different thickness of HZO. The inset is MW.

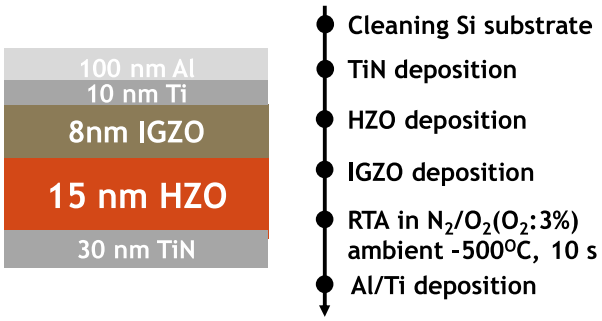

FIGURE 9. The structure and fabrication process of the metal/HZO/IGZO/metal capacitor.

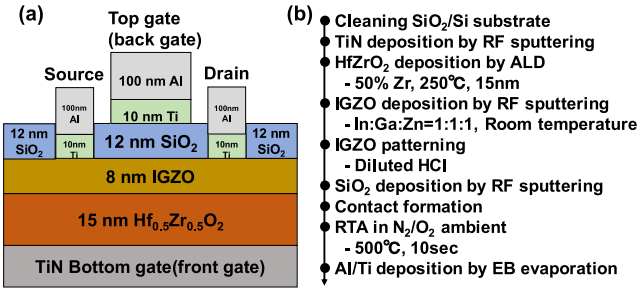

FIGURE 10. (a) Schematic illustration of the device structure of ultrathin-body IGZO FeFET for proof-of-concept, (b) Fabrication process flow of bottom-gate ultrathin-body IGZO FeFET.

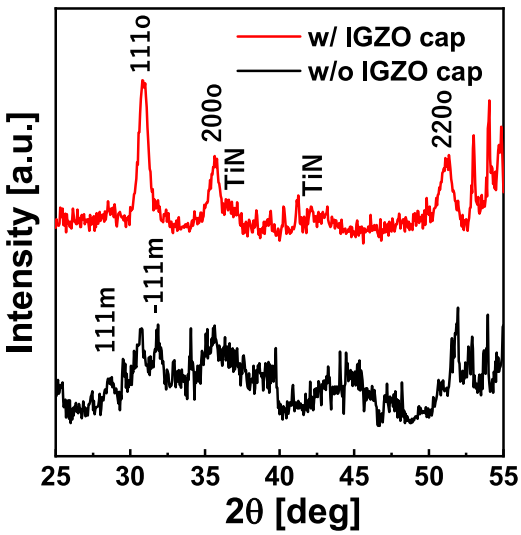

FIGURE 11. Measured GIXRD spectra of HZO film (upper) with and (lower) without IGZO cap after crystallization anneal.

substrate. Fig. 9 shows the metal/HZO/IGZO capacitor structure and the process flow. Thickness of HZO and IGZO are determined in Section II. TiN is deposited by RF sputtering on the RCA-cleaned Si substrate. 15nm 50% Zr-doped $HfZrO_2$ is deposited by atomic layer deposition (ALD) at 250°C. 8nm IGZO and Ti/Al are deposited by RF sputtering and EB evaporation, respectively. Lastly, the stack is annealed by rapid thermal anneal (RTA) in N_2/O_2 (O_2:3%) ambient at 500°C for 10sec.

We also fabricate an IGZO FeFET. Bottom-gate device structure is used for the proof-of-concept as shown in Fig. 10 (a). V_g is applied from the bottom gate. The fabrication process flow is shown in Fig. 10 (b). First, 20nm-thick TiN is deposited as a bottom gate on an RCA cleaned SiO_2/Si substrate by RF sputtering. 15nm 50% Zr-doped HfO_2 is deposited as a gate insulator by ALD system at 250°C. 8nm-thick IGZO is deposited as a channel by RF sputtering in Ar ambient using IGZO target. The carrier concentration is estimated to be $\sim 10^{19}$ cm^{-3} by Hall measurement. Then, IGZO is patterned by diluted HCl. 12nm-thick SiO_2 is deposited as a passivation layer by RF sputtering. RTA is done in N_2/O_2 (O_2:3%) ambient at 500°C for 10sec. Al and Ti are deposited as an optional top gate to fix substrate potential by EB evaporation.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

Fig. 11 compares the measured GI-XRD spectra of HZO film with and without IGZO cap after annealing. The IGZO is a capping material on HZO which provides mechanical strain in the HZO film to preferentially induce ferroelectric-phase as described later. The peak (red line) near 30.4° shows the orthorhombic-phase are formed with IGZO cap after annealing. However, there is no similar peak (black line) without IGZO cap. Thus, the ferroelectricity of HZO can emerge with IGZO capping. Fig. 12 shows the cross sectional TEM images of the fabricated IGZO FeFET. Each layer is uniformly formed. HZO is fully crystallized and IGZO remains amorphous. The interface of HZO and IGZO is free of low-k interfacial layer. Fig. 13 shows the relative atomic concentration in the TiN/HZO/IGZO layers by electron energy loss spectroscopy (EELS) line scan. From the left to right, IGZO, HZO and TiN regions are shown. There is no significant interdiffusion of the elements beyond the resolution of EELS analysis and the sharp interface is realized between HZO and IGZO.

Fig. 14 shows P-V and I-V curves of the TiN/HZO/IGZO/Ti/Al capacitor. The capacitor shows

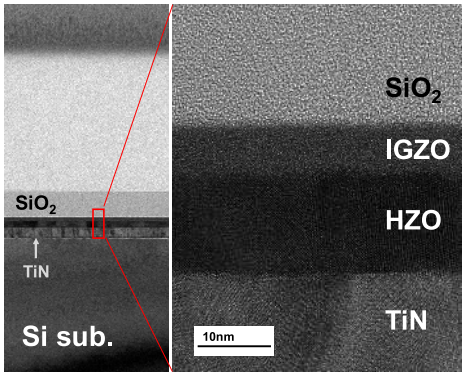

FIGURE 12. Cross sectional low-magnification and high-magnification TEM images of the fabricated SiO_2/IGZO/HZO/TiN structure in the channel region. Each layer is uniformly formed.

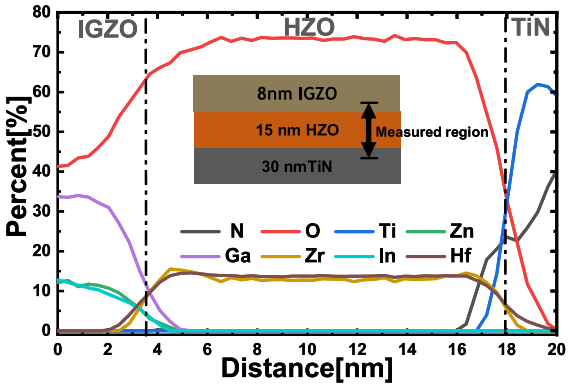

FIGURE 13. Measured relative atomic concentration of TiN/HZO/IGZO layer.

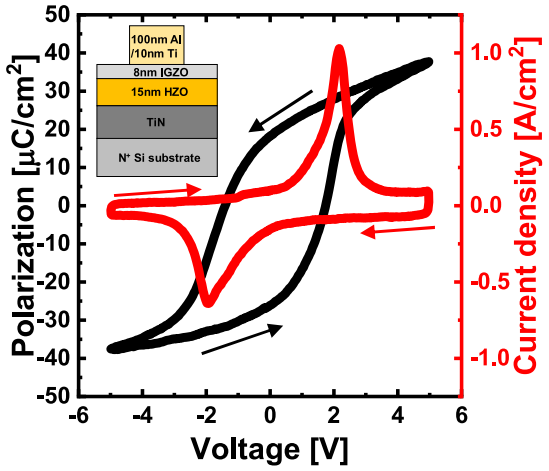

FIGURE 14. Measured P-V and transient I-V curves of the fabricated metal/HZO/IGZO/metal capacitor showing clean ferroelectric property.

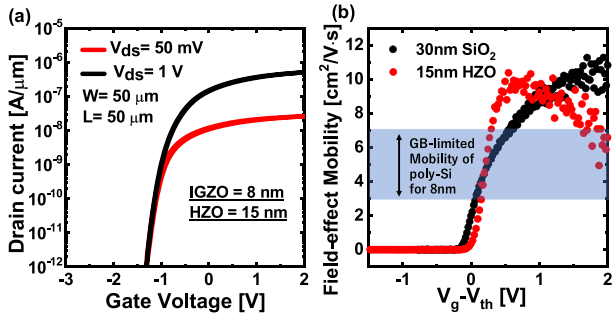

FIGURE 15. (a) Measured $I_d - V_g$ curves of the 8nm-thick IGZO FET with 15nm HZO in a narrow V_g sweep range, (b) Measured field-effect mobility of the 8nm-thick IGZO FET with SiO_2 and HZO gate insulator.

clear ferroelectricity. P_r is about 22 $\mu C/cm^2$ with 5V maximum sweep voltage, which is as large as HZO with TiN top capping [21]. The large P_r is attributed to the low thermal expansions coefficient of IGZO ($\approx 4.31 \times 10^{-6}$/K) [22], because the top electrode with lower thermal expansion coefficient induces large tensile strain in HZO film during rapid thermal process which results in P_r as reported [23]. Metal/HZO/IGZO/metal capacitor has $V_c = 2V$ with 15 nm HZO and 8 nm IGZO. Note that the positive and negative V_c are almost symmetric. For the positive V_g, IGZO is in accumulation, while, for the negative V_g, IGZO is in depletion. However, unlike Si, IGZO has as large dielectric constant as 15. Even with thin IGZO, depletion layer capacitance of IGZO is large, and thus the large voltage can be applied on the HZO layer. In addition, the work function difference between IGZO and TiN preferentially shifts the P-V curve. These are the reasons for the symmetric V_c.

We apply V_g less than switching voltage to prevent polarization switching, leave the top gate floating, and measure $I_d - V_g$ curves with $V_{ds} = 50$ mV and 1 V as shown in Fig. 15 (a). $I_d - V_g$ curves show nearly ideal junctionless FET characteristics. Fig. 15 (b) compares the field effect mobility with HZO and with SiO_2 gate insulator extracted from measured $I_d - V_g$ curves. The field effect mobility is consistent with Hall mobility $\sim 10 cm^2/V{\cdot}s$ and not significantly degraded by HZO gate insulator compared with SiO_2 gate insulator, thanks to the bulk conduction in junctionless FET operation.

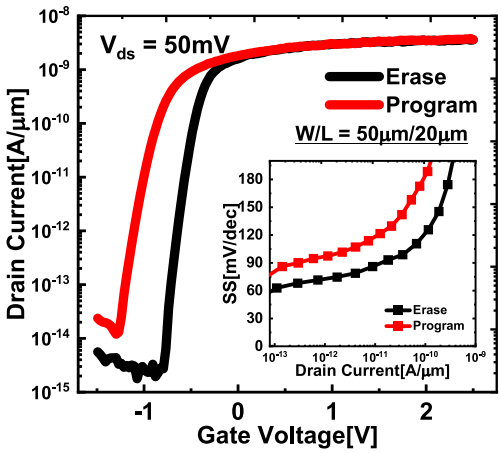

FIGURE 16. Measured $I_d - V_g$ curves of the IGZO FeFET after applying 500μs erase (−3V) / program (+2.5V) voltage. V_g is swept from −1.5V to 2.5V for measurement. MW ~0.5V appears. The inset is SS.

Fig. 16 shows the measured $I_d - V_g$ after applying erase and program pulse voltages from the bottom-gate while the

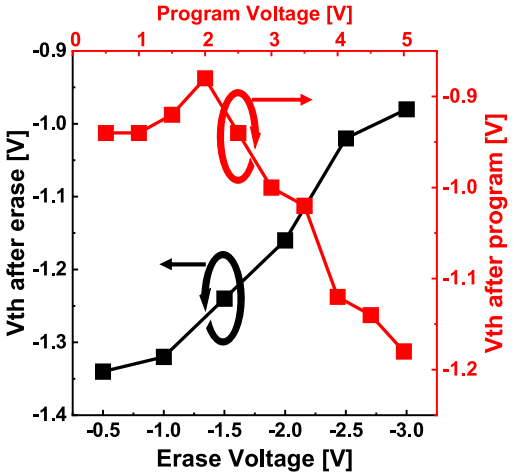

FIGURE 17. Measured voltage-dependent V_{th} shift of the IGZO FeFET after erase/program operation using 500 μs voltage pulse.

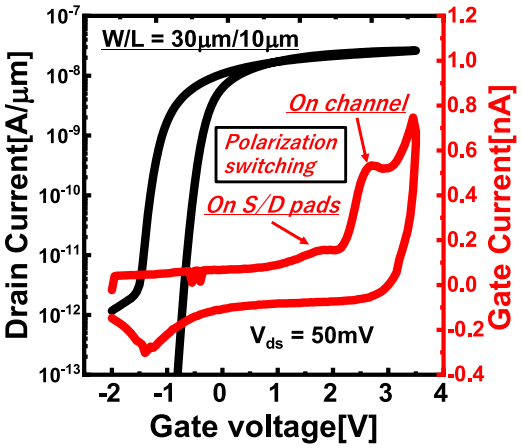

FIGURE 18. Measured $I_d - V_g$ and $I_g - V_g$ curves of the IGZO FeFET in a wide V_g sweep range. Polarization switching on the IGZO channel is observed in I_g.

top-gate potential is fixed. MW is ~0.5V as expected from the simulation results, and erase and program occur, thanks to the fixed body potential by the top gate. The extracted SS is shown in the inset of Fig. 16. Nearly ideal SS is obtained for both erase and program state. At program state, SS is slightly worse than at erase state, which can be due to the interface states. The off current is mainly due to the leakage between the drain pad and the bottom gate. Fig. 17 shows the voltage dependent V_{th} shift after erase/program operation. The program/erase pulse width is 500μs. The gradual V_{th} shift is observed in controlled manner when the erase/program voltage is larger than |2V|.

Polarization switching can be observed in quasi-static I_g measurement for large V_g swing as shown in Fig. 18. Particularly, in positive V_g sweep after erase, two I_g peaks are observed. The first peak in lower V_g corresponds to the polarization switching current between bottom-gate and drain/source pads. The voltage is almost the same as the polarization switching voltage of the metal/HZO/IGZO/metal

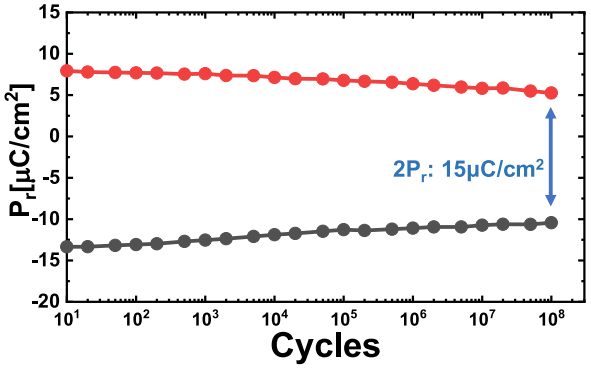

FIGURE 19. Endurance characteristic of the metal/HZO/IGZO/metal capacitor with ±4V/1μs program/erase voltage.

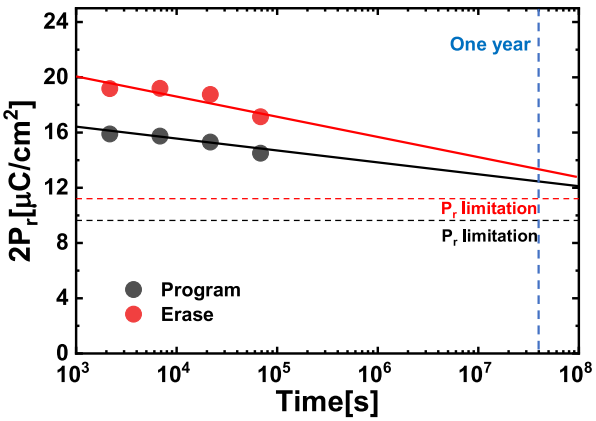

FIGURE 20. Room temperature retention characteristic of the metal/HZO/IGZO/metal capacitor with ±4V program/erase voltage.

capacitor. While the second peak in higher V_g corresponds to the polarization switching current between bottom-gate and the channel. Because the voltage partly drops on SiO_2, the polarization switching voltage of HZO on IGZO channel is higher than on S/D pad. Note that the peak in negative V_g sweep after program is mainly due to the polarization switching between bottom gate and pads. During erase, both depletion layer and SiO_2 capacitances are added to HZO capacitance in series, the total capacitance becomes small, and thus the displacement current is much smaller than that under the pads.

We also studied endurance and retention characteristics. Endurance characteristics of the Al/Ti/IGZO/HZO/TiN stack is shown in Fig. 19. ±4V/1μs pulse is used to program/erase the capacitor. Thanks to the nearly-zero interfacial layer between HZO and IGZO, the capacitor can be programmed and erased up to 10^8 cycles with nearly $2P_r = 15\mu C/cm^2$ without wake-up nor significant degradation. Fig. 20 shows the room temperature retention characteristics. P_r limitation is assumed to be half of remanent polarization. Program/erase voltage is again ±4V. The IGZO capacitor has at least one-year retention at both program and erase state by extrapolating the result of Fig. 20. It should be noted that FeFET reliability characteristics are largely affected by

depolarization field on HZO induced by the IGZO layer, which requires further study in our future work.

V. SUMMARY

We designed and fabricated FE-HfO_2 FET with the ultrathin body IGZO channel. The device shows the ideal SS and high channel mobility, thanks to the junctionless operation and the nearly-zero interfacial layer. IGZO is an effective capping material which helps to form ferroelectric phase. The metal/IGZO/HZO/metal stack capacitor shows clear ferroelectricity. Both endurance and retention characteristics show high reliability. The controllable memory device operation is demonstrated in the IGZO FeFET by fixing the body potential using the top gate. FeFET with ultrathin IGZO body is a promising candidate for high-density memory application.

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