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Low Voltage Operation of IGZO Thin Film Transistors Enabled by Ultrathin Al_2O_3 Gate Dielectric

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An ultrathin, 5 nm, Al_2O_3 film grown by atomic-layer deposition (ALD) was used as a gate dielectric for amorphous indium-gallium-zinc oxide (a-IGZO) thin-film transistors (TFTs). The Al_2O_3 layer showed a low surface roughness of 0.15 nm, a low leakage current and a high breakdown voltage of 6 V. In particular, a very high gate capacitance of 720 nF/cm^2 was achieved, making it possible for the a-IGZO TFTs to not only operate at a low voltage of 1 V, but also exhibit desirable properties including a low threshold voltage of 0.3 V, a small subthreshold swing of 100 mV/decade, and a high on/off current ratio of 1.2×10^7. Furthermore, even under an ultralow operation voltage of 0.6 V, well-behaved transistor characteristics were still observed with an on/off ratio as high as 3×10^6. The electron transport through the Al_2O_3 layer has also been analyzed, indicating the Fowler–Nordheim tunneling mechanism.

Amorphous indium-gallium-zinc oxide (a-IGZO) thin-film transistors (TFTs) have received much attention because of their excellent performance, including high electron mobility, excellent uniformity and stability, optical transparency, and low process temperature.[1-3] As such, a-IGZO TFTs have started replacing amorphous-silicon transistors in large-area displays.[4] A wide variety of applications can also greatly benefit from the ease of deposition of IGZO on flexible substrates, such as wearable electronics[5] and thin-film circuits[6]. These portable electronic products are typically battery hungry, hence making low-voltage operations highly desirable and even necessity. However, most IGZO TFTs reported to date have to be driven by large voltages in order to achieve high mobility and high on/off current ratios.

The simplest method to reduce the operation voltage is reducing the thickness of the gate dielectric layer. However, the thickness reduction of the conventional SiO_2 gate dielectric layer

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is limited since the gate leakage current would become severe when the dielectric is too thin. Many researchers have tried to use high-dielectric-constant (high-k) gate dielectrics to reduce the TFT operation voltage. Various high-k materials, e.g., HfLaO,[7, 8] Ta_2O_5,[9] $BaSrTiO_3$,[10] Y_2O_3,[11] Al_2O_3,[12-16] $HoTiO_3$,[17] $LaLuO_3$,[18] HfO_2,[19, 20] $LaAlO_3$,[21] have been applied because they simultaneously enable a low leakage current and a low-voltage operation. Shao et al reported low-operation-voltage a-IGZO TFTs using a 20 nm HfO_2 gate dielectric layer.[20] Cheng et al. also demonstrated that 15.5 nm $LaAlO_3$ a-IGZO TFTs exhibited excellent electrical performances.[21] In addition to these solid-state dielectrics, ionic liquids such as water have also been used as dielectrics to reduce operation voltage.[22,23] For high- k materials, there is a general phenomenon that the bandgap decreases with the increase of k value.[24] Therefore, a high-quality dielectric film is necessary to avoid a large leakage current. Among the well-known high-k materials, Al_2O_3 has a large band gap (E_g = 8 eV), a high dielectric constant (k = 9.0), a high breakdown field (5–10 MV/cm), strong adhesion to dissimilar materials, and superior thermal and chemical stability.[24] The growth of Al_2O_3 film is usually done using atomic-layer deposition (ALD) technology which allows highly conformal, pinhole-free films with precise thickness control.

In this work, we fabricate a-IGZO TFTs with Al_2O_3 layer grown by ALD as the gate dielectric. The Al_2O_3 films were deposited at 150 ^oC using alternating precursors of trimethyl aluminum [$Al(CH_3)_3$] (TMA) and H_2O vapor at a deposition rate of approximately 0.1 nm per cycle. One deposition cycle of Al_2O_3 consisted of an exposure of TMA for 0.03 s, a purge period with N_2 for 30 s, and an exposure of H_2O vapor for 0.015 s, followed by a final purge period with N_2 for 30 s. Each deposition cycle lasted about 60 s. The carrier gas was N_2 and the pressure in chamber was 0.015 torr during the deposition. A longer purge time than typical ones in the literature was used here to ensure the quality of the very thin Al_2O_3 films. Different thicknesses, 30, 10, and 5 nm, have been experimented to study their effects on a-IGZO TFT operations. We show that even a very thin 5 nm Al_2O_3 film can be a highly reliable dielectric with low leakage. The obtained TFTs exhibit desirable properties for low power operations, including a low threshold voltage (V_T), a high mobility (μ), a small subthreshold swing (SS), and a high on/off current ratio (I_{on}/I_{off}). In particular, we are able to operate our a-IGZO TFTs at an extremely low voltage of 0.6 V. This is the lowest operating voltage reported to date,

which may have implications for thin-film technology based low-power electronics.

The fabricated IGZO TFT structure is shown in Fig. 1(a). Firstly, the Al_2O_3 layer (30, 10, and 5 nm) was grown by ALD on n-type heavily doped Si wafers. Then, a 24-nm IGZO was deposited by radio-frequency (RF) sputtering through a shadow mask at room temperature to form the active layer. A 3-in. circular target was used with In_2O_3:Ga_2O_3:ZnO = 1:1:1 mol. %. During the sputtering, the RF power and Ar pressure were maintained at 90 W and 3.65 mTorr, respectively. Finally, Al source and drain contact electrodes were formed by thermal evaporation through a shadow mask. The active channel length (L) and channel width (W) of the fabricated a-IGZO TFTs are 60 µm and 2000 µm, respectively. Prior to IGZO TFT fabrication, metal-insulator-semiconductor ($Al/Al_2O_3/n$-Si) capacitors were made to investigate the capacitance of the gate dielectric. These devices were characterized by current-voltage (I-V) and capacitance-voltage (C-V) measurements using the Agilent B2900 Precision Source/Measure Unit (SMU) and E4980A Precision LCR Meter. To further ensure the quality of Al_2O_3 layer, the surface morphology of the Al_2O_3 film was investigated by atomic-force microscopy (AFM).

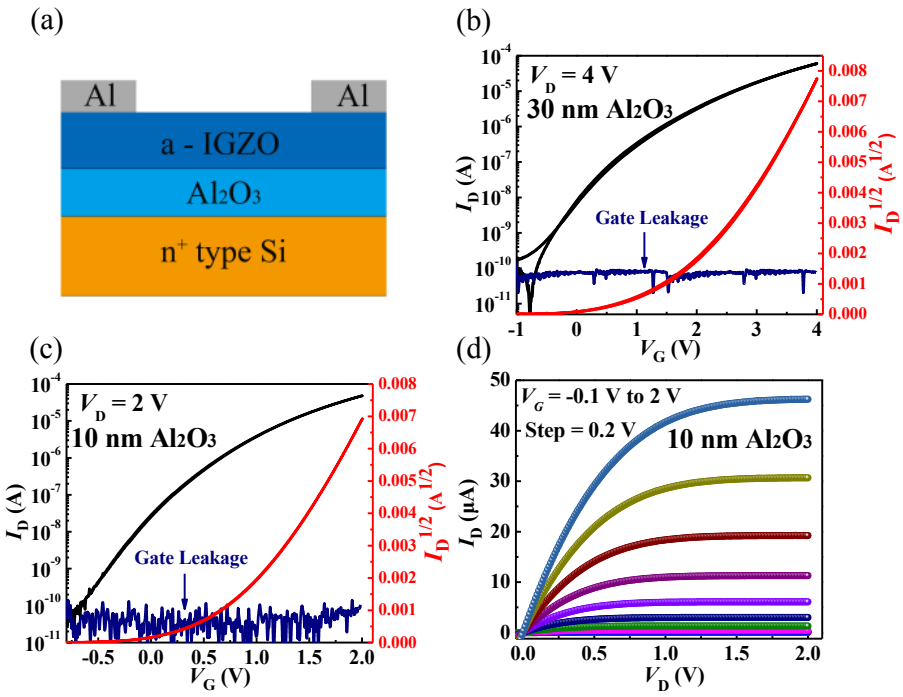

Fig. 1. (a) Schematic cross-sectional view of the a-IGZO TFTs. Transfer characteristics of a-IGZO TFTs with 30 nm (b), and 10 nm (c) Al_2O_3 gate dielectrics. Output (d) characteristic of an a-IGZO TFT with 10 nm Al_2O_3 gate dielectrics.

Figures 1(b) and (c) show the transfer characteristics of a-IGZO TFTs with 30 nm and 10

nm Al_2O_3 gate dielectrics, respectively. After 150 °C thermal annealing in air for 1 h, very little hysteresis is observed in drain current versus gate voltage (I_D–V_G) curves. This indicates that no significant mobile bulk oxide charge is present and that the density of slow interface traps is very low, suggesting a high quality of Al_2O_3 dielectrics.[21] Figure 1(d) shows the output characteristics of an a-IGZO TFT with a 10 nm Al_2O_3 gate dielectric, exhibiting a well-defined pinch-off behavior. When the Al_2O_3 thickness was decreased from 30 to 10 nm, V_T decreased from 1.9 to 0.8 V, and *SS* decreased from 0.39 to 0.26 V/decade. The lower *SS* value in the 10 nm Al_2O_3 TFT is a result of the increased gate capacitance. The gate leakage of the Al_2O_3 gate dielectric is below 1×10^{-8} A/cm^2, which is among the lowest in reported high-*k* dielectric based TFTs.[8, 12, 18, 21] Importantly, with the decrease of the Al_2O_3 thickness, the operation voltage reduces from 4 V to 2 V.

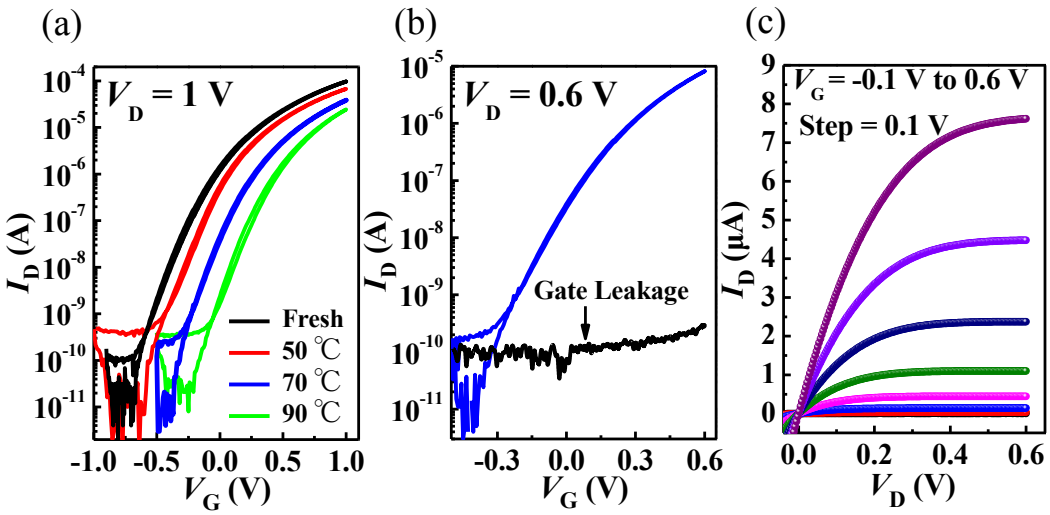

Fig. 2. (a) Transfer characteristics of devices after 1 h thermal annealing with different temperatures. Transfer (b) and output (c) characteristics of a-IGZO TFTs with 5 nm Al_2O_3 gate dielectric layer under 0.6 V operation voltage.

Given that the gate leakage current remained low as shown in both Figs. 1(b) and (c), we have explored the possibility to further reduce the Al_2O_3 dielectric thickness to 5 nm in order to reduce the operation voltage to 1 V. The as-fabricated devices with 5 nm Al_2O_3 and 10 nm a-IGZO indeed operated under 1 V with a large on/off ratio well beyond 10^6 as shown in Fig. 2(a). However, the device needs to be turned off at a gate voltage of - 0.7 V. Unlike Al_2O_3 which was deposited chemically by ALD, sputtered films often have unbalanced stoichiometry due to the high-energy ion bombardment. In the case of oxide deposition, it is common for the sputtered film to contain a large number of oxygen vacancies, resulting in a rather conductive

film. Thermal annealing in air is an effective method to reduce such vacancies.[??] With increase of the annealing temperature, V_T was found to shift in the positive direction (0 V → 0.1 V → 0.3 V → 0.4 V) as shown in Fig. 2(a). To maintain a good carrier mobility and high on/off ratio, we choose 70 °C as the optimum annealing temperature.

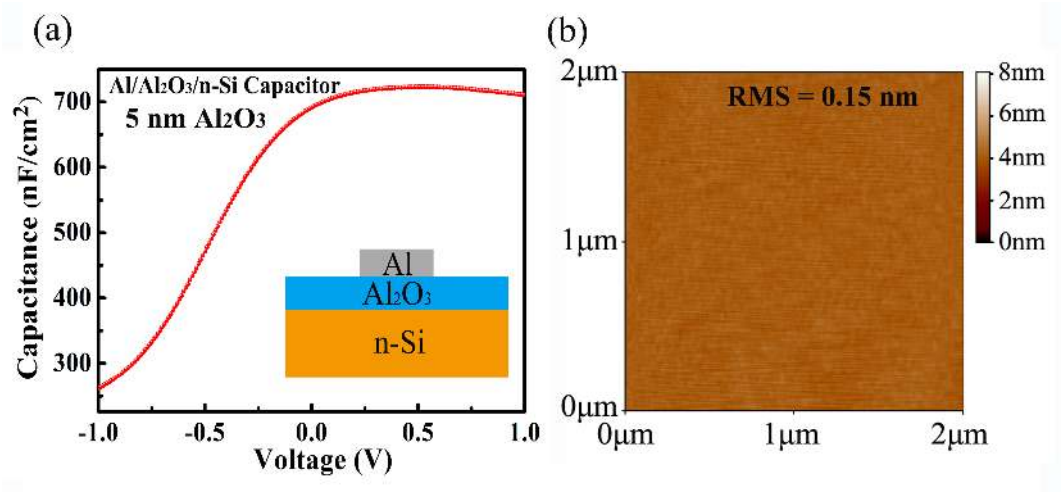

Fig. 3. (a) *C-V* characteristics (main graph) and schematic diagram (inset) of an Al/Al_2O_3(5 nm)/n-Si MOS capacitor. (b) AFM image of 5 nm Al_2O_3 film.

Very thin gate dielectrics have been found to show different dielectric properties from thick ones.[25, 26] To make our calculation of carrier mobility accurate, metal-insulator-semiconductor capacitors were made to determine the capacitance of the gate dielectric (C_{ox}). Figure 3(a) and the inset show the *C-V* characteristics and schematic diagram of an Al/Al_2O_3 (5 nm)/n-Si capacitor, respectively. A very high capacitance of C_{ox} = 720 nF/cm^2 is determined, which is equivalent to the capacitance of a 3.3 nm standard SiO_2 dielectric. The latter, however, would be much more susceptible to leakage current. The surface morphology of the 5 nm Al_2O_3 dielectric film was also studied by AFM, showing a very low root-mean-square (RMS) roughness of 0.15 nm in Fig. 3(b), smaller than the roughness of thicker films which are 0.25 and 0.28 nm for 10 nm and 30 nm Al_2O_3, respectively. The interface trap density is known to directly associate with interface roughness between IGZO and gate dielectric. The quality of gate dielectric can also be manifested by the TFT subthreshold swing. Under 1 V operation voltage, the 5 nm Al_2O_3 based device exhibits a very low *SS* of 100 mV/decade, which is quiet desirable in order to turn on the transistor effectively at a low power. Furthermore, a low V_T of 0.3 V and a high mobility μ of 6.3 cm^2/Vs were achieved. The extremely small hysteresis indicates very low density of trapping states (N_t) at the gate dielectric interface, which also

correlates well with the low Al_2O_3 surface roughness. The value of N_t can be determinate by:

$$SS = \frac{k_B T \ln 10}{q}\left[1 + \frac{q^2}{C_{ox}} N_t\right] \quad (1)$$

where k_B is Boltzmann's constant, T is the temperature in Kelvin, and q is the electron charge. Taking the SS value of the 5 nm Al_2O_3 IGZO TFTs, the interface trap density N_t is found to be 3.0×10^{12} $eV^{-1}cm^{-2}$, which is among the lowest values in reported Al_2O_3 TFTs to date.[27]

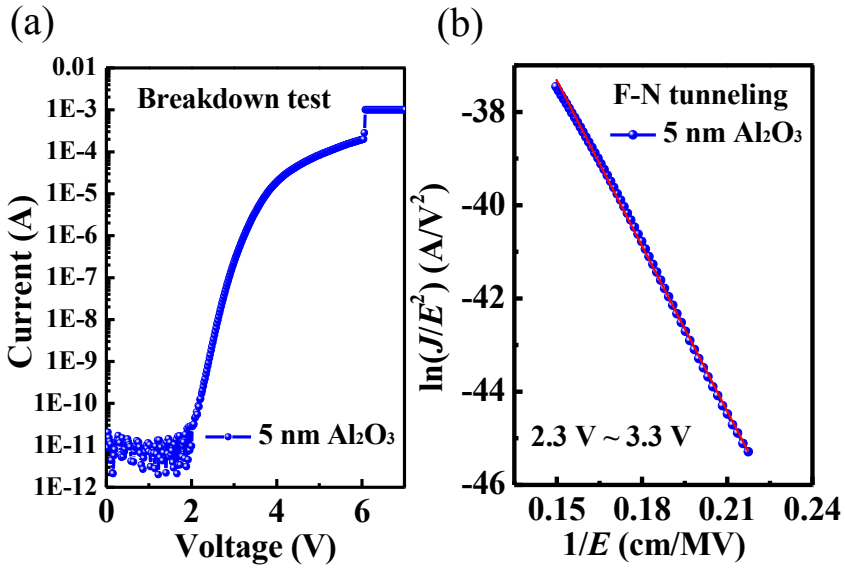

Fig. 4. (a) Breakdown tests for Al/Al_2O_3/n-Si MOS devices with 5 nm Al_2O_3 layer. (b)The liner fitting for leakage current of 5 nm Al_2O_3 layer by F-N tunneling model.

To test the robustness of the 5-nm-thin Al_2O_3 and study the vertical carrier transport mechanism (related to leakage current), we applied large voltages to the metal-insulator-semiconductor capacitors. It is quite surprising to discover that the breakdown voltage of 5 nm Al_2O_3 is as high as about 6 V as shown in Fig.4 (a). This again confirms the high quality of the 5 nm Al_2O_3 dielectric film. There are a few possible electron transport mechanisms including direct tunneling, Fowler–Nordheim (F-N) tunneling, Poole-Frenkel emission, and Schottky emission, etc. The F-N tunneling current is given by

$$\frac{J}{E^2} = C_1 e^{-C_2/E} \quad (2)$$

where J is the current density and E is the electric field across the oxide. C_1 and C_2 are given by

$$C_1 = q^3 m / 16\pi^2 \hbar m_{ox} \emptyset_o \quad (3)$$

$$C_2 = \frac{4}{3}\frac{(2m_{ox})^{1/2}}{q\hbar}\emptyset_o^{\frac{3}{2}} \quad (4)$$

where q is the electron charge, m and m_{ox} are the electron mass in free space and in the oxide respectively, $2\pi\hbar$ is Planck's constant, and $\emptyset_o$ is the barrier height. Figure 4 (b) show a liner fitting of the leakage current according to Eq. 2. The dotted line is the experiment result and the red solid line is the fitting. Other transport models do not provide such a good agreement. The fitting in Fig. 4(b) hence indicates that the vertical transport mechanism in our thin Al_2O_3 dielectrics is F-N tunneling.

We also further tested the TFTs based on 5 nm Al_2O_3 under lower operation voltages. Even under a 0.6 V bias, a high I_{on}/I_{off} ratio and well behaved transistor output characteristics were achieved, as shown in transfer and output characteristics in Figs. 2(b) and (c). The mobility is 3.8 cm^2/Vs, somewhat lower than that at 1 V (6.3 cm^2/Vs). This is not unusual because carrier trapping by interface states becomes more dominated at low gate voltages. Importantly, even under such low operation voltage, the on current is still about 5 orders of magnitude higher than the leakage current. In Table I, we have compared the key device parameters of our a-IGZO TFTs with previously reported devices, where T_{ox} is the thickness of gate dielectrics and V_{ON} represents the operation voltage. Our devices show the lowest operating voltages in oxide semiconductor TFTs, which is favorable for low-power electronics applications.

TABLE I. Comparison of a-IGZO TFTs with different gate dielectrics

Gate dielectrics	T_{ox} **(nm)**	V_{ON} **(V)**	V_T **(V)**	***SS*** **(mV/dec)**	μ **(cm^2/Vs)**	I_{on}/I_{off}
HfLaO[7]	300	2	0.2	76	25	5×10^7
Ta_2O_5[9]	200	3	0.3	610	61.5	1×10^5
$BaSrTiO_3$[10]	170	3	0.5	60	10	8×10^7
Y_2O_3[11]	140	6	1.4	200	12	1×10^8
Al_2O_3[12]	100	5	0.4	100	8	6×10^7
HfO_2[19]	60	0.8	0.2	90	5.9	2.4×10^7
$HoTiO_3$[17]	60	8	0.1	160	21.4	1.3×10^8
HfLaO[8]	40	1.5	0.1	180	22.1	2×10^5
$LaLuO_3$[18]	20	2	0.3	310	6.6	1×10^3
HfO_2[20]	20	2	0.2	109	8.1	1×10^7
$LaAlO_3$[21]	15.5	1.4	0.4	68	4.1	1×10^5
(This work)	**5**	**0.6**	**0.2**	**100**	**3.8**	$\mathbf{3 \times 10^6}$
Al_2O_3	**5**	**1**	**0.3**	**100**	**6.3**	$\mathbf{1.2 \times 10^7}$

In summary, a-IGZO TFTs with an ultrathin 5 nm Al_2O_3 layer have been demonstrated to be

capable of operating not only at 1 V but also at 0.6 V. Importantly, the TFTs exhibit desirable properties despite the low driving voltages, including a steep subthreshold slope, negligible hysteresis, and high I_{on}/I_{off} ratio. We also discovered that the breakdown voltage of the 5 nm-thin Al_2O_3 film is as high as 6 V and the electron transport mechanism through the Al_2O_3 layer has been analyzed. The results indicate that our low-voltage-driven a-IGZO TFTs may have a great promise for future low-power electronics applications.

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References

[1]B. Zhang, H. Li, X. Zhang, Y. Luo, Q. Wang, and A. Song, Appl. Phys. Lett. 106, 093506 (2015).

[2]L. Du, H. Li, L. Yan, J. Zhang, Q. Xin, Q. Wang, and A. Song, Appl. Phys. Lett. 110, 011602 (2017).

[3]Q. Xin, L. Yan, L. Du, J. Zhang, Y. Luo, Q. Wang, and A. Song, Thin Solid Films 616, 569-572 (2016).

[4]K. Fukuda, Y. Takeda, Y. Yoshimura, R. Shiwaku, L. T. Tran, T. Sekine, M. Mizukami, D. Kumaki, and S. Tokito, Nat. Commun.5, 8 (2014).

[5]Y. S. Rim, S.-H. Bae, H. Chen, N. De Marco, and Y. Yang, Adv. Mater. 28, 4415-4440 (2016).

[6]J. I. Leon, S. Kouro, L. G. Franquelo, J. Rodriguez, and B. Wu, IEEE Trans. Electron Devices 63, 2688-2701 (2016).

[7]N. C. Su, S. J. Wang, and A. Chin, IEEE Electron Device Lett. 30, 1317-1319 (2009).

[8]S. Nai-Chao, W. Shui-Jinn, H. Chin-Chuan, C. Yu-Han, H. Hao-Yuan, C. Chen-Kuo, and A. Chin, IEEE Electron Device Lett. 31, 680-682 (2010).

[9]C. J. Chiu, S. P. Chang, and S. J. Chang, IEEE Electron Device Lett. 31, 1245-1247 (2010).

[10]J. B. Kim, C. Fuentes-Hernandez, and B. Kippelen, Appl. Phys. Lett. 93, 242111 (2008).

[11]H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, Appl. Phys. Lett. 89, 112123 (2006).

[12]J. B. Kim, C. Fuentes-Hernandez, W. J. Potscavage, X. H. Zhang, and B. Kippelen, Appl. Phys. Lett. 94, 142107 (2009).

[13]A. Suresh, P. Wellenius, V. Baliga, H. Luo, L.M. Lunardi, and J.F. Muth, IEEE Electron Device Lett. 31,317-319 (2010).

[14]C.H. Wu, K.M. Chang, S.H Huang, I.C. Deng, C.J. Wu, W.H. Chiang, and C.C. Chang, IEEE Electron Device Lett. 33, 552-554 (2012).

[15]C.R. Park, J.H. Hwang, Ceramics International. 40, 12917–12922 (2014).

[16]X.W Ding, H. Zhang, J.H. Zhang, J. Li, W.M. Shi, X.Y. Jiang, Z.L. Zhang, Materials Science in Semiconductor Processing. 29, 69–75 (2015).

[17]T.-M. Pan, C.-H. Chen, J.-H. Liu, J.-L. Her, and K. Koyama, IEEE Electron Device Lett. 35, 66-68 (2014).

[18]I.C. Kun, H. Hsiao-Hsuan, C. Chun-Hu, L. Kai-Yu, L. Shang-Rong, and A. Chin, IEEE Electron Devices and Solid-State Circuits. 1-2, (2013).

[19]C. H. Lu, T. H. Hou, and T. M. Pan, IEEE Trans. Electron Devices. 63, 5060-5063 (2016).

[20]Y. Shao, X. Xiao, X. He, W. Deng, and S. D. Zhang, IEEE Electron Device Lett. 36, 573-575 (2015).

[21]C. H. Cheng, K. I. Chou, and H. H. Hsu, Journal of Nanoscience and Nanotechnology. 15, 1486-1489 (2015).

[22]Y. Huang, E. Sutter, J.T. Sadowski, M. Cotlet, O.L.A. Monti, D.A. Racke, M.R. Neupane, D. Wickramaratne, R.K. Lake, P. Sutter, et al. ACS Nano. 8, 10743–10755 (2014).

[23]Y. Huang, J.S. Qiao, K. He, S. Bliznakov, E. Sutter, X.J. Chen, D. Luo, F.K. Meng, D. Su, P. Sutter, et al. Chem. Mater. 28, 8330−8339 (2016).

[24]J. Robertson, R.M. Wallace, Mater. Sci. Eng. R, 88 (12), 1-41 (2015).

[25]M.D. Gronera, J.W. Elama, F.H. Fabreguettea, S.M. Georgea, Thin Solid Films, 413, 186–

197 (2002).

[26]A. Daus, C. Vogt, N. Münzenrieder, L. Petti, S. Knobelspies, G. Cantarella, M. Luisier, G.A. Salvatore, and G. Tröster, IEEE Trans. Electron Devices. 64, 2789-2796 (2017).

[27]X. Ding, J. Zhang, W. Shi, H. Ding, H. Zhang, J. Li, X. Jiang, Z. Zhang, and C. Fu, Mater. Sci. Semicond. Process. 29, 326-330 (2015).