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Low Voltage Ride Through Capability of a 5 kW Grid-Tied Solar Inverter

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***Abstract*— Distributed power generation systems (DPGS) such as wind and solar become more and more widely spread. As a consequence grid operating companies demand system services. As part of the general fault ride through (FRT) requirements this paper deals with low voltage ride through (LVRT) capability of a three-phase-four-wire grid-tied solar inverter. The standard system will be described and necessary changes to the control such as positive (PS), negative (NS) and zero sequence (ZS) separation, a stable phase-locked-loop (PLL) as well as voltage support by means of reactive current as well as stress factors to the hardware will be identified.**

***Keywords*— Low Voltage Ride Through, LVRT, Fault Ride Through, FRT, Photovoltaik, PV, Solar Inverter, Power Quality, Grid Codes, P+Resonant, P-Resonant, dq0, 3 phase 4 wire, three-phase-four-wire**

I. Introduction

With increasing penetration of renewable energies more and more participation on power quality is required in countries like USA, Canada, France, Spain, Germany and Denmark according to [1]. With much bigger proportion one important feature for wind turbines already is the low voltage ride through (LVRT) capability bringing along challenges. Photovoltaic (PV) systems, mostly evolving from single phase applications connected to the low voltage (LV) grid the most attention was paid to maximum power point (MPP) tracking, maximization of active current due to the individual feed in tariff and strict disconnection in any kind of grid faults following interconnection standards such as IEEE 1547, UL 1741, G83/1 or VDE 0126-1-1 along with national regulations. The overall amount of distributed power generation systems (DPGS) for renewable energy is rapidly increasing. Besides large wind systems not only small PV systems are highly requested but also larger systems of multi MW size either built from central inverters or from a sum of string inverters. With increasing plant size more often connected to the medium voltage (MV) grid and thereby highly increased installed power also PV system starting to have en effect on power quality. As a consequence the interconnection requirements start changing rapidly, requiring participation on system services. Therefore and due to the differences of renewable energies the specific behaviour of solar inverters will be investigated. The paper is structured as following: In section II power quality and the requirements on grid interconnetion are presented. In the following section the system is described. In sections IV, V and VI the theoretical background is absorbed, simulations are investigated and experimental results are presented. In the last section there is a conclusion.

II. Power Quality and Grid Interconnection

Power quality is a widely spread area and therefore effected by a variety of phenomena [2]. Beyond that it can be seen directly related to voltage and by ohmic law to current quality. EN 50160 [3] is the central European reference defining the voltage quality to the consumer. Voltage quality can among others be defined by the Total Harmonic Distortion (THD) and the Voltage Unbalance Factor (VUF). According to the newest version of [3] the voltage THD shall be less than 8% and the VUF less than 2% to 3%. The THD is not directly affected by grid unbalance and according to [3] it is defined as the square root of the sum of the harmonics X_h divided by the fundamental X_1:

$$THD = \frac{\sqrt{\sum_{h=2}^{n=40} X_h^2}}{X_1} \tag{1}$$

Whereas the VUF is directly related to unbalances in the voltage. The definition from [3] calculates the ratio of Negative Sequence (NS) to Positive Sequence (PS) from phase to phase voltages. Following [3] unbalance regarding the Zero Sequence (ZS) is not considered relevant for the possible interference of appliances connected to the grid and thereby no limits are defined.

$$VUF = \frac{|U^-|}{|U^+|} = \sqrt{\frac{6 \cdot (U_{ab}^2 + U_{bc}^2 + U_{ca}^2)}{(U_{ab} + U_{bc} + U_{ca})^2} - 2} \tag{2}$$

It is further stated that transient grid failures can occur up to 1000 times a year. To avoid misunderstandings, it has to be cleared out that [3] does not include limits for emission of harmonics or unbalance but instead values of what can be expected from the grid. Current quality is not defined for faulty grid conditions yet and will therefore not be considered in the following. The national grid codes went rapidly through a change of paradigma, coming from disconnection in case of any grid failure and a maximized active power delivery to sharing reactive power for voltage support i.e. by a constant $cos(\varphi)$ different to 1 and even grid support in case of transient failures.

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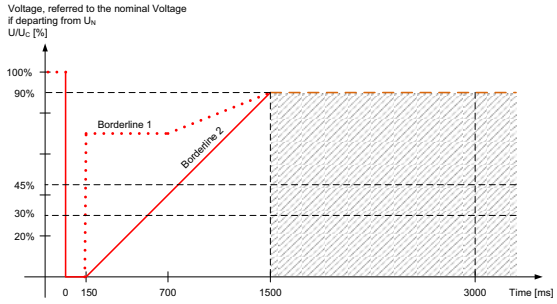

Fig. 1. Borderlines for voltage support

As described in [1] and [4] most grid codes do not define requirements for voltage support. Unlike the German grid codes for high [5], for medium [6] and in future also for low voltage level. As described in [4] they also include highest requirements for DPGS. Therefore they are taken as representative for advanced grid integration of DPGS. The grid codes include measurements for voltage support. Figure 1 combines the high and medium voltage level requirements in strongest interpretation. As stated in [5], [6] and [7] grid faults with a remaining voltage above borderline 1 shall not lead to tripping DPGS. Beneath borderline 1 but above borderline 2 temporary disconnection with defined resynchronization cycles are partly accepted. Below borderline 2 and up to 1500 ms DGPS are allowed to disconnect with longer resynchronization cycles. After 1500 ms DGPS have to disconnect. Fig. 2 shows the required reactive current during transient grid faults. The slope k of the characteristic and the dead-band can vary, comparing [5], [6] and [7]. The figure also includes reference to a high voltage ride through (HVRT) which occurs according to [2] much less than the here discussed LVRT. As described, the grid codes require special behavior of the DPGS in case of faulty grids. The German requirements for reactive current i_R^* for voltage support can be described as:

$$i_R^* = k \cdot \frac{U}{U_N} \cdot I_N \tag{3}$$

Thereby the typical value of $k = 2$ is given. Following [5] and [6] the reactive current needs to be delivered within 20 ms after failure occurence. As more detailed described

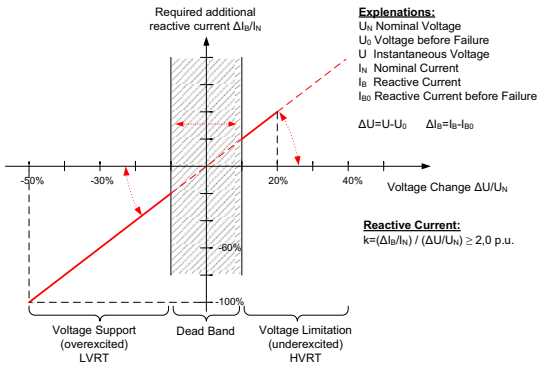

Fig. 2. Required reactive current for voltage support

for wind systems in [7] which refers to [8] giving detailed describtion for certification purposes the time of 20 ms can be complied with if the step response of the reactive current has a peak time of 60 ms and a settling time, definied as staying within the tolerance band of 90% to 120% of the set-point, of 80 ms. Further [8] requires the orientation of the reactive current on the positive sequence (PS) of the voltage.

III. System Description

The system consists of a PV array with the IV characteristic given in fig. 3. It shows a typical and for the following simulations used I/V characteristic of a solar system. The maximum power point (MPP) at standard test conditions (STC) is chosen to 700 V at a rated current of 7.25 A leading to a power of 5 kW. The system voltage U_{oc} is chosen as state of the art to 1000 V with a short-circuit current I_{sc} of 9.15 A. Originating from the diode equation, the short-circuit current is mostly related to the irradiation whereas the open-circuit voltage is highly related to the temperature expressed through the coefficient a_T measured in $[V/°]$.

$$U_{oc,x°} = U_{oc,25°} \cdot a_T \cdot (T_{x°} - T_{25°}) \tag{4}$$

The variable output voltage of the PV array is fed to the grid by the inverter topology given in fig. 4. It consists of a voltage source inverter and a boost converter in the DC link to cover the whole voltage range of the solar array under different environmental conditions. The connection to the grid is realized via an LCL filter [9]. Special about this topology is the fourth wire that connects the midpoint of the split DC capacitors C_{DC} that have an overall size of 660 μF with the neutral phase of the grid. The advantage of the fourth wire is a great reduction of the leakage current through the parasitic capacitance C_{PV} at the PV array that arises due to the variation of the DC link potential to ground generated by the switching pattern as described in [10]. The disadvantage is the higher DC link voltage V_{DC} needed for normal operation.

IV. Background

As mentioned above precise characterization of the voltage is the key to implement fault ride through (FRT) capability. The following chapter will describe the used methods to characterize the voltage as well as the used

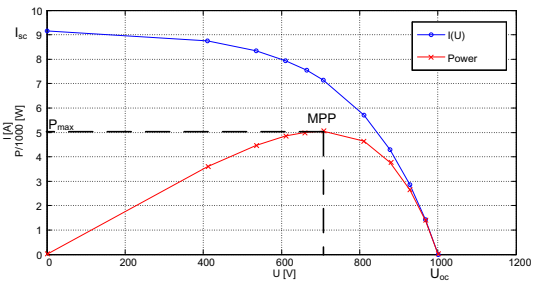

Fig. 3. I/V characteristic of solar system at STC (temperature of 25° C, spectrum of light equals 1.5 air mass, irradiation 1000 W/m^2)

control structure. Starting with the controller itself, taking a stable Phase-Locked-Loop (PLL) into consideration and showing different methods for sequence separation and the chosen detection method for voltage dips and swells it leads to the necessary design.

A. P+Resonant Controller

The often used PI controller shown in eq. (5) perfectly controls DC signals. Therefore the standard approach to control three phase systems is using dq transformations to transform the signal into DC.

$$G_{PI} = K_P + K_{I,PI} \cdot \frac{1}{s} \tag{5}$$

By contrast the resonant controller can track sinusoidal signals having an infinit gain at its resonance frequency as described among others in [10] and [11].

$$G_{PR} = K_P + K_{I,PR} \cdot \frac{s}{s^2 + \omega^2} \tag{6}$$

Following [12] the connection between both types of controller can be shown using a lowpass-bandpass-tranformation described in eq. (7) by which the transformation from PI (5) to PR (6) can be achieved. Attention has to be paid to the factor of 2 resulting in a the redefinition $K_{I,PR} = 2 \cdot K_{I,PI}$ In this case not the signal is transformed but instead the controller.

$$s \rightleftharpoons \frac{s^2 + \omega^2}{2 \cdot s} \tag{7}$$

B. Phase Lock Loop

Faulty grids and unsymmetrical conditions can lead to failing PLL behaviour. In [13] PLL behavior within faulty grid conditions is studied. For synchronization purposes a dq-PLL is used. It is based on Park's dq-transformation and will therefore be affected by unsymmetrical grid conditions. The sequence separation method will be used as a pre-filter to give only the PS onto the PLL. This carries out two tasks simultaneously: First it stabilizes the PLL within unsymmetrical conditions as illustrated in fig. 5 and fig. 6 from $t = 0.05\ s$. Second it ensures the required orientation of the current.

C. Dip Detection and Sequence Separation Methods

Two different approaches of dip detection and thereby calculating the required reactive current have been studied. The grid code compliant root mean square (RMS) method is based on calculating the voltages between

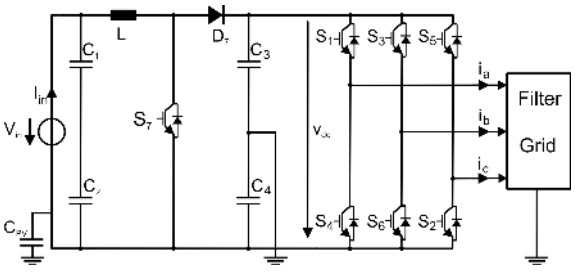

Fig. 4. Solar inverter with earthed dc link midpoint

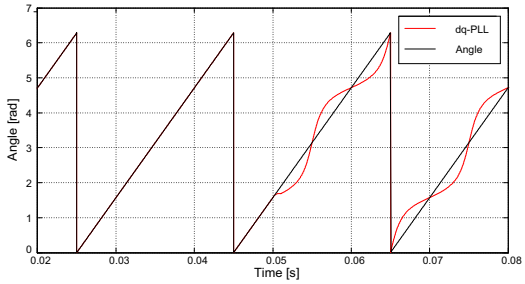

Fig. 5. Comparison of standard PLL Performance

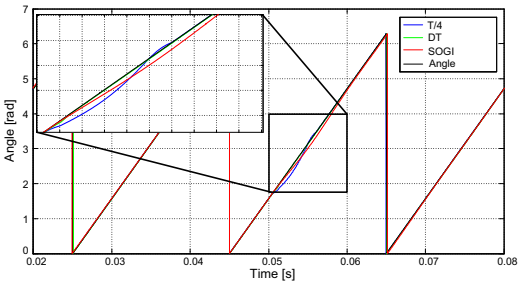

Fig. 6. Comparison of PLL Performance with pre-filter

phases. By calculating the RMS value over half a period T for each phase detection of the phase to phase (p2p) voltage drop can be determined.

$$x_{p2p,RMS} = \sqrt{\frac{2}{T} \cdot \int_{t_0}^{t_0+T/2} x_{p2p}^2(t)\mathrm{d}t} \tag{8}$$

Through sequence separation also the change of PS could be taken for detection purposes, resulting in slightly different results from the RMS method under unsymmetrical conditions. As already discussed in [14], [15] and [16] different methods for sequence separation can be found for three-phase-systems. They differ mainly in stability against harmonics and noise as well as detection speed. Based on Clark's $\alpha\beta 0$ transformation the zero sequence (ZS) is separated, so that only positive (PS) and negative sequence (NS) remain within the signal. Hereby the methods become also applicable to three-phase-four wire systems as described above. As described in [14] PS (+) as well as NS (-) can be isolated in $\alpha\beta$ coordinates by smartly setting the signals against their orthogonal components. Common goal of the three separation methods is the creation of the orthogonal component. The T/4 method delays a signal to itself by one fourth of a period and provides thereby cancelling capability for periodic signals. To the same time it reduces accuracy with noise signals. By using the following equations the PS and NS can be obtained.

$$\underline{x}^{+}_{\alpha\beta,T/4} = \frac{1}{2} \cdot \left(x_{\alpha\beta}(t) + j x_{\alpha\beta}\left(t - \frac{T}{4}\right)\right) \tag{9}$$

$$\underline{x}^{-}_{\alpha\beta,T/4} = \frac{1}{2} \cdot \left(x_{\alpha\beta}(t) - j x_{\alpha\beta}\left(t - \frac{T}{4}\right)\right) \tag{10}$$

The differentiation method (DT) has been studied in [15]. It creates the orthogonal component by differentiating the

signal what makes it very sensible to harmonics.

$$\underline{x}^{+}_{\alpha\beta,DT} = \frac{1}{2} \cdot \left(x_{\alpha\beta}(t - T_S) + j \left(-\frac{1}{\omega_0} \right) \frac{\mathrm{d}}{\mathrm{d}t} x_{\alpha\beta}(t) \right) \quad (11)$$

$$\underline{x}^{-}_{\alpha\beta,DT} = \frac{1}{2} \cdot \left(x_{\alpha\beta}(t - T_S) - j \left(-\frac{1}{\omega_0} \right) \frac{\mathrm{d}}{\mathrm{d}t} x_{\alpha\beta}(t) \right) \quad (12)$$

As stated in [14] and [17] the orthogonal component can also be created by using a second-order-generalized-integrator (SOGI) whereas the operator $q = e^{-j\frac{\pi}{2}}$.

$$\underline{x}^{+}_{\alpha\beta,SOGI} = \frac{1}{2} \cdot \begin{pmatrix} 1 & -q \\ q & 1 \end{pmatrix} \cdot \underline{x}_{\alpha\beta} \quad (13)$$

$$\underline{x}^{-}_{\alpha\beta,SOGI} = \frac{1}{2} \cdot \begin{pmatrix} 1 & q \\ -q & 1 \end{pmatrix} \cdot \underline{x}_{\alpha\beta} \quad (14)$$

In both of the following cases a symmetrical fault (a=b=c=50%) was applied. Fig. 7 shows the performance of three sequence separation methods also for dip/swell detection and the pure detection method of RMS under ideal conditions whereas fig. 8 shows the behavior under grid conditions with a THD of 5%. It can be observed that T/4 method does have discontinuities depending on the amplitude of the original wave at failure start. While oscillating with 50 V the differentiation method as the fastest method shows highly unsatisfying results under harmonic distorted conditions. SOGI is the slowest but most stable method also under noisy and harmonic distorted conditions. Both, T/4 and SOGI are usable for sequence separation and thereby for dip detection by means of PS change. The RMS dip detection method detects all kind of dips as well as swells with high accuracy in standard time of half a period. In the following the dip and swell detection will be performed by RMS method in compliance with the grid codes.

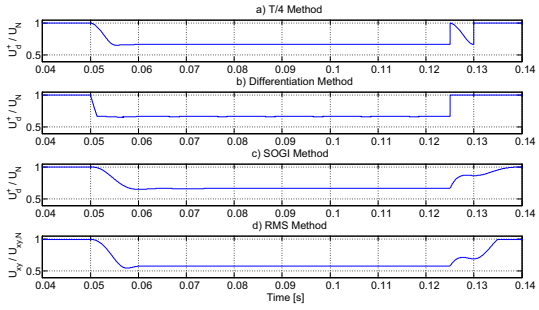

Fig. 7. Detection methods under unsymmetrical grid fault

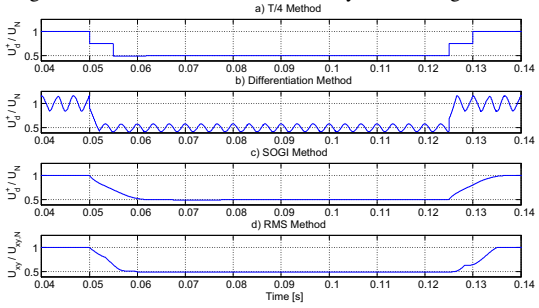

Fig. 8. Detection methods under symmetrical grid fault with harmonics (THD=5%)

D. Control Structure

A cascaded control structure as shown in fig. 9 was chosen. Sequence separation is performed on sampled grid voltages by use of the SOGI method. Because of stability problems with harmonics as shown above the differentiation method will be neglected, although it is the fastest of the investigated methods. The often stated T/4 is fast but shows only advantages with periodic signals. So noise and partly harmonics corrupt performance. The separated PS is given onto the PLL for synchronization and stabilization purposes as well as for orientation of the reactive current during faulty grid conditions. Two current limitations are implemented. First after the DC-Link controller limiting the active reference to the rated current and second after the reference calculation limiting the vector sum of the currents again to the rated current. The DC-Link controller generates the active reference current $i^*_{d,DC}$ under normal grid conditions. The reference calculation generates the active i^*_d and the reactive i^*_q (including LCL filter comensation) [18] reference current for the under laid P+Resonant controllers. To improve the dynamics of the control loop a feed-forward of the grid voltage is implemented and placed before generating the PWM pattern. Fig. 10 illustrates the performance without grid voltage feed-forward. A voltage dip (a=50%, b=c=100%) is applied on the shown phase, resulting in an increasing inverter output current (blue). The reference current (green) is met by the inverter output current after 14 ms. Whereas fig. 11 shows the improved bahaviour including the feed-forward for the same voltage dip, enabling the control to be fast enough to meet the requirements for reactive current delivery as discussed above as well as protecting the hardware from overcurrent.

V. Simulation Results

The following simulations show different voltage dips under precondition of a voltage fall and rise time of

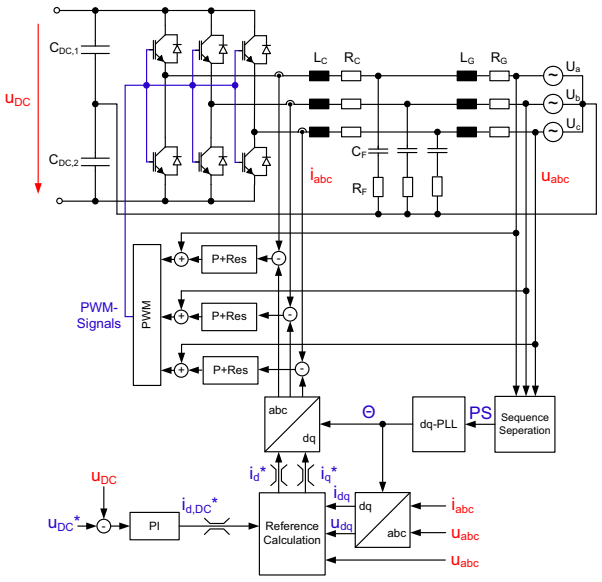

Fig. 9. Control Structure

1 ms to take cable length and transformation from higher grid voltage levels into consideration. The described PV characteristic shown in fig. 3 was chosen in a way that the booster could be deactived for all simulations to represent a basic solar inverter. Fig. 12 illustrates in a) a symmetrical dip (a=b=c=50%) that occurs at 100 ms and lasts for 75 ms. The collapsing phases carry an increase of the currents as seen in b) because of the changed voltage slope. Further the DC link voltage c) has a dip at failure start and end because of a varying power transfer before the DC link controller has adapted. The related active power P and reactive power Q is shown in d). It can be seen that the inverters can handle symmetrical grid faults with a standard control, as long as the grid currents are limited. Fig. 13 illustrates simulations results from an unsymmetrical failure of the same time span. Highly distorted and excessive grid currents in b), swinging active and reactive power transfer in d) and by that a swinging DC link in c) are the upcoming side effects. Neglecting possible hardware issues at high DC voltages as first sub conclusion it can be stated that solar inverters with line current limitation are capable of symmetrical grid faults. Second they are not necessarily capable of unsymmetrical grid failures with a standard control loop, mainly depending on the used PLL. Further in both of the standard scenarios the inverter does not deliver the required reactive current for voltage support. Therefore the advanced control loop as described above was developed. Its performance under unsymmetrical transient grid conditions (a=b=100%, c=0%) is shown in fig. 14. The expected behavior of active and reactive power by means of swinging can be influenced by control strategies as studied in [14]. Each optimization carries a compromise with its related side effects. The implementation of such strategies seems not to be necessary referring to no written requirements in the grid codes regarding balanced or unbalanced currents to the time being and will therefore be neglected. Reactive current is fed into the grid as it can be seen from the reactive power signal Q in d). Using this control both powers are swinging, which could on the one hand effect the lifetime of the DC link capacitors regarding the active power but on the other hand this keeps the THD lower. As studied in [14] the more constant the powers become the more distorded become the grid currents. Due to the increase of reactive current and the

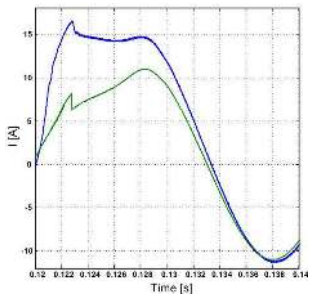

Fig. 10. Control without grid voltage feed-forward

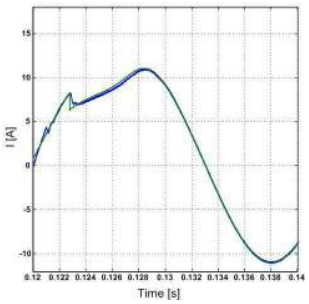

Fig. 11. Control with grid voltage feed-forward

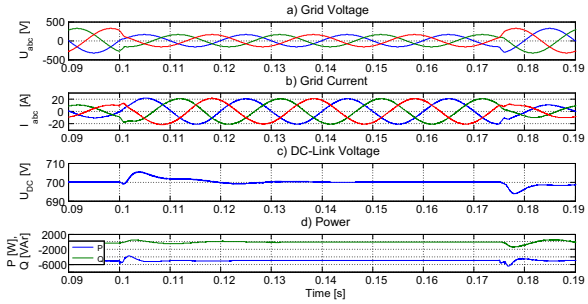

Fig. 12. Symmetrical LVRT with standard control

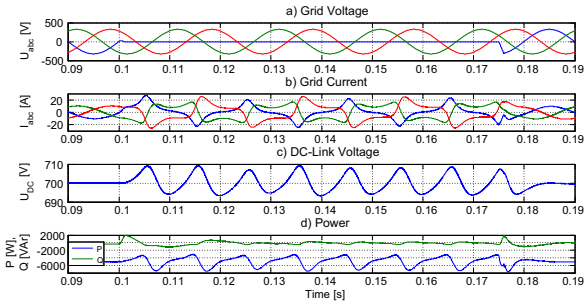

Fig. 13. Unsymmetrical LVRT with standard control

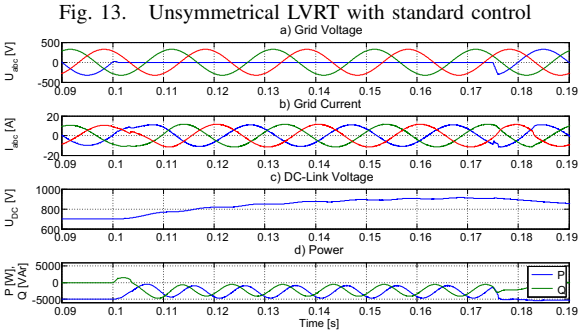

Fig. 14. Unsymmetrical LVRT with advanced control

system operating at nominal power the active current has to be reduced for system security purposes leading to a increase of the DC link voltage as seen in c). A slight unsteadiness in the symmetrical current signal can be identified at failure start and end. The increase of the DC link voltage is limited to U_{oc} by the I/V characteristic of the solar system, since this voltage is reached no power is transferred from the PV array. Additionally layouting PV systems the maximum voltage U_{oc} is mostly calculated at $-10°$ C. Depending on the used PV modules this gives an extra safety margin on the voltage following eq. (4) that might enable semiconductors to operate with full current without delivering active power but instead only reactive current. Taking an additional voltage margin due to the PV layout at $-10°C$ into account and although the PV array does not deliver any power in case U_{oc} is reached, challenges arise. It can be stated that depending on the chosen PV modules as well as semiconductors it is recommended that the maximum voltage is limited by any method to ensure safe operation of the semiconductors as well as to reduce stress on the DC link capacitors.

VI. Measurements

A. Test Setup

As power source a standard power supply was used. The inverter was controlled with an Infinion TriCore 1796 μController and connected through a transformer to the public grid. The switching frequency was chosen to 20 kHz whereas the sampling frequency was 5 kHz. The LCL filter was built up slightly different from the simulation parameters using a choke on the inverter side $L_C = 2.5\ mH$, a choke on the grid side $L_G = 0.5\ mH$ and a capacitor $C_F = 4.4\ \mu F$ leading to a resonance frequency around $f_{res} = 3717\ Hz$. Grid failures were performed using a sag generator according to [19]. Measurements were performed using either internal registers of the TriCore itself or a Dewetron DEWE2010 power meter.

B. Phase Locked Loop

The PLL was tested with and without pre-filter showing that unsymmetrical voltages will effect the PLL heavily as it was expected from the simulations. Fig. 15 shows the performance of the used PLL with PS pre-filter at unsymmetrical grid conditions (a=b=100%, c=0%). Clear PS characterization of the grid voltage is the foundation of high quality voltage support by means of reactive current according to the requirements of [8].In the following 100 steps are equivalent to one grid period of 20 ms.

C. Sequence Separation and Detection

The performance of the sequence separation and detection methods over time as studied in the simulations in fig. 7 and fig. 8 is illustrated for the three realized methods in fig. 16, fig. 17 and fig. 18. The measurement results are very well fitting to the above described simulation results regarding characteristic behaviour, detection time and behaviour due to noise. The accuracy of the dip / swell detection by the used RMS method was investigated among others with an unsymmetrical grid failure (a=b=100%, c=0%).The expected result of 57.4% remaining voltage can be achieved with a slight variation, probably depending on a slight variance in measurement accuracy of the voltage measurement.

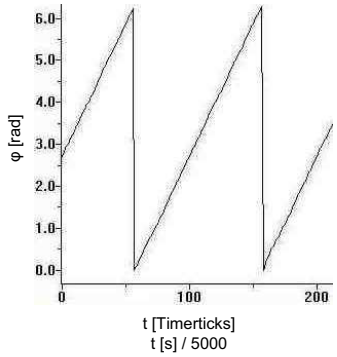

Fig. 15. Measurement performance dq-PLL with pre-filter

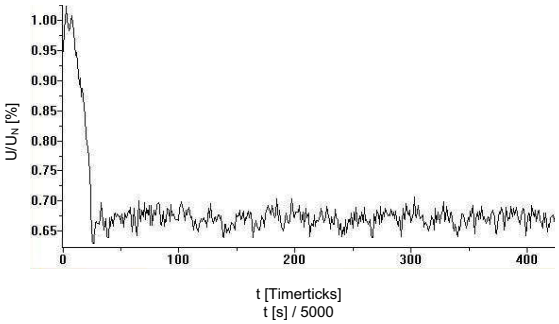

Fig. 16. Measurement performance T/4 method

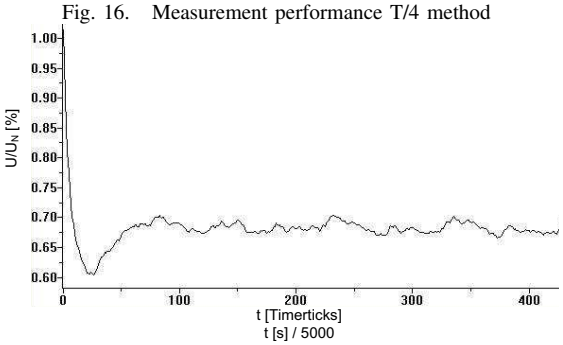

Fig. 17. Measurement performance SOGI method

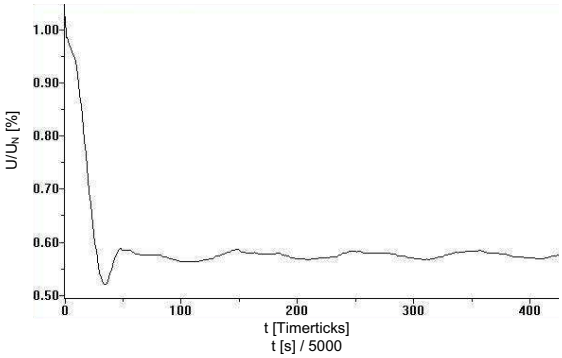

Fig. 18. Measurement performance RMS method

D. Low Voltage Ride Through

Using a controll loop without the described grid voltage feed-forward, LCL filter compensation nor line current limitation, the measurements shall be compared with the simulation results for symmetrical in fig. 12 and for unsymmetrical in fig. 14 grid faults. The T/4 method was used as pre-filter for the PLL. Departing from the simulations and [8] the grid voltage was reduced to around one fourth of the nominal voltage and the required ramp-out of the reactive current after grid failure clearance according to [8] was neglected to avoid confusion. In fig. 19 the slope for the reactive current was chosen to $k = 1$. A symmetrical dip (a=b=c=12.5%) resulting in ca. 13 V remaining voltage was applied to the inverter. For the following figures $k = 2$ was chosen. Fig. 20 illustrates a symmetrical LVRT (a=b=c=50%). As predicted by the simulations in fig. 12 the delivered currents rise depending on the voltage slope. The full reactive current is not delivered within one periode but

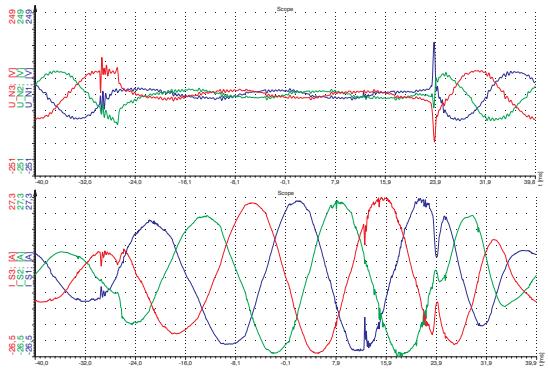

Fig. 19. Symmetrical LVRT, grid voltage (upper) and inverter output current (lower) graph

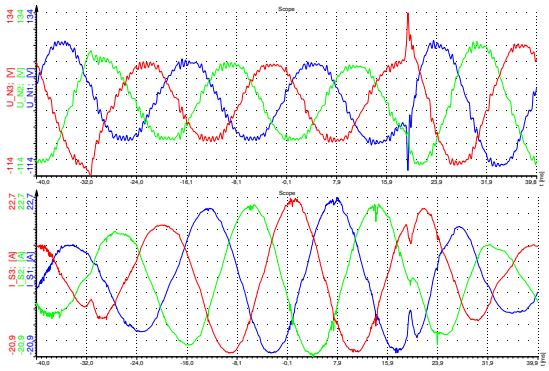

Fig. 20. Symmetrical LVRT, grid voltage (upper) and inverter output current (lower) graph

still within the mandatory time of 80 ms according to [8]. Departing from that fig. 21 shows an unsymmetrical LVRT (a=37%, b=c=100%). It can be seen that due to the common core of the sag generator as described in [19] the dipping phase effects the non dipping phases. Again voltage support by means of reactive current is not quite delivered within one periode of 20 ms but is still inside the required time of [8]. Other than the simulation in fig. 14 that was performed at nominal power including a line current limitation the currents are not limited and not all three are increasing in the same amount. Due to the reduced voltage using a transformer and using the sag generator which also includes a transformer current distortion and phase displacement is increased with decreasing voltage and current. As sub conlcusion it can be stated that the system behaves as predicted in the simulations. In both cases the basic requirements for voltage support from [5] and [6] by means of staying connected on grid and delivering reactive current as mandatory in [8] can be fulfilled. Anyway the discrete implemented controller design that need to be improved.

In addition to the shown measurements the LVRT was also performed with a dq0 control according to [10] using the same inverter hardware. These measurements were performed with half the grid voltage. The slope for the required reactive current was chosen to $k = 1$. In general the observed behaviour for symmetrical voltage dips is similar to the previous measurements. Fig. 22 shows a symmetrical fault (a=b=c=37%). The delivered currents do not rise as heavy as in fig. 20. Further a light ring in the output current which is depending on the instantaneous peak value of the failing phase can be obsereved due to the absence of an active damping method. This is created by the capacitor C_F of the LCL filter and dependant on the slope of the voltage failing. Reactive current is delivered to support the voltage. The unsymmetrical LVRT (a=37%, b=c=100%) shown in fig. 23 shows different behaviour than in fig. 21. The current of the failing phase increases as expected but another phase current decreases and all currents are additionally overlaid with harmonic distortion

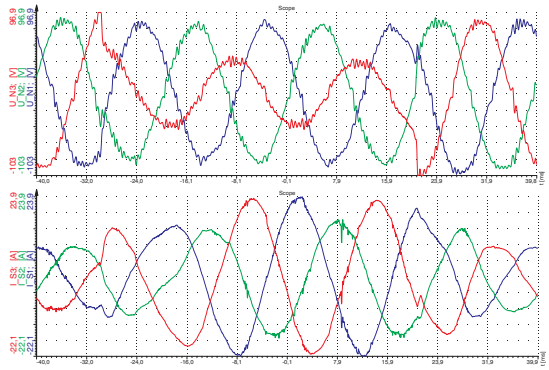

Fig. 21. Unsymmetrical LVRT, grid voltage (upper) and inverter output current (lower) graph

assumed to be the 100 Hz created by the existance of the NS. As sub conlcusion it can be statet that the system is able to ride through symetrical grid faults as long as the line current limitations are in place. Unsymmetrical grid faults lead to a NS that can not be handled using the standard dq0 control because of the reference frame rotating in positive direction. To prevent this additional NS compensation by means of a dq0 reference frame rotation in negative direction is needed. As mentioned in [20] and [21] the resonant controller does not need this due to its ω^2 in the return path of the integrator which enables the controller handling both sequnces that have in abc reference frame $\pm$ 50 Hz. Also for the dq0 control the basic requirements for transient voltage support as discussed above can be fulfilled.

VII. Conclusion

The fault ride through capability of a solar inverter is analysed. Main grid requirements are presented. The LVRT of a three-phase-four-wire grid-tied solar system with different control loops, different sequence separation and detection methods as well as stabilization of a three-phase dq-PLL have been investigated by simulations and experimental results. It can be concluded that LVRT capability of solar inverters rises high requirements to

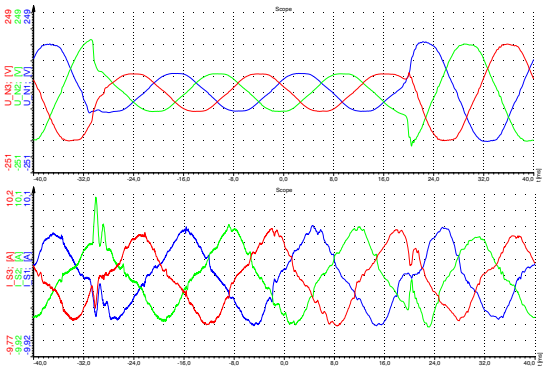

Fig. 22. Symmetrical LVRT with dq0 control, grid voltage (upper) and inverter output current (lower) graph

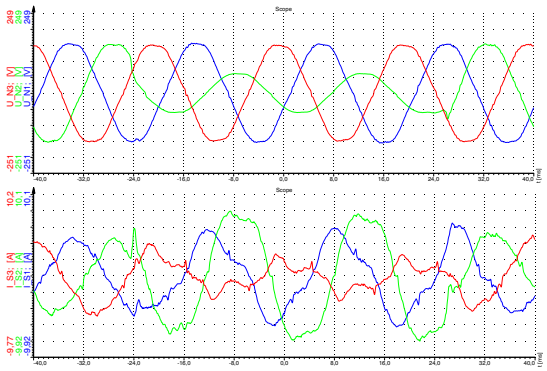

Fig. 23. Unsymmetrical LVRT with dq0 control, grid voltage (upper) and inverter output current (lower) graph

PLLs, especially under unsymmetrical grid conditions. The investigated topology can handle LVRTs without disconnection as long as a line current limitations are in place. For all types of LVRT special detection methods for transient variation of the grid voltages, a stable PLL as well as sequence separation methods to achieve the PS for orientation purposes of the reactive current required for voltage support have to be applied. Using P+Resonant controller in abc reference frame no issues due to other sequence components arise. Other than using PI controller in dq0 reference frame additional sequence compensation is needed. Although the PV power limits itself, additional stress is created on the DC link capacitors by oscillation during unsymmetrical grid faults and during the absence of a booster stage on the semiconductors by switching full current at the applied open circuit voltage of the PV system.

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