Low-Voltage Topologies for 40-Gb/s Circuits in Nanoscale CMOS

Theodoros Chalvatzis, *Student Member, IEEE*, Kenneth H. K. Yau, *Student Member, IEEE*, Ricardo A. Aroca, *Student Member, IEEE*, Peter Schvan, *Member, IEEE*, Ming-Ta Yang, and Sorin P. Voinigescu, *Senior Member, IEEE*

***Abstract*—This paper presents low-voltage circuit topologies for 40-Gb/s communications in 90-nm and 65-nm CMOS. A retiming flip-flop implemented in two different 90-nm CMOS technologies employs a MOS-CML Master–Slave latch topology with only two vertically stacked transistors. Operation at 40 Gb/s is achieved by a combination of low and high-V_T MOSFETs in the latch. Full-rate retiming with jitter reduction is demonstrated up to 40 Gb/s. Low-power broadband amplifiers based on resistor–inductor transimpedance feedback are realized in 90-nm and 65-nm CMOS to investigate the portability of high-speed building blocks between technology nodes. Experiments show that the transimpedance amplifier based on the CMOS inverter can reach 40-Gb/s operation with a record power consumption of 0.15 mW/Gb/s. A comparison between CMOS technologies underlines the importance of General Purpose rather than Low Power processes for high-speed digital design.**

***Index Terms*—Decision circuit, flip-flop, GP CMOS, LP CMOS, MOS-CML, retimer, transimpedance amplifier.**

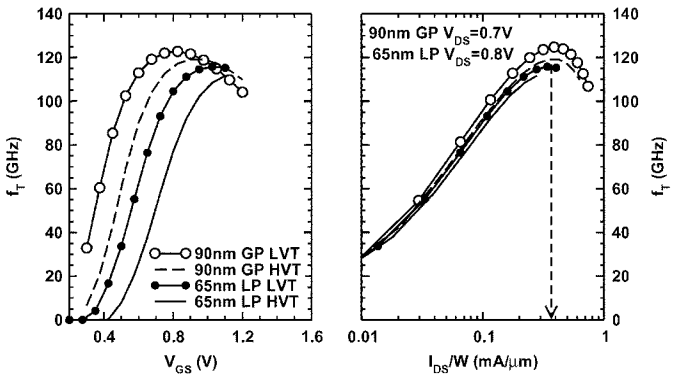

Fig. 1. Measured f_T versus (a) V_{GS} and (b) I_{DS}/W of 90-nm and 65-nm nMOSFETs with low and high-V_T, showing that the peak-f_T current density and peak-f_T value do not depend on V_T.

I. Introduction

ONE of the main advantages of MOSFET scaling to nanometer gate lengths is the ability to reach device speeds exceeding 120 GHz with low supply voltages. Despite the high intrinsic speed of transistors available in these processes, the design of 1.2-V 40-Gb/s digital blocks in CMOS for fiber optic and backplane communications remains a challenge. A CMOS implementation would permit 40-Gb/s serializer–deserializer (SERDES) chips to reach the same levels of integration as state-of-the-art 10-Gb/s ICs [1], [2] and to operate from a single 1.2-V power supply. For a 40-Gb/s SERDES to be economically viable, its cost and performance must be competitive compared to a 4×10 Gb/s solution [3]. Typically, a 40-Gb/s SERDES must have less than 2.5 times the cost of a 10-Gb/s system while consuming less than 2.5 times the power.

Although a half-rate 40-Gb/s transmitter in CMOS has been reported in [4], it operates from 1.5 V and consumes two times the power of a similar SiGe BiCMOS transmitter operating at 86 Gb/s [5]. Full-rate retiming has been successfully demonstrated at speeds above 40 Gb/s only in III-V [6], [7] and SiGe BiCMOS technologies [8], [9]. However, these circuits operate from 1.5 V or higher supplies and consume at least 20 mW per latch. A full-rate 40-Gb/s latch has yet to be realized in CMOS. To truly benefit from the lower power potential of nanoscale MOSFETs, the traditional CML latch topology must be simplified by reducing the number of vertically-stacked transistors to allow for 1.2-V operation. The availability of low-V_T devices is also a prerequisite. In the past, the low-voltage latch has been implemented either by removing the current source [10] or using transformers [11] to couple the signal between the differential pairs in the clock and data paths. The former solution has been demonstrated in 90-nm CMOS at speeds below 20 GHz. The latter has been used in a 60-Gb/s 2:1 multiplexer (MUX) clocked at 30 GHz, but its bandwidth is limited to that of the transformer. On the other hand, low-voltage transimpedance amplifiers (TIAs) in 90-nm CMOS operating from 1 V [12] and 0.8 V [13] have been recently reported, but at data rates of 38.5 Gb/s and 25 Gb/s, respectively. This paper presents the first 40-Gb/s full-rate D-type flip-flop (DFF) and the first 40-Gb/s TIA in CMOS. Operation at 40 Gb/s is made possible by combining low-V_T and high-V_T transistors in the latch and optimally biasing, and sizing the transistors at the peak-f_T current density (Fig. 1).

This paper is organized as follows. The design of a 40-Gb/s latch and decision circuit is described in Section II. A discussion of 90-nm General Purpose (GP) and 65-nm Low Power (LP) technology performance is presented in Section III. The differences between GP and LP processes for high-speed design are

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T. Chalvatzis, K. H. K. Yau, R. A. Aroca, and S. P. Voinigescu are with the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, M5S 3G4, Canada (e-mail: theo@eecg.utoronto.ca).

P. Schvan is with Nortel Networks, Ottawa, ON, K1Y 4H7, Canada.

M.-T. Yang is with Taiwan Semiconductor Manufacturing Company, Science-Based Industrial Park, Hsin-Chu, Taiwan 300-77, R.O.C.

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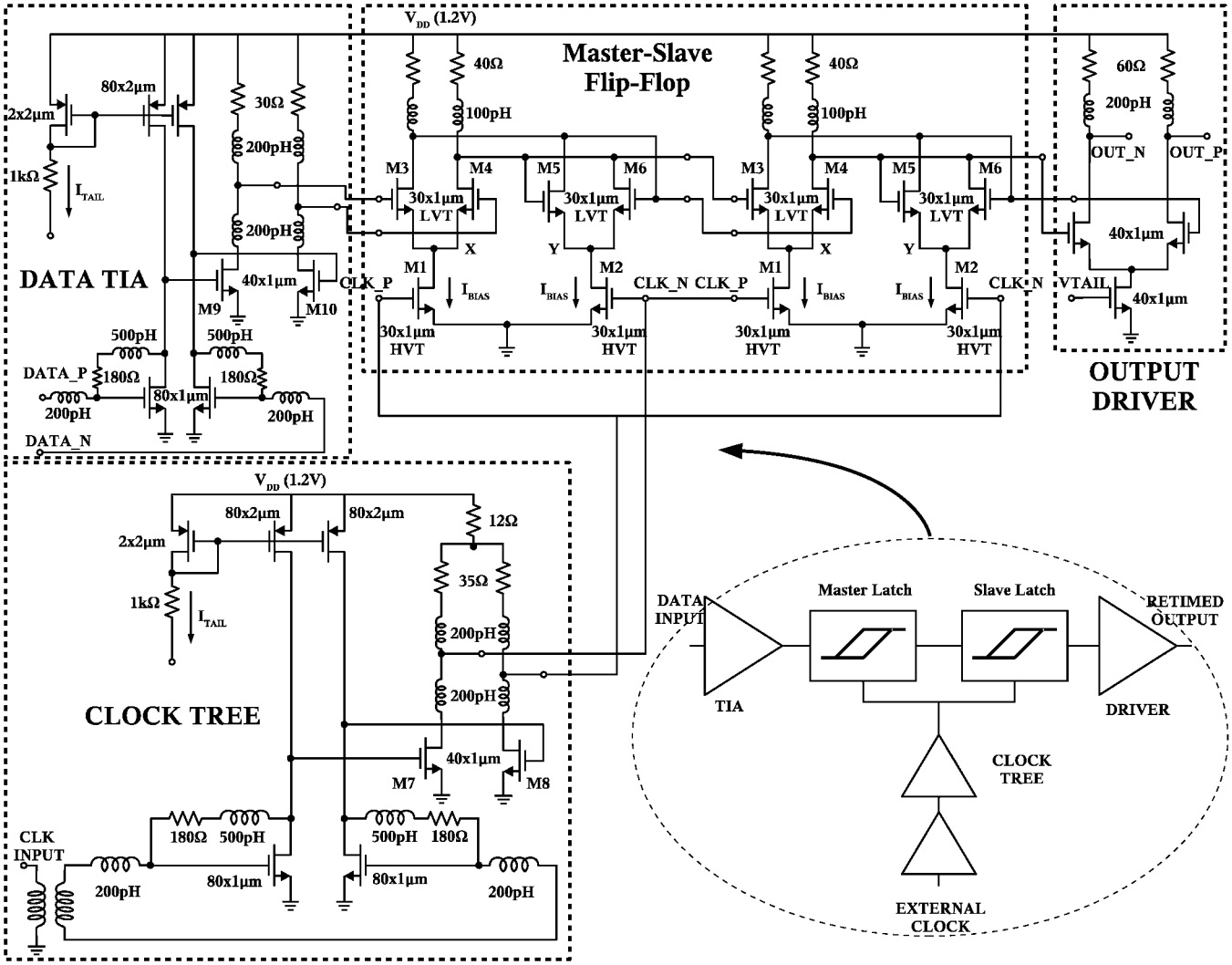

Fig. 2. Full transistor-level schematic of decision circuit in 90-nm CMOS. All devices have minimum channel length.

analyzed based on experimental data on devices, latches, and TIA circuits.

II. Decision Circuit

Flip-flop circuits are the most critical digital blocks used in high-speed wireline and fiber-optic transceivers, equalizers, and mm-wave-sampling ADCs [14]. In a full-rate transceiver, the flip-flop must retime the data at a clock frequency equal to the data rate, while also removing the jitter. Fig. 2 illustrates the proposed MOS-CML latch schematic and its placement in a decision circuit. The data and clock signals are applied to the Master-Slave flip-flop through broadband TIAs. A MOS-CML output buffer drives the 40-Gb/s signal to 50-Ω loads.

A. Latch

In the proposed latch topology, the clock signal switches the differential pair transistors M1 and M2 from 0 to $2\times I_{\rm BIAS} = 0.3$ mA/μm. The latter corresponds to the peak-f_T current density of nMOSFETs [12]. Equivalently, when the gate voltages of M1 and M2 are equal, the current density through each device is 0.15 mA/μm. To fully switch the 90-nm MOS differential pair, a voltage swing exceeding 300 $\rm mV_{pp}$ per side is required [12]. For a 30×1 μm $\times$ 0.09 μm device with $I_{\rm BIAS} = 4.5$ mA and a load resistance of $R_L = 40\ \Omega$, the voltage swing at the output of each latch is

$$\Delta V_{\rm swing} = (I_{M1} + I_{M2})R_L = 360\ \text{mV} \tag{1}$$

which is sufficient to fully switch the differential pair in the next stage and results in an inverter gain $A_V = -1.2$. The bandwidth of the latch is extended with shunt inductive peaking. For a fanout of $k = 1$ and the input capacitance of the next stage equal to $C_{\rm gs} + (1 - A_V)C_{\rm gd}$, the total capacitance at the drain of M3 is

$$\begin{aligned} C_T &= C_{\rm db3} + C_{\rm gd3} + C_{\rm gd5} + C_{\rm db5} + C_{\rm gs6} \\ &\quad + (1 - A_V)C_{\rm gd6} + k\,(C_{\rm gs} + (1 - A_V)C_{\rm gd}) \\ &= 197\ \text{fF} \end{aligned} \tag{2}$$

and the inductance $L = 100$ pH increases the $\rm BW_{3dB}$ [15] to

$$\rm BW_{3dB} = 1.6 \times \frac{1}{2\pi R_L C_T} = 32.3\ GHz \tag{3}$$

which is adequate for 40-Gb/s operation on the data path.

The second technique that improves the speed of the latch is the choice of devices with different V_T in the data and clock paths of the latch. As shown in Fig. 2, low-V_T transistors are employed in the data path differential pairs M3–M4 and M5–M6. The clock pair is designed with high-V_T devices. This approach ensures that transistors in the clock path buffer, immediately preceding the latch, have $V_{DS} > 0.3$ V, as required for operation at 40 GHz. When either M1 or M2 is turned off, its V_{GS} is equal to V_T. A high-V_T device (0.34 V) on the clock path ensures that the f_T of M7/M8 remains larger than 80 GHz because their $V_{DS} = 0.34$ V. On the other hand, when M3 or M4 are fully turned off, $V_X = V_{DS,M1} = V_{DD} - \Delta V_{\text{swing}} - V_{T,M3}$. By choosing a low V_T (0.18 V) device for M3–M6, the V_{DS} and therefore the speed of M1/M2 are maximized.

B. Data and Clock Buffers

The gain stages that provide the data and clock signals to the latches in the flip-flop are implemented as fully differential versions of the nMOS TIA with pMOS active load described in [16]. As illustrated in Fig. 2, an on-chip 1:1 vertically stacked transformer converts the single-ended external clock to a differential signal applied to the TIA input for testing purposes. Although the transformer limits the bandwidth of the clock tree at low frequencies to about 20 GHz, it is preferred over applying the clock signal to one side of the amplifier's differential input. Because the differential amplifier has no common-mode rejection, the clock signal would arrive at the latch with amplitude and phase mismatch. However, in a 40-Gb/s SERDES implementation a 40-GHz VCO would be integrated on chip and the transformer would be removed. The TIAs are followed by differential common-source stages with inductive peaking.

To tune out the parasitic capacitance in the feedback loop of the TIA, a 500-pH inductor, realized with vertically stacked windings in the top two metal layers of the process, is inserted in series with the feedback resistor R_F. Its self-resonant frequency exceeds 100 GHz when a layout with 35 μm diameter and 2 μm conductor width is employed. The relatively large series resistance of the vertically-stacked inductor can be absorbed in the feedback resistor R_F.

The pMOS current mirrors control the bias currents of the MOSFETs in the TIA stages and in the following common-source amplifiers, making them independent of temperature and power supply variations [17]. The role of the differential common-source stages with inductive peaking is also to provide the proper DC levels to the latches in the flip-flop. The 12-Ω common-mode resistor at the clock tree output lowers the DC voltage level at the gates of M1 and M2. The gate voltage must correspond to a drain current density of 0.15 mA/μm, such that the transistors switch from 0 to 0.3 mA/μm. It should be noted that a CML inverter with a tail current source cannot be employed in place of the M7–M8 differential pair due to lack of voltage headroom. More importantly, this bias scheme is robust to supply voltage variation from 1.1 V to 1.3 V. When the supply voltage increases above 1.1 V, the V_{GS} of the clock pair transistors in the latch increases commensurately. As illustrated in Fig. 1, this has no impact on the f_T of the nMOSFET which remains practically constant at large V_{GS}.

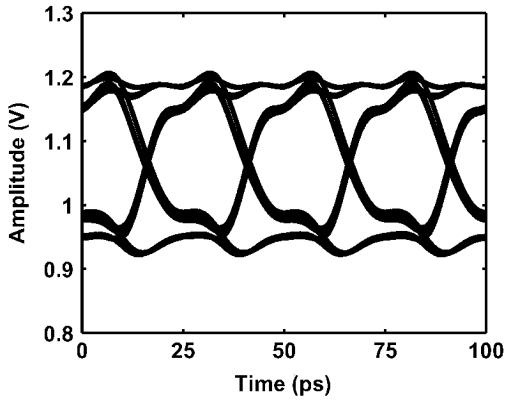

Fig. 3. Simulated 40-Gb/s eye diagram of decision circuit in 90-nm CMOS.

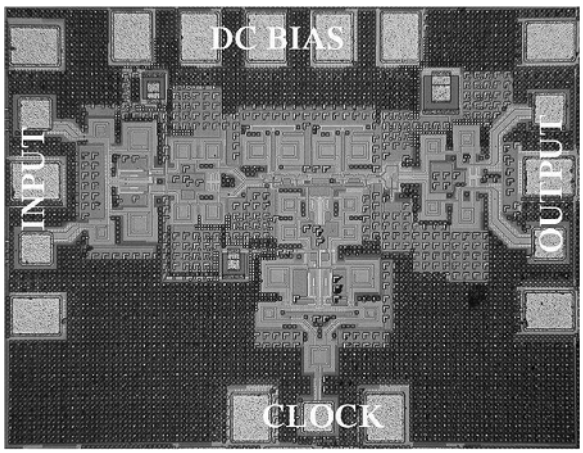

Fig. 4. Die photo of decision circuit in 90-nm CMOS.

C. Simulation Results

The decision circuit was simulated over process and temperature corners after extraction of layout parasitics with a 2^7-1 pseudorandom signal. The corresponding output 40-Gb/s eye diagram at $V_{DD} = 1.2$ V is shown in Fig. 3.

D. Experimental Results of Decision Circuit

The decision circuit was fabricated in two different 90-nm CMOS processes to investigate the portability of the design across foundries. All transistor sizes are identical and the passive components have the same value (R and L) in both technologies. Both dies (Fig. 4) occupy 800×600 μm^2 including the pads.

The circuits were tested on wafer with 67-GHz single-ended and differential probes. In the absence of a full-fledged 40-Gb/s bit error rate tester (BERT), the 40-Gb/s pseudorandom binary sequence (PRBS) data were generated by multiplexing four appropriately shifted pseudorandom streams at 10 Gb/s each. The external clock was provided by a low phase noise Agilent E8257D PSG signal source and data were captured by an Agilent Infiniium DCA-86100C oscilloscope with 70-GHz remote heads. It should be noted that contributions from the test setup and oscilloscope have not been de-embedded from the measured jitter, amplitude, and rise/fall times shown in Figs. 5–8 and 11. Fig. 5 reproduces the input and output eye

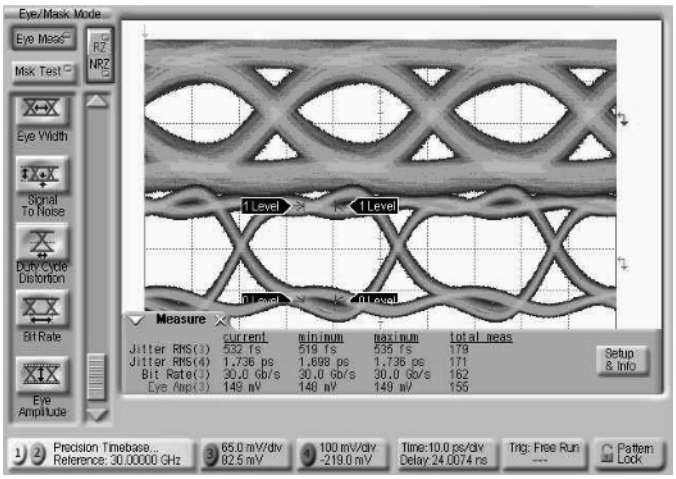

Fig. 5. Input (top, channel 4) and output (bottom, channel 3) eye diagrams at 30 Gb/s ($V_{DD} = 1.2$ V, 508-bit pattern).

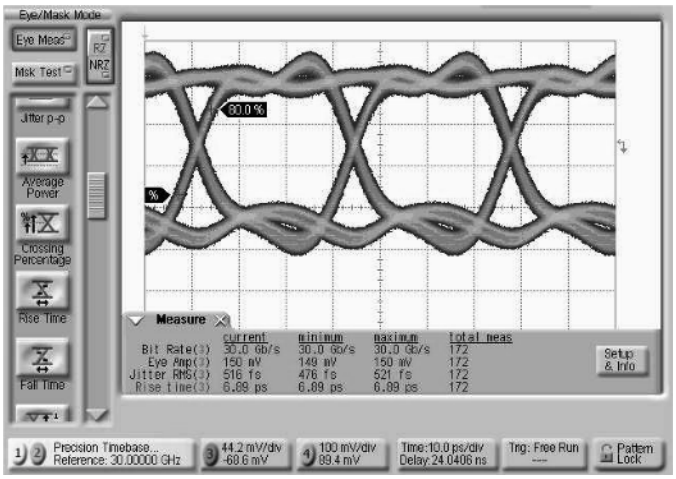

Fig. 6. Output eye diagram at 30 Gb/s ($V_{DD} = 1.2$ V, 508-bit pattern) showing rise time smaller than 7 ps.

diagrams at 30 Gb/s and 1.2-V supply, showing a significant reduction in jitter from 1.7 to 0.5 ps rms. The rise/fall times are improved from 14 ps to less than 7 ps (Fig. 6). Compared to the decision circuit of [18], where 40-Gb/s operation required $V_{DD} = 1.5$ V, an improved clock distribution tree in this design allowed for 40-Gb/s full-rate retiming from 1.2 V (Figs. 7 and 8). Fig. 8 illustrates the output eye diagram at 40 Gb/s for a $4 \times (2^{31} - 1)$ input pattern. The measured phase margin of the latch is 163°. The resulting bathtub curve at 40 Gb/s can be found in Fig. 9. Error-free operation was verified for an input pattern of $4 \times (2^7 - 1) = 508$ bits, by capturing the input and output bitstreams on the sampling scope. Part of the captured bitstream at 40 Gb/s is shown in Fig. 10. Power dissipation at 1.2 V is 130 mW.

The decision circuit was tested across temperature for different supply voltages to verify the robustness of the latch biasing scheme in the absence of current sources. Measurements were conducted for supply voltages between 1 V and 1.5 V and at temperatures up to 100 °C. At 1-V supply and 100 °C, the maximum rate with retiming and jitter reduction is

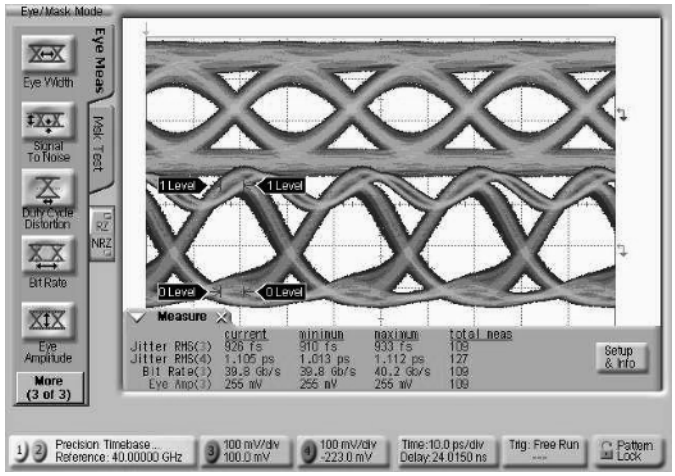

Fig. 7. Input (top, channel 4) and output (bottom, channel 3) eye diagrams at 40 Gb/s ($V_{DD} = 1.2$ V, 508-bit pattern).

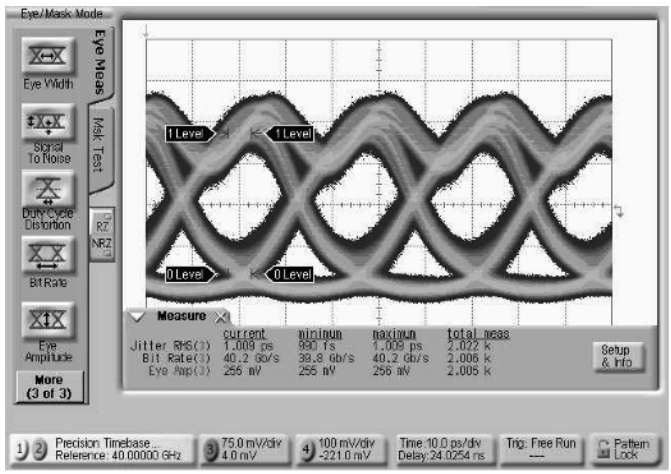

Fig. 8. Output eye diagram at 40 Gb/s and 25 °C ($V_{DD} = 1.2$ V) with 2×255 $\mathrm{mV_{pp}}$ output swing for a $4 \times (2^{31} - 1)$ input pattern.

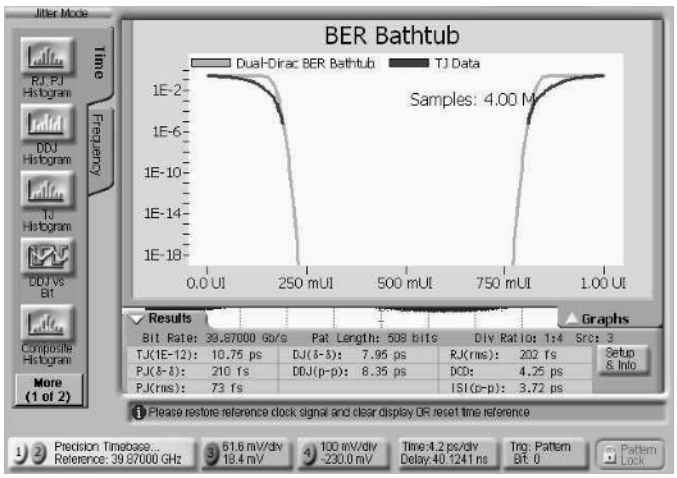

Fig. 9. Bathtub curve of output at 40 Gb/s and 25 °C ($V_{DD} = 1.2$ V, 508-bit pattern).

32 Gb/s. Fig. 11 shows the 40-Gb/s eye diagram at 1.2 V and 100 °C. Even though no errors were observed in this case, the output jitter is not improved over that at the input, indicating

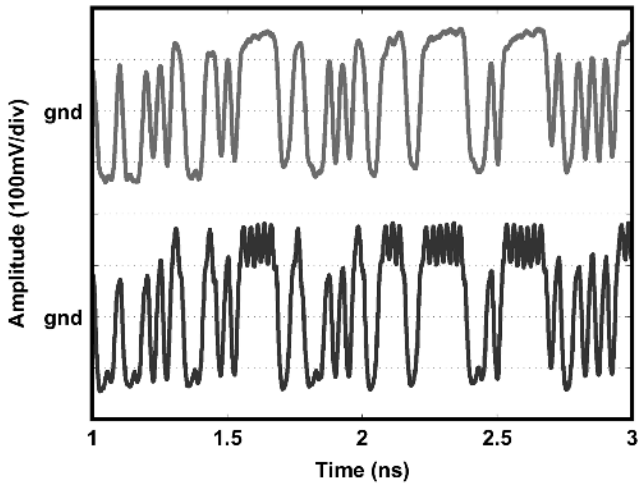

Fig. 10. Input (top) and output (bottom) signals for a 508-bit pattern at 40 Gb/s and 25 °C ($V_{DD} = 1.2$ V, 508-bit pattern).

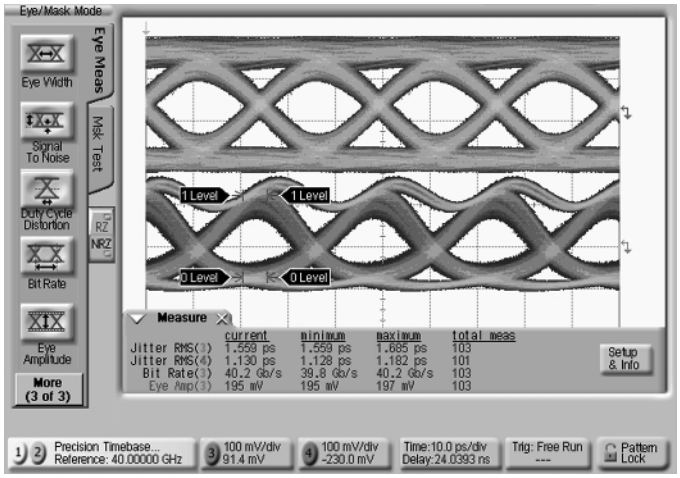

Fig. 11. Input (top, channel 4) and output (bottom, channel 3) eye diagrams at 40 Gb/s and 100 °C ($V_{DD} = 1.2$ V, 508-bit pattern).

that the clock path does not have enough bandwidth and that the latches do not retime the data.

Table I compares this circuit to state-of-the-art latches in SiGe BiCMOS and InP technologies. The proposed MOS-CML latch has the lowest power dissipation. At 40 Gb/s, the CMOS latch consumes half the power of the 43-Gb/s SiGe BiCMOS latch.

III. Scaling to 65-nm CMOS

A. Device Performance in 90-nm GP and 65-nm LP CMOS

The measured f_T of 90-nm GP and 65-nm LP nMOSFETs from two different foundries is summarized in Fig. 1. The measured data in Fig. 1 clearly indicate that the peak-f_T value occurs at the same current density irrespective of the device threshold voltage and technology node. As shown in Section II, this property of submicron MOSFETs can be applied in the design of high-speed digital circuits that are robust to threshold voltage, V_{GS}, and ultimately power supply voltage variation. Another important aspect unveiled by the measured data in Fig. 1 is that the threshold voltage of the low-V_T 65-nm LP MOSFETs is actually higher than that of the high-V_T 90-nm

TABLE I
Comparison of High-Speed Latches in Decision Circuits

Ref	Technology	Rate (Gb/s)	Supply (V)	P_{latch} (mW)	Area (μm^2)
[6]	245-GHz InP HEMT	80	5.7	N/A	N/A
[7]	150-GHz InP HBT	50	1.5	20	N/A
[5]	150-GHz SiGe BiCMOS	43	2.5	20	55×63
[8]	120-GHz SiGe HBT	43	3.3	N/A	N/A
This work	120-GHz CMOS	40	1.2	10.8	100×80

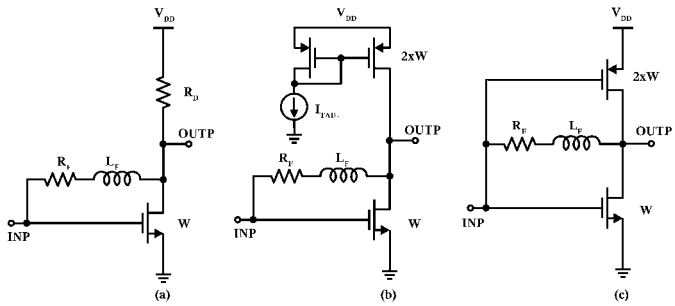

Fig. 12. Circuit schematics of low-voltage TIAs with resistive and inductive feedback. (a) nMOS inverter with resistive load. (b) nMOS inverter with pMOS active load. (c) CMOS inverter.

GP devices. At the same time, the f_T of the 65-nm LP FETs is slightly lower than that of the 90-nm GP ones. Both effects are due to the thicker gate oxide and slightly longer gate lengths of the 65-nm LP process. This behavior is the result of the requirement to reduce gate leakage in LP processes for RF and analog applications [19]. However, gate and subthreshold leakage pose no problem at mm-wave frequencies and in high-speed digital CML gates, where the tail current far exceeds the leakage currents [20].

B. Building Block Evaluation in 65-nm LP CMOS

To investigate the benefits of switching from 90-nm GP CMOS to 65-nm LP CMOS for 40-Gb/s applications, two TIA circuits and a static divider using the same topology as the 90-nm GP CMOS latches described earlier were designed and tested.

1) Transimpedance Amplifiers: A 40-Gb/s CMOS TIA must be able to operate from 1.2-V supply with more than 30 GHz bandwidth and low noise. Possible TIA topologies are shown in Fig. 12. The TIA with resistive load [Fig. 12(a)] requires a significant DC voltage drop on R_D in order to achieve adequate open loop gain, making it impractical. One approach to increase the gain, while requiring only 0.6 V of DC headroom, is to replace the resistor R_D with a pMOS active load [Fig. 12(b)], as has been shown in [12]. The loop gain of the TIA increases from $g_m \times R_D//R_F$ to $g_m \times r_{o,n}//r_{o,p}//R_F$. The pMOS load is needed to increase the gain of the amplifier at low supply voltages, at the expense of higher capacitance at the output node. The latter effect is partially mitigated by the feedback inductor, which resonates out the parasitic capacitance of the nMOS and

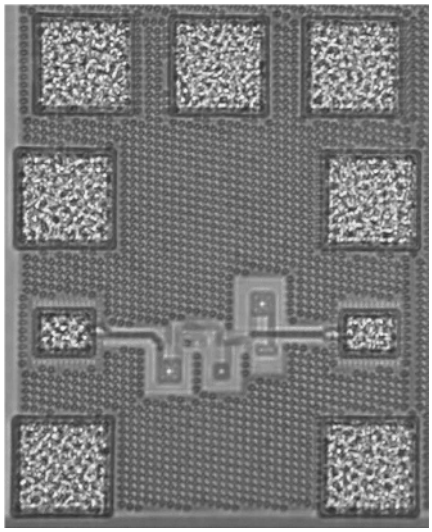

Fig. 13. Die photo of CMOS TIA in 65-nm CMOS.

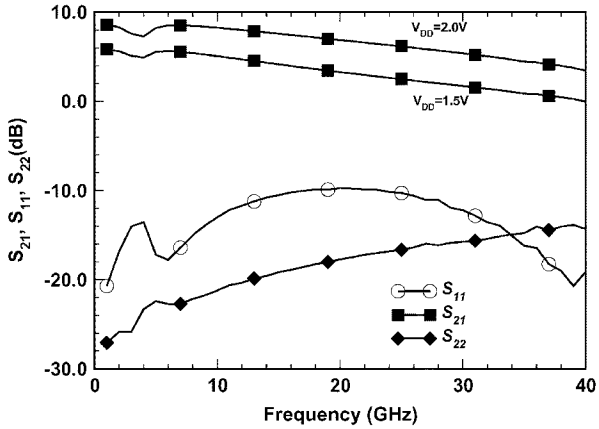

Fig. 14. Measured S-parameters of CMOS TIA in 65-nm CMOS.

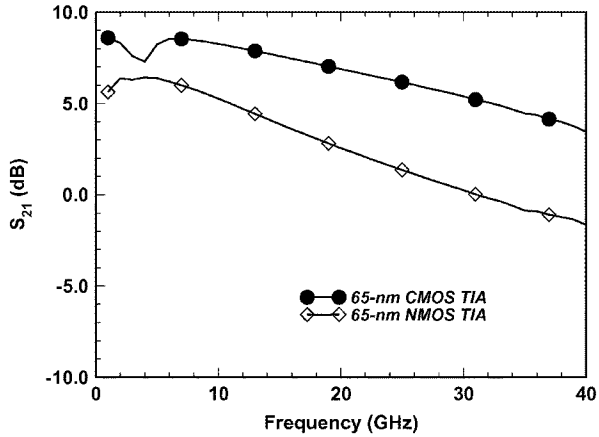

Fig. 15. Measured S_{21} of nMOS and CMOS TIAs in 65-nm CMOS.

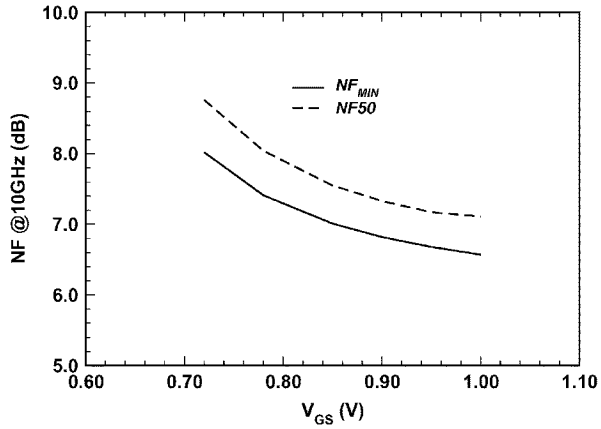

Fig. 16. $\mathrm{NF_{MIN}}$ and $\mathrm{NF50}$ at 10 GHz of CMOS TIA in 65-nm CMOS for different bias voltages.

pMOS transistors. To further improve performance, while reducing the power dissipation, one can employ a typical CMOS inverter with resistive and inductive feedback [Fig. 12(c)]. As outlined in [16], the CMOS inverter offers the advantage of smaller size and lower bias current for the same performance. For example, the CMOS inverter with feedback resistor R_F has a small-signal open-loop gain of

$$A = \frac{g_{m,n} + g_{m,p}}{g_{o,n} + g_{o,p} + 1/R_F} \tag{4}$$

with an input resistance

$$R_{IN} = \frac{R_F}{1 + A}. \tag{5}$$

Due to its higher transconductance, it can achieve the same noise impedance for about 1/3 the transistor size of an nMOS TIA [12].

The nMOS TIA with pMOS active load [Fig. 12(b)] and the CMOS inverter TIA [Fig. 12(c)] were fabricated in the 65-nm LP technology. The values of the transistor total gate width W, feedback resistor R_F, and inductor L_F are shown in Table II. In both cases, the core TIA stage is followed by a buffer, which drives the signal to the external 50-Ω load. The die photo of the 65-nm CMOS TIA is reproduced in Fig. 13. The circuit occupies an area of 300×370 μm^2 including the pads. The core area of the TIA is 85×65 μm^2 and the 600-pH inductor has a diameter of 10 μm with 0.5 μm metal width and is realized in the top three metal layers of the process. S-parameter, eye diagram, and noise measurements were performed on wafer.

Due to the higher threshold voltage of the 65-nm LP MOSFETs compared to the GP technology (Fig. 2), and therefore the larger V_{GS} required for maximum gain and lowest noise [12], the supply voltage $V_{DD} = V_{GSn} + V_{SGp}$ of the TIA exceeds 1.3 V. The measured S-parameters of the 65-nm CMOS TIA are provided in Fig. 14. The 3-dB bandwidth of the 65-nm CMOS and nMOS TIAs is 23 GHz and 21 GHz, respectively, from 1.5-V power supplies. We also note that the 65-nm nMOS TIA has lower bandwidth while operating from higher supply voltages than its counterpart implemented in 90-nm GP CMOS [12].

Noise parameter measurements were performed up to 26 GHz with a Focus Microwaves system. The $\mathrm{NF_{MIN}}$ and $\mathrm{NF50}$ of the CMOS TIA is presented in Fig. 16 for various $V_{GS} = V_{DD}/2$ voltages. Fig. 17 illustrates the $\mathrm{NF_{MIN}}$ and $\mathrm{NF50}$ versus frequency of both 65-nm TIAs and a 90-nm nMOS TIA from [12]. Despite its lower current, the CMOS TIA has lower $\mathrm{NF_{MIN}}$ due

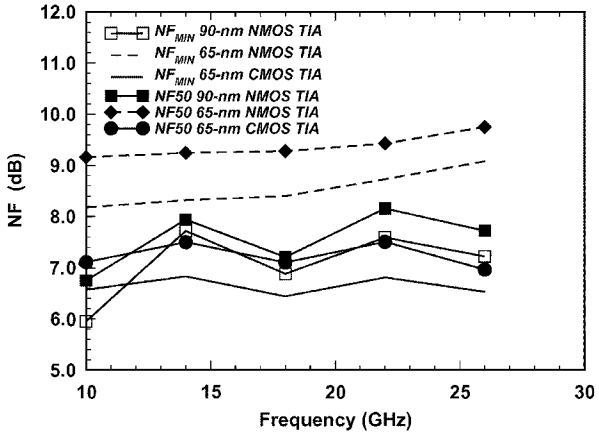

Fig. 17. $\mathrm{NF50}$ and $\mathrm{NF_{MIN}}$ versus frequency of nMOS TIAs in 90 nm and 65 nm and CMOS TIA in 65 nm. Measurements taken at minimum noise bias.

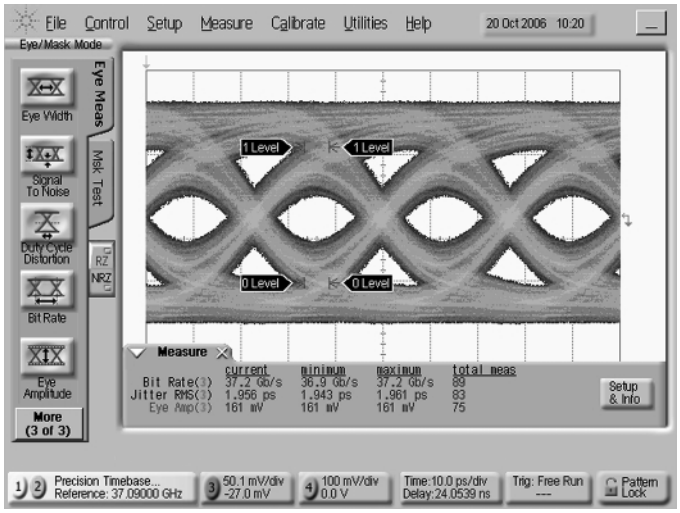

Fig. 18. Output eye diagram at 37 Gb/s of nMOS TIA in 65-nm CMOS with 100-$\mathrm{mV_{pp}}$ input and 508-bit pattern.

to its lower noise resistance R_n and because the real part of its optimum noise impedance R_{Sopt} is closer to 50 Ω.

Eye diagrams were measured for both TIA circuits with a $4\times(2^7-1)=508$ bits pseudorandom sequence having 100 $\mathrm{mV_{pp}}$ amplitude. The output eye diagrams at 37 Gb/s are illustrated in Figs. 18 and 19. The bandwidth improvement is apparent in the eye diagrams, with the CMOS TIA having a larger eye opening. The better frequency response of the CMOS inverter TIA allowed for 40-Gb/s operation as shown in Fig. 20. For a power consumption of 6 mW in its gain stage, the circuit achieves 0.15 mW/Gb/s, while having a noise figure lower than 9 dB and 6 dB of gain.

The 65-nm TIA experiments prove that, in a given technology node, the CMOS inverter TIA has lower noise figure, higher gain, and larger bandwidth, while consuming less than half the power of a nMOS TIA. The 40-Gb/s CMOS TIA also consumes less power than common-gate TIAs [13], [21]. However, when comparing the performance of the same nMOS TIA topologies in 90-nm GP and 65-nm LP technologies we find that, despite the lower metal pitch and area, the 65-nm LP circuits suffer from

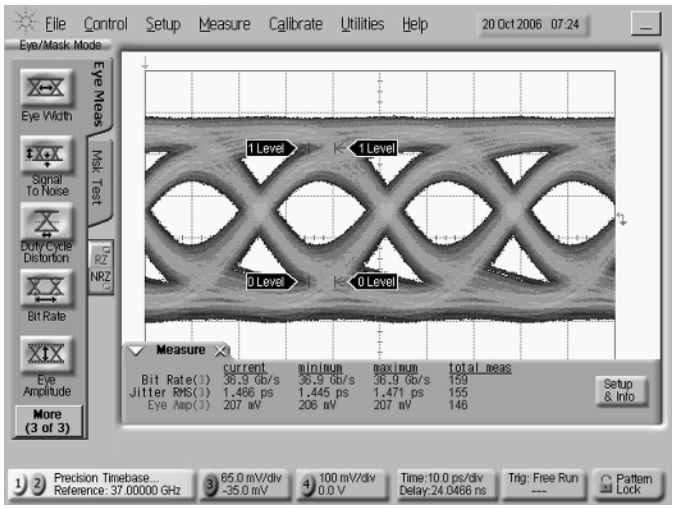

Fig. 19. Output eye diagram at 37 Gb/s of CMOS TIA in 65-nm CMOS with 100-$\mathrm{mV_{pp}}$ input and 508-bit pattern.

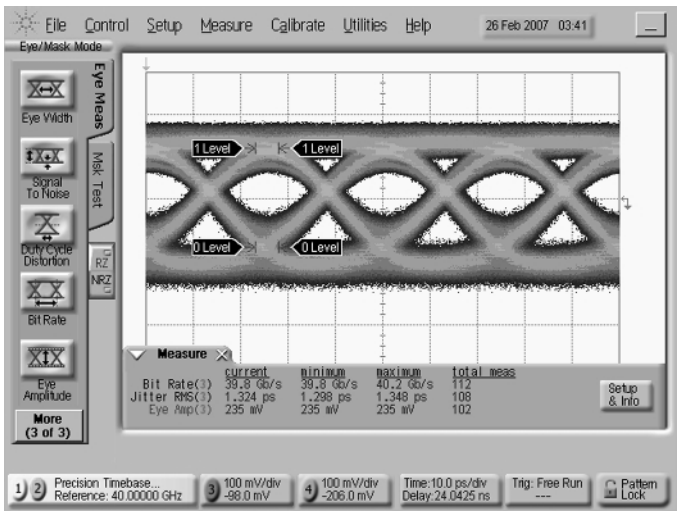

Fig. 20. Output eye diagram at 40 Gb/s of CMOS TIA in 65-nm CMOS with 100-$\mathrm{mV_{pp}}$ input and $4\times(2^{31}-1)$ pattern.

TABLE II
COMPARISON OF TIA TOPOLOGIES

Topology	65-nm NMOS (Fig. 12b)	65-nm CMOS (Fig. 12c)
W (μm)	50	20
R_F (Ω)	200	170
L_F (pH)	600	600
I_{DS} (mA)	10	4
BW_{3dB} (GHz)	21	29
$Gain$ (dB)	6	8
V_{DD} (V)	1.3	1.5
P (mW)	13	6
$NF50@26GHz$ (dB)	9.75	6.96

higher noise, lower bandwidth and dissipate more power than the 90-nm GP ones. The performance of both TIA topologies in 65-nm LP CMOS is summarized in Table II.

2) Static Divider: The static divider consists of two latches with feedback and an output driver (Fig. 21). The same latch

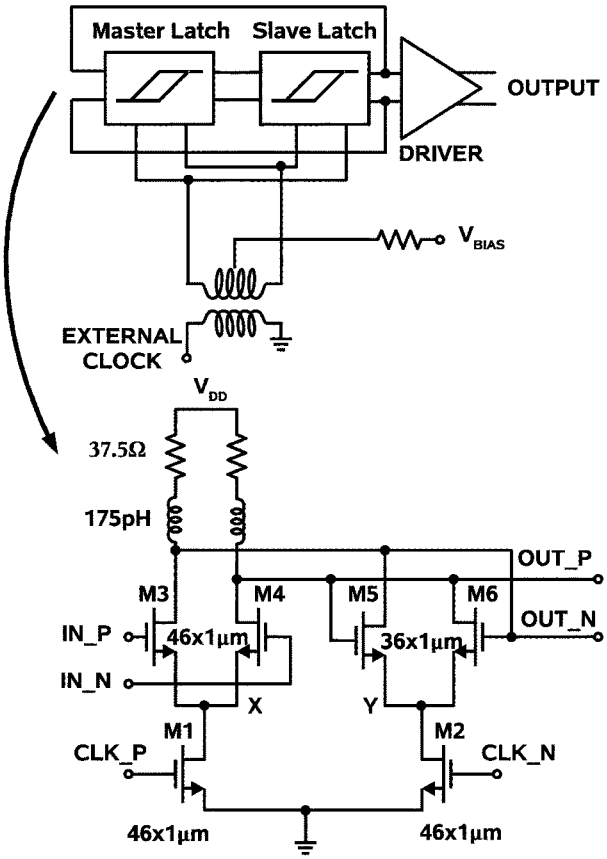

Fig. 21. Static divider and latch in 65-nm CMOS.

topology as in Fig. 2 is employed and the 65-nm LP transistors have a total width of $W = 46$ μm and 36 μm with a corresponding $I_{\rm BIAS} = 7$ mA. The single-ended external clock is converted to a differential signal through a transformer. The gate bias of the clock transistors in the latch is applied at the center tap of the transformer. Fig. 22 shows the layout of the 65-nm LP CMOS static divider. Its measured self-oscillation frequency was 28 GHz and the circuit was verified to divide up to 36 GHz when biased from 1.5-V supply. Clearly, the 65-nm CMOS TIA and static divider measurements indicate that, to reach 40 Gb/s, 65-nm LP CMOS circuits require supply voltages exceeding 1.2 V.

IV. Conclusion

Low-voltage circuit blocks have been fabricated for 40-Gb/s wireline communications in 90-nm GP and 65-nm LP CMOS technologies. A decision circuit achieves full-rate retiming at 40 Gb/s from 1.2 V with a power consumption of 10.8 mW in the latch. A CMOS inverter TIA with resistive and inductive feedback has higher bandwidth, lower noise, and larger gain than an nMOS TIA with active pMOS load, while consuming 1/3 of the current with a power dissipation of 6 mW. Biasing MOSFETs at the peak-f_T current density (0.3 mA/μm) in the latch for maximum speed and at optimum noise figure current density (0.15 mA/μm) in the TIAs for low noise and maximum bandwidth ensures the optimum performance across technology nodes and foundries.

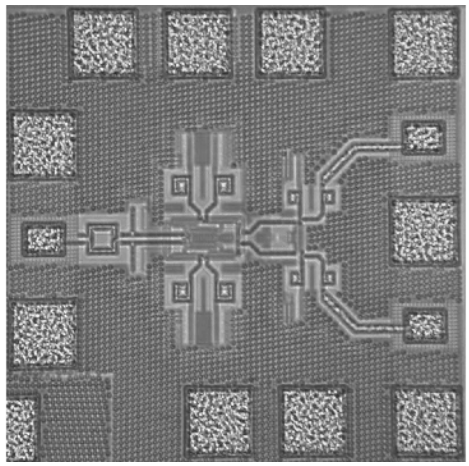

Fig. 22. Die photo of static divider in 65-nm CMOS.

While these low-power topologies show for the first time operation in CMOS at 40 Gb/s from 1.2-V supply, the behavior over temperature indicates that 90-nm GP and 65-nm LP CMOS technologies do not have enough margin for a 40-Gb/s SERDES with full-rate retiming. A comparison of transistor and circuit performance between 90-nm GP and 65-nm LP technologies clearly indicates that a 65-nm LP process is not adequate for a 40-Gb/s SERDES operating from 1.2-V supply, because of the high threshold voltage and insufficient f_T, and $f_{\rm MAX}$ of nMOSFETs. At the minimum, 65-nm GP CMOS or 45-nm CMOS technology will be required to compete with SiGe BiCMOS technology for 40-Gb/s circuits.

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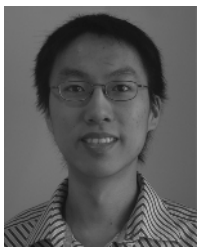
Theodoros Chalvatzis (S'07) received the Diploma in electrical and computer engineering from the University of Patras, Greece, in 2001 and the M.A.Sc. degree in electrical engineering from Carleton University, Ottawa, ON, Canada, in 2003. He is currently working toward the Ph.D. degree at the University of Toronto, Toronto, ON, Canada.

From 2002 to 2003, he held an internship with Nortel Networks, where he worked on advanced wireless receivers. His research interests include high-speed analog-to-digital converters and digital circuits for wireless and wireline applications.

Mr. Chalvatzis received the second Best Student Paper Award at the RFIC 2006 Symposium.



Kenneth H. K. Yau (S'03) received the B.A.Sc. degree, with distinction, in engineering physics from the University of British Columbia, Vancouver, BC, Canada, in 2003 and the M.A.Sc. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2006. He is currently pursuing the Ph.D. degree in electrical engineering at the University of Toronto.

He has held an internship with Broadcom Corporation, Vancouver, Canada, where he was involved with the development of embedded software for IP telephony. He was also involved with the development of a nanoscale vibration control system for the quadrupole magnets of the Next Linear Collider. His current research interests are in the area of device modeling for advanced MOSFETs and SiGe HBTs, and nanoscale device physics.

Mr. Yau received numerous scholarships, including an undergraduate research award and a post-graduate scholarship from the Natural Sciences and Engineering Council of Canada (NSERC). He also received an achievement award from the Association of Professional Engineers and Geoscientists of British Columbia (APEGBC).

Ricardo A. Aroca (S'06) received the B.S. (Hons) degree in electrical engineering from the University of Windsor, Canada, and the M.S. degree from the University of Toronto, Canada, in 2001 and 2004, respectively.

In 2000, he spent two 4-month internships with Nortel Networks in the Microelectronics Department. He is currently working toward the Ph.D. degree at the University of Toronto, where his research interests lie in the area of equalization and clock and data recovery techniques for 40- to 100-Gb/s wireline integrated circuits.

Mr. Aroca received the Natural Sciences and Engineering Research Council of Canada (NSERC) Postgraduate Scholarship award in 2002.

Peter Schvan (M'05) received the M.S. degree in physics and the Ph.D. degree in electronics in 1985.

Since joining Nortel, he has worked in the areas of device modeling, CMOS and BiCMOS technology development followed by circuit design for fiber optic and wireless communication using SiGe, BiCMOS, InP and CMOS technologies. Currently, he is leading a group designing analog components for high speed data transmission including 20 GS/s and above A/D and D/A converters. He has authored or co-authored over 20 publications.

Ming-Ta Yang (M'96) received the B.S and M.S. degrees in physics and applied physics from Chung-Yuan University, Chung -Li, Taiwan, in 1989 and 1992. During the 1989 academic year, he joined the Department of Physics, Chung-Yuan University, as a faculty member. In 1995, he received the Ph.D. degree in electrical engineering from the National Central University, Chung-Li, Taiwan. His Ph.D. dissertation was focused on the characterization and model of AlGaAs/InGaAs doped-channel heterostructure FETs and its application in monolithic microwave integrated circuits (MMICs).

In 1995, he joined Mosel Vitelic Inc., Hsin-Chu, Taiwan, where he worked on VLSI advanced technology development. He then joined the Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC) since 1998, where he set up a high-frequency characterization laboratory and organized a team to response for the development of characterization and Spice model both in the Mixed-Signal and RF applications. His current research interests include the development of advanced HF characterization and model of devices both in the RF CMOS and high-speed SiGe HBT BiCMOS technologies. He has served on the advisory Workshop Committees of Compact Modeling for RF/Microwave Applications (CMRF) in 2004 and 2005.

Sorin P. Voinigescu (M'90–SM'02) received the M.Sc. degree in electronics from the Polytechnic Institute of Bucharest, Bucharest, Romania, in 1984, and the Ph.D. degree in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 1994.

From 1984 to 1991, he worked in R&D and academia in Bucharest, Romania, where he designed and lectured on microwave semiconductor devices and integrated circuits. Between 1994 and 2002 he was with Nortel Networks and with Quake Technologies in Ottawa, ON, Canada, where he was responsible for projects in high-frequency characterization and statistical scalable compact model development for Si, SiGe, and III-V devices. He also led the design and product development of wireless and optical fiber building blocks and transceivers in these technologies. In 2000 he co-founded and was the CTO of Quake Technologies, the world's leading provider of 10 Gb Ethernet transceiver ICs. In September 2002, he joined the Department of Electrical and Computer Engineering, University of Toronto, as an Associate Professor. He has authored or co-authored over 80 refereed and invited technical papers spanning the simulation, modeling, design, and fabrication of high frequency semiconductor devices and circuits. His research and teaching interests focus on nanoscale semiconductor devices and their application in integrated circuits at frequencies up to and beyond 100 GHz.

Dr. Voinigescu received NORTEL's President Award for Innovation in 1996. He is a co-recipient of the Best Paper Award at the 2001 IEEE Custom Integrated Circuits Conference and at the 2005 Compound Semiconductor IC Symposium. His students have won Best Student Paper Awards at the 2004 IEEE VLSI Circuits Symposium, the 2006 SiRF Meeting, 2006 RFIC Symposium and 2006 BCTM.