LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35-μm CMOS

Andrea Boni, *Member, IEEE,* Andrea Pierazzi, and Davide Vecchi

***Abstract*—This paper presents the design and the implementation of input/output (I/O) interface circuits for Gb/s-per-pin operation, fully compatible with low-voltage differential signaling (LVDS) standard. Due to the differential transmission technique and the low voltage swing, LVDS allows high transmission speeds and low power consumption at the same time. In the proposed transmitter, the required tolerance on the dc output levels was achieved over process, temperature, and supply voltage variations with neither external components nor trimming procedures, by means of a closed-loop control circuit and an internal voltage reference. The proposed receiver implements a dual-gain-stage folded-cascode architecture which allows a 1.2-Gb/s transmission speed with the minimum common-mode and differential voltage at the input. The circuits were implemented in a 3.3-V 0.35-μm CMOS technology in a couple of test chips. Transmission operations up to 1.2 Gb/s with random data patterns and up to 2 Gb/s in asynchronous mode were demonstrated. The transmitter and receiver pad cells exhibit a power consumption of 43 and 33 mW, respectively.**

***Index Terms*—Back-plane drivers, CMOS integrated circuits, high-speed integrated circuits, input/output (I/O), low-power design, low-voltage differential signaling (LVDS).**

I. Introduction

THE EVER-increasing processing speed of microprocessor motherboards, optical transmission links, intelligent hubs and routers, etc., is pushing the off-chip data rate into the gigabits-per-second range. However, unlike internal clocks, chip-to-board signaling gains little benefit in terms of operating frequency from the increased silicon integration. In the last decade, high data rates were achieved by massive parallelism, with the disadvantages of increased complexity and cost for the IC package and the printed circuit board (PCB). For this reason, the off-chip data rate should move to the range of Gb/s-per-pin in the near future. Indeed, the SIA Silicon Roadmap [1] forecasts an off-chip frequency of 1 GHz for peripheral buses with the 100-nm generation (in 2006). Furthermore, while the reduction of the power consumption is of great concern in battery-powered portable systems, it is also required in other systems to reduce the costs related to packaging and additional cooling systems. Low-voltage differential signaling (LVDS) technology was developed in order to provide a low-power and low-voltage alternative [2], [3] to other high-speed I/O interfaces for point-to-point transmission, such as emitter-coupled logic (ECL) [4]–[5]. LVDS achieves significant power savings by means of a differential scheme for transmission and termination, in conjunction with a low voltage swing. LVDS standards pose relatively stringent requirements on the tolerance affecting the output levels, raising interesting design issues if low-cost solutions with neither external components nor trimming procedures are required. At the same time, the very large variation tolerated for the common-mode voltage at the input of a LVDS receiver requires several design improvements over the typical architecture if transmission speeds in the gigabits-per-second range must be achieved. It should be remarked that a recent standard [3] recommends a maximum data rate of 655 Mb/s, forecasting data rates of 1.5 Gb/s in the near future with low-loss media. At the moment, commercial LVDS chipsets are specified for operation in the megabits-per-second range [6]–[9].

This paper describes the design and the implementation of a complete LVDS I/O interface in 0.35-μm CMOS technology. The interface was tested up to 1.2 Gb/s with 8-bit random data patterns and up to 2 Gb/s in asynchronous mode. Complete compatibility of the output levels with the requirements of standards [2], [3] was achieved by means of an internal reference.

Manuscript received June 7, 2000; revised November 28, 2000.

The authors are with the Dipartimento di Ingegneria dell' Informazione, University of Parma, Parma I43100, Italy (e-mail: boni@ee.unipr.it).

Publisher Item Identifier S 0018-9200(01)02414-3.

II. LVDS Link

LVDS uses differential data transmission and the transmitter is configured as a switched-polarity current generator. A differential load resistor at the receiver end provides current-to-voltage conversion and optimum line matching at the same time, Fig. 1(a). For operation in the gigabits-per-second range, an additional termination resistor is usually placed at the source end to suppress reflected waves caused by crosstalk [10] or by imperfect termination, due to package parasitics and component tolerance, Fig. 1(b). Differential transmission greatly improves the robustness of the link to common-mode voltage bouncing (to be considered in the case of a cable as a transmission media) and crosstalk, therefore a reduced noise margin can be well tolerated. Indeed, LVDS uses a lower voltage swing than ECL, Table I, with further advantages in terms of reduced crosstalk and radiated electro-magnetic interference (EMI). From Fig. 1, the power saving achieved with LVDS against either differential or single-ended PECL is evident. Indeed, PECL exhibits an open-emitter output stage and requires a resistor (R_T) to $V_{DD} - 2$ V at the receiver end for line termination and biasing or a pull-down resistor (R_B) toward ground. Whichever termination arrangement is used, the open-emitter configuration and the larger voltage swing lead to a higher power consumption in a PECL link than in LVDS one.

A. Transmitter

A typical LVDS transmitter behaves as a current source with switched polarity. The output current flows through the load resistance, establishing the correct differential output voltage swing. The implemented transmitter, Fig. 2, uses the typical configurations with four MOS switches in bridge configuration, $M1 - 4$: with $M1$ and $M3$ switched on, the polarity of the

TABLE I
OUTPUT LEVELS FOR LVDS AND 100K PECL

	V_{OD_MIN}	V_{OD_MAX}	V_{OD_TYP}	V_{CM_MIN}	V_{CM_TYP}	V_{CM_MAX}
LVDS TX	0.250	-	0.450	1.125	-	1.375
LVDS RX	0.100	-	-	0.100	-	2.200
PECL TX	-	0.750	-	-	$V_{DD} - 1.330$	-

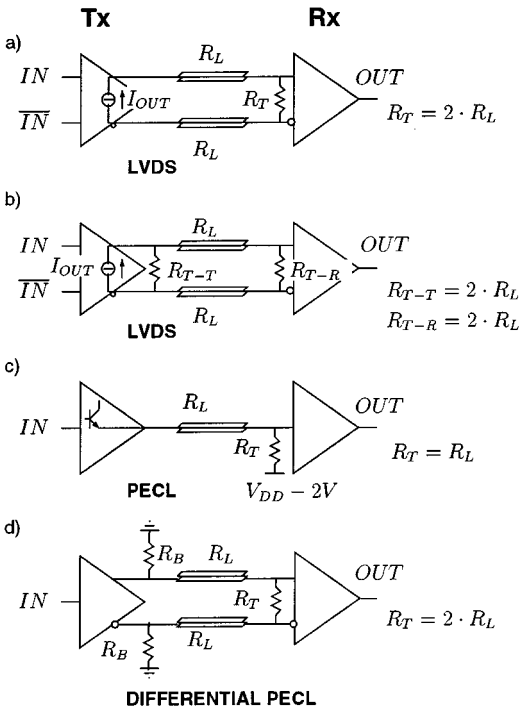

Fig. 1. Different solutions for high-speed data links. All the transmission lines, with the characteristic impedance R_L, are ground referenced. (a) Data link using LVDS with line termination at the receiver end. (b) LVDS link with termination at the receiver and source ends for gigabits-per-second operation. (c) Single-ended and (d) differential PECL links.

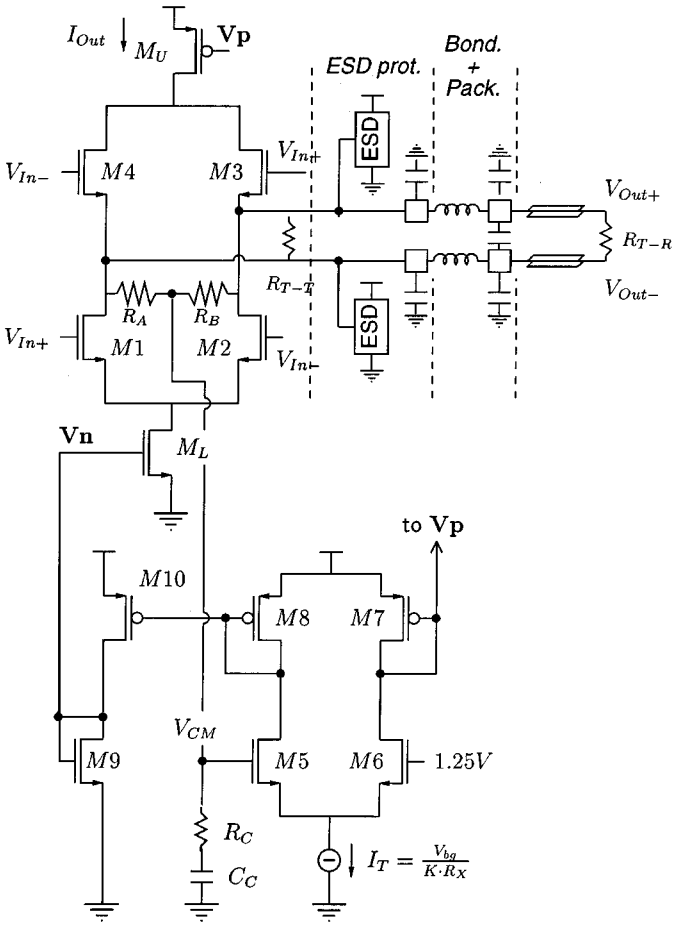

Fig. 2. Schematic diagram of the LVDS transmitter (top part) and the closed-loop control circuit (bottom part).

output current is positive together with the differential output voltage. On the contrary, if $M1$ and $M3$ are switched off, the polarity of the output current and voltage is reversed. Since the proposed transmission link is intended for operation in the gigabits-per-second range, the double termination scheme, Fig. 1(b), was used and the termination resistors were integrated in the transmitter (R_{T-T}) and in the receiver cell (R_{T-R}).

With a nominal 100-Ω load at the receiver, both the common-mode voltage and the differential swing at the output should fall within the LVDS standard specifications [2], [3] over the full range of process, supply voltage, 3 V $\div$ 3.6 V, and temperature variations, $-40\,^{\circ}\mathrm{C}$ $\div 125\,^{\circ}\mathrm{C}$ (PVT)

$$250\ \mathrm{mV} \le |V_{\mathrm{OD}}| \le 450\ \mathrm{mV} \quad (1)$$

$$1.125\ \mathrm{V} \le V_{\mathrm{CM}} \le 1.375\ \mathrm{V} \quad (2)$$

where V_{OD} and V_{CM} are the differential output voltage and the common-mode voltage at the transmitter output, respectively. Since this design aims at minimizing the PCB complexity and the production costs, external components and voltage references should be avoided together with wafer-level trimming. In order to define the correct output levels, a feedback loop across a replica of the transmitter circuit may be used [11], but in this case the effect of component mismatches between the transmitters and the replica should be carefully taken into account. Moreover, a reported reference circuit for LVDS buffers is unnecessary complicated and requires an external resistor and two reference voltages [12].

In order to achieve higher precision and lower circuit complexity, a simple low-power common-mode feedback control was implemented in the transmitter, Fig. 2, bottom part. The common-mode output voltage is sensed by means of a high resistive divider $R_A - R_B$ ($R_A = R_B = 100\ \mathrm{k}\Omega$) and compared with a 1.25-V reference by the differential amplifier $M5$–$M8$. The fraction of the tail current I_T flowing across $M7$ and $M8$ is mirrored to M_U and M_L, respectively, thus forcing $V_{\mathrm{CM}} \approx 1.25$ V. In order to develop the correct voltage swing on the 50-Ω load resistance ($R_{T-T}//R_{T-R}$), the bridge must be biased at $I_{\mathrm{Out}} = V_{\mathrm{OD_{nom}}}/50\ \Omega$. To this aim, I_T is set equal to I_{Out}/K, where K is the gain of current mirrors $M8 - M_L$ and $M7 - M_U$; a large

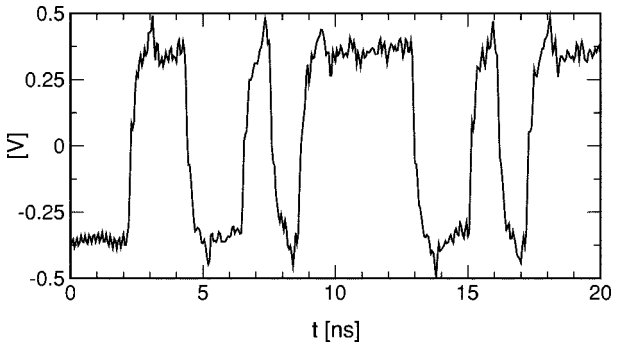

Fig. 3. Simulation of a differential signal transmitted over two 7-cm-long 50-Ω μ-strips. Chip-level parasitics, ESD protections, *LRC* package model and lossy transmission line model are included.

gain was used in order to make negligible the power consumption of the common-feedback circuit. Bias current I_T is obtained from a reference voltage provided by an internal bandgap, $V_{\rm BG}$, and an integrated resistor, R_X, i.e., $I_T = V_{\rm BG}/R_X$.

A large stability margin over PVT variations is achieved for the common-mode feedback by means of a pole-zero compensation network, $R_C - C_C$ ($R_C = 1.5$ kΩ and $C_C = 9.5$ pF).

The precision of the setting of the differential output voltage, $V_{\rm OD}$ depends on the tolerance affecting the bandgap voltage and resistors R_{T-T} (nominally 100 Ω) and R_X.

$$V_{\rm OD} \approx \frac{V_{\rm BG}}{R_X} \cdot 50\,\Omega \cdot \left(1 + \epsilon_{V_{\rm BG}} - \epsilon_{R_X} + \frac{\epsilon_{R_{T-T}}}{2}\right) \qquad (3)$$

under the hypothesis that the transmitter is loaded by a precise 100-Ω resistor (at the receiver). Since in the proposed design both R_{T-T} and R_X are polysilicon resistors of the same type, we can assume $\epsilon_{R_{T-T}} = \epsilon_{R_X}$, leading to

$$V_{\rm OD} \approx V_{\rm OD_{nom}} \cdot \left(1 + \epsilon_{V_{\rm BG}} - \frac{\epsilon_{R_X}}{2}\right). \qquad (4)$$

Therefore, integrating the R_{T-T} termination resistor halves the effect of the polysilicon resistivity tolerance on the output swing, with respect to the case of external termination resistor. It should be noted that implementing resistors R_{T-T} and R_{T-R} by gate-controlled MOS transistor arrays is an alternative solution which would allow flexible adjustment of the matching resistance. However, this would lead to an increased circuit complexity and raise problems in terms of electrostatic discharge (ESD) hardness.

In spite of the simplicity of the implemented control circuit, Monte Carlo simulations (process and mismatch level) at different supply voltages and temperatures demonstrate that both the output swing and the common-mode voltage are within the allowed LVDS tolerance for more than 90% of the simulation runs.

The proposed buffer was designed as a pad-cell with custom ESD protections, optimized for minimum load capacitance. The simulated typical capacitance contributed by the pad and the ESD protections is about 1.7 pF toward ground for each output. Fig. 3 shows a simulated differential signal transmitted over two 7-cm-long and 0.6-mm-large 50-Ω μ-strip lines (FR4 thickness is 360-μm). In the simulation a full back-annotated schematic of the transmitter (including ESD protections) was used together

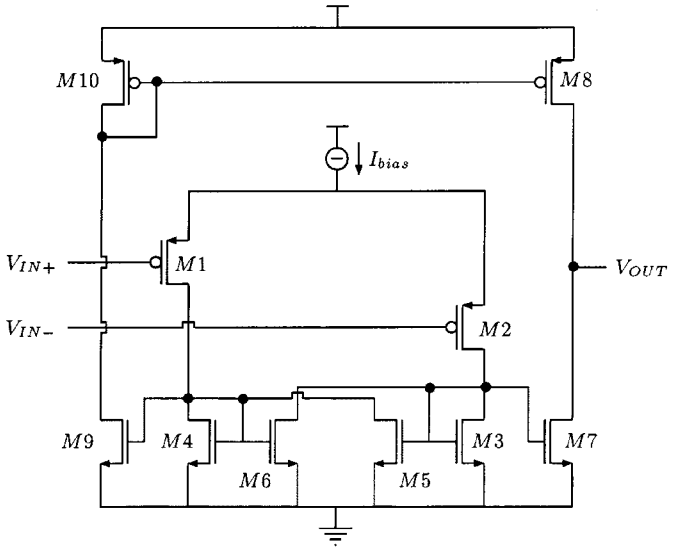

Fig. 4. Schematic diagram of a typical LVDS receiver.

with an *LRC* model of the package (28-pin plastic SOIC) used for the experiment. The μ-strips were modeled by a discrete lossy model (valid up to 10 GHz) generated by a dedicated software [13]. If loaded by a 10-pF external capacitance, the developed buffer achieves a maximum toggle frequency of 1 GHz. The implemented pad cell occupies an area of 0.175 mm^2 and exhibits a current consumption of 20 mA.

B. Receiver

A typical LVDS receiver is shown in Fig. 4 [14]. The differential voltage signal at the input is detected by a Schmitt trigger $M1 - M6$ which ensures a 25 mV $\div$ 50 mV hysteresis. Full-swing CMOS levels are obtained at the output, $V_{\rm OUT}$, by inverter $M7 - M8$. Even if this circuit performs satisfactorily with the typical LVDS common-mode voltage at the input, i.e., 1.25 V, several problems arise if the full variation of the common-mode voltage should be supported. In fact, the LVDS levels specified at the receiver input are [2]–[3]

$$|V_{\rm OD_{IN}}| \geq 100\,{\rm mV} \qquad (5)$$

$$100\,{\rm mV} \leq V_{\rm CM_{IN}} \leq 2.4\,{\rm V}. \qquad (6)$$

If low-threshold devices are not available, $M1$ and $M2$ enter in triode region when the input common-mode voltage approaches 100 mV, leading to a significant reduction of the voltage gain. The reduced voltage gain of the input amplifier may not be sufficient to properly drive the output inverter, so as to obtain a full CMOS swing at the output $V_{\rm Out}$.

In [15], a fully differential rail-to-rail input amplifier was used for accommodating the LVDS input range. However, that circuit is likely characterized by a higher power consumption since the common-mode output voltage is fixed by means of CMOS inverters with resistive feedback.

In the proposed LVDS receiver, Fig. 5, a large gain-bandwidth product independent on the input common-mode voltage is achieved by means of a folded-cascode input amplifier, $M1 - M6$, with resistive load, $R1 - R2$. The common-gate nMOS devices, $M5 - M6$, set a low dc voltage at the drain terminal of

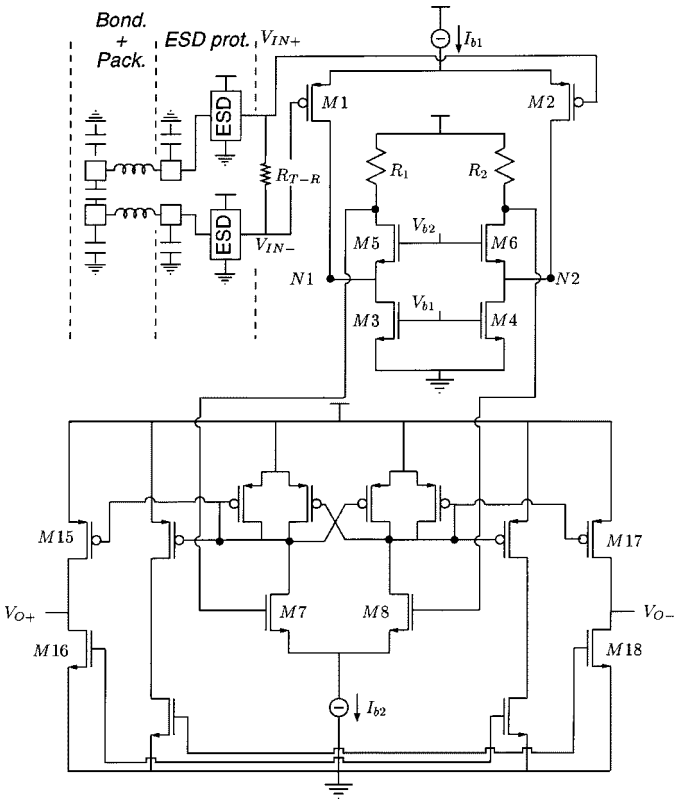

Fig. 5. Schematic diagram of the improved LVDS receiver supporting the full input range of the LVDS standard.

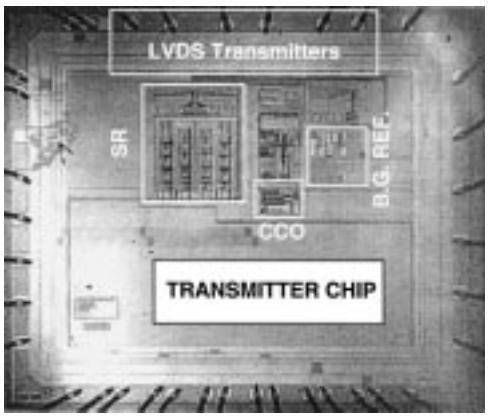

Fig. 6. Chip photograph of the transmitter chipset: SR is the serializer circuitry, CCO is the controlled oscillator, and B.G.REF. is the biasing circuitry.

$M1 - M2$, in order to keep the voltage gain almost insensitive to the input common-mode voltage. Since the input devices are designed with a large aspect ratio, in order to achieve a sufficient voltage gain, the impedance level at the drain of those devices is critical in order to obtain the required bandwidth. The problem is easily overcome by means of the cascode configuration, which ensures a low small-signal resistance at nodes $N1$ and $N2$. The value of the load resistors, $R1-R2$, is optimized so as to achieve at the same time the required voltage gain, bandwidth, and the correct common-mode voltage for the second differential gain stage. Since the aspect ratio of the nMOS input devices of the second stage is about one order of magnitude lower than the aspect ratio of $M1 - M2$, the impact of $R1 - R2$ on the overall bandwidth is quite limited. Biasing voltages V_{b1} and V_{b2} are set to 1.05 and 2.1 V, respectively (typical values). Input transistors, $M1$ and $M2$, experience a minimum source-to-drain voltage of about 250 mV with 0.1-V common-mode voltage at the input.

The second stage is a nMOS version of the typical LVDS receiver, Fig. 4, where the choice of pMOS input devices was mainly determined by the input common-mode range to be supported. In the proposed receiver, the use of nMOS input devices for the second stage has the advantage that the same voltage gain can be achieved with lower aspect ratios, thus providing a larger bandwidth. The implemented pad cell exhibits an area of about 0.08 mm^2 and a current consumption of 10 mA at 1 Gb/s.

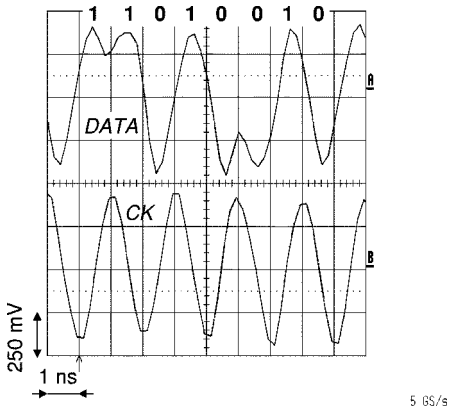

Fig. 7. Measured *CK* and *DATA* waveforms with a 11 010 010 pattern transmitted at 1 Gb/s.

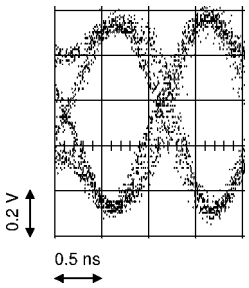

Fig. 8. Measured eye pattern at 1 Gb/s. The probe bandwidth is limited to 1 GHz.

III. Experimental Results

The two circuits were implemented in a couple of test chips in a 0.35-μm CMOS technology [16], Fig. 6. The transmitter is a serializer transmitting a 8-bit data burst with a 90° shifted clock reference over two pairs of 3-cm-long, 0.6-mm-large 50-$\Omega\,\mu$-strip lines (FR4 thickness is 360 μm). The transmission speed is set by means of an internal current-controlled oscillator. The receiver is a serial-to-parallel converter which allows to verify the performance of the proposed LVDS receiver. Measurements were performed up to 1.2 Gb/s with random data patterns. Fig. 7 shows the measured *CK* and *DATA* waveforms with a 11 010 010 pattern transmitted at 1 Gb/s, while the eye pattern at 1 Gb/s is shown in Fig. 8. A 1-GHz differential probe was used for the measurements.

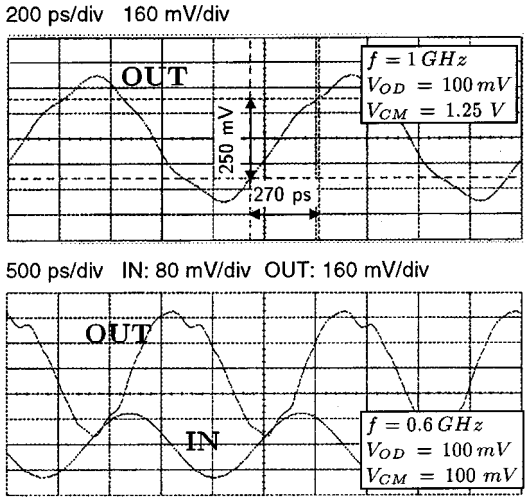

Fig. 9. Top: 1 GHz waveform measured at the output of the LVDS transmitter cell, with $V_{\rm OD} = 100$ mV and $V_{\rm CM} = 1.25$ V at the input of the LVDS receiver. Bottom: IN is the input sine-wave provided to the LVDS receiver, corresponding to worst case conditions ($V_{\rm OD} = 100$ mV and $V_{\rm CM} = 100$ mV) at 600 MHz and OUT is the correspondent LVDS output.

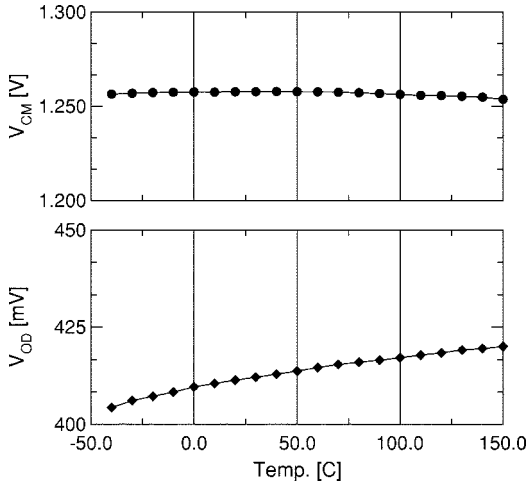

Fig. 10. Measured dc common-mode and differential output voltage of the implemented LVDS transmitter, over a ($-40\,^{\circ}$C to 150 °C) temperature range.

The receiver chip also includes a separate receiver and a transmitter, connected in series. A sine-wave synthesizer was interfaced to the receiver by means of a wide bandwidth central tapped transformer. A similar transformer and a 1 -m-long UT-141 semirigid cable were used to connect the transmitter to a 20-GHz bandwidth sampling scope. The measurement results are reported in Fig. 9: the top graph shows the measured output waveform at 1 GHz, i.e., 2 Gb/s, with $V_{\rm OD} = 100$ mV and $V_{\rm CM} = 1.25$ V at the input of the LVDS receiver. The measured rising and falling times are mainly determined by the limited bandwidth (about 900 MHz) of the transformer. The bottom graph shows the output and input waveforms at 600 MHz and with $V_{\rm OD} = 100$ mV and $V_{\rm CM} = 100$ mV at the input.

To verify the robustness of the proposed closed-loop bias control in the LVDS transmitter, Fig. 2, the dc output common-mode and differential voltages were measured over a large temperature range. The measurement results, Fig. 10, show correct LVDS output levels from $-40\,^{\circ}$C up to 150 °C.

TABLE II
PERFORMANCE SUMMARY OF THE LVDS TRANSMITTER AND RECEIVER

	TX	RX
Maximum Capacitive load (C_L)	10 pF	1 pF
Maximum Toggle Freq.	1GHz	600 MHz
DC Current Consumption	13 mA	10 mA
Maximum delay	800 ps	1.4 ns
DC I/O levels	[2], [3]	[2], [3]
Cell size	0.175 mm^2	0.081 mm^2

Table II reports a performance summary of the implemented pad cells.

IV. CONCLUSION

A complete transmission link fully compatible with the LVDS standards and implemented in a 0.35-μm CMOS technology was presented. Thanks to the differential transmission and the low voltage swing, a significant power saving is achieved with respect to conventional ECL circuits, but the reduced noise margin requires a tight control of the dc output levels over PVT variations. The proposed closed loop control at the transmitter provides fully compatible LVDS levels without resorting to external components or trimming procedures. The limits of the typical LVDS receiver were overcome by means of a double-stage folded cascode architecture featuring a maximum transmission speed of 1.2 Gb/s with minimum common-mode and differential input voltage.

ACKNOWLEDGMENT

The authors would like to thank Austria Mikro Systeme Int. AG for the specification, manufacturing, and testing of this design. In particular, the support of Dipl.-Ing. M. Manninger, Dipl.-Ing. R. Holzhaider, Dipl.-Ing. C. Trattler, Dipl.-Ing. Dr.techn. W. Meusburger is acknowledged. The authors are indebted to Prof. C. Morandi of University of Parma for fruitful discussions and critical review of the paper.

REFERENCES

[1] "The National Technology Roadmap for Semiconductors," Semiconductor Industry Associations, 1997.
[2] *IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI), 1596.3 SCI-LVDS Standard*, IEEE Std. 1596.3-1996, 1994.
[3] *Electrical characteristics of low-voltage differential-signalling (LVDS) interface circuits, TIA/EIA-644*, National Semiconductor Corp., ANSI/TIA/EIA, 1996.
[4] *F100K ECL user's handbook*, Fairchild Camera and Instrument Corp., 1982.
[5] *F100K ECL 300 series databook and design guide*, National Semiconductor Corp., 1992.
[6] *DS90LV031A 3V LVDS QUAD CMOS differential line driver datasheet*, National Semiconductor Corp., 1998.
[7] *DS90C032B LVDS QUAD CMOS differential line receiver datasheet*, National Semiconductor Corp., 1999.
[8] *DS90CR287 +3.3-V rising edge data strobe LVDS 28-bit channel 75-MHz datasheet*, National Semiconductor Corp., 1999.
[9] *SN55LVDS31, SN65LVDS31, SN65LVDS3487, SN65LVDS9638 high-speed differential line drivers datasheet*, Texas Instruments Inc., 1999.
[10] H. W. Johnson and M. Graham, *High-Speed Digital Design, A Handbook of Black Magic*. Englewood Cliffs, NJ: Prentice Hall, 1993.

[11] M. Steyaert, W. Bijker, P. Worekamp, and J. Sevenhans, "ECL-CMOS and CMOS-ECL interface in 1.2-μm CMOS for 150-MHz digital ECL data transmission systems," *IEEE J. Solid-State Circuits*, vol. 26, pp. 18–24, Jan. 1991.

[12] T. Gabara *et al.*, "LVDS I/O buffers with a controlled reference circuit," in *Proc. ASIC Conf.*, Sept. 1997, pp. 311–315.

[13] "Transmission line model generator (LMG)," in *IC 4.4.3 product documentation*. San Jose, CA: Cadence Design Systems, Inc., 1999.

[14] Y. Unekawa *et al.*, "A 5-Gb/s 8×8 ATM switch element CMOS LSI supporting five quality-of-service classes with 200-MHz LVDS interface," in *Proc. Int. Solid-State Circuits Conf.*, 1996, pp. 118–119.

[15] P. Xiao *et al.*, "A 500-Mb/s 20-channel CMOS laser diode array driver for a parallel optical bus," in *Proc. Int. Solid-State Circuits Conf.*, Feb. 1997, pp. 250–251.

[16] "0.35-μm CMOS process parameters," Austria Mikro Systeme Int. AG, Unterpremstätten, Austria, 1999.