Magnetic Tunnel Junctions for Spintronic Memories and Beyond

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(Invited Paper)

***Abstract*—In this paper, recent developments in magnetic tunnel junctions (MTJs) are reported with their potential impacts on integrated circuits. MTJs consist of two metal ferromagnets separated by a thin insulator and exhibit two resistances, low (R_P) or high (R_{AP}), depending on the relative direction of ferromagnet magnetizations, parallel (P) or antiparallel (AP), respectively. Tunnel magnetoresistance (TMR) ratios, defined as $(R_{AP} - R_P)/R_P$ as high as 361%, have been obtained in MTJs with $Co_{40}Fe_{40}B_{20}$ fixed and free layers made by sputtering with an industry-standard exchange-bias structure and postdeposition annealing at $T_a = 400$ °C. The corresponding output voltage swing ΔV is over 500 mV, which is five times greater than that of the conventional amorphous Al-O-barrier MTJs. The highest TMR ratio obtained so far is 500% in a pseudospin-valve MTJ annealed at $T_a = 475$ °C, showing a high potential of the current material system. In addition to this high-output voltage swing, current-induced magnetization switching (CIMS) takes place at the critical current densities (J_{co}) on the order of 10^6 A/cm^2 in these MgO-barrier MTJs. Furthermore, high antiferromagnetic coupling between the two CoFeB layers in a synthetic ferrimagnetic free layer has been shown to result in a high thermal-stability factor with a reduced J_{co} compared to single free-layer MTJs. The high TMR ratio enabled by the MgO-barrier MTJs, together with the demonstration of CIMS at a low J_{co}, allows development of not only scalable magnetoresistive random-access memory with feature sizes below 90 nm but also new memory-in-logic CMOS circuits that can overcome a number of bottlenecks in the current integrated-circuit architecture.**

***Index Terms*—CoFeB electrode, magnetoresistive random-access memories (MRAMs), memory-in-logic CMOS circuit, MgO barrier, spintronics, tunnel magnetoresistance (TMR).**

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I. Introduction

MAGNET-BASED nonvolatile memory, such as core memory, was once the choice of main memory of computers [1]. More compact and fast thin magnetic-film memories, developed subsequently that were supposed to be nonvolatile, suffered from creep of domain walls, a slow motion of the boundary of regions having different magnetization directions to reduce the magnetostatic energy, which resulted in loss of information [2]. Soon after, the position enjoyed by the magnetic memories was taken over by more stable and fast semiconductor memories.

Currently, we can define small magnetic elements by lithography, small enough that introduction of domain walls is energetically unfavorable: The domain-wall creep is no longer an issue. The individual magnetic element can also be made virtually nonvolatile; the cutting-edge hard-disk-drive (HDD) technology has proven that magnetic grains of less than 10 nm in diameter can retain its magnetization direction (the coded information) for more than ten years. We can encode these individual magnetic bits electrically and fast, either by external magnetic fields generated by an electrical current (magnetic-field write) [3], [4] or by a spin current produced by a flow of spin-polarized charge current in a magnetic structure (spin-injection write) [5], [6]. The write endurance is virtually unlimited in the former case, according to the knowledge accumulated by the HDD technology. We can read these magnetic bits electrically using magnetic tunnel junctions (MTJs), in which the junction resistance changes with its magnetization state, as shown in Fig. 1. Thus, putting all the existing technologies together in a one MTJ–one transistor (Tr) configuration (we still need a Tr switch to select a bit), one may expect to build a nonvolatile magnetoresistive random-access memory (MRAM) with the bit size of 10 nm, if the Tr can be reduced accordingly.

Fig. 2 shows the MRAM development trend with the International Roadmap for Semiconductors (ITRS) product technology trends for DRAM and Flash for comparison. Here, MRAM stands for those that employ the magnetic-field write, as shown in Fig. 1 [3], [4], [7]–[14], while SPRAM stands for MRAMs that employ the spin-current write [15], [16], which will be described later. Freescale has started shipping 4-Mb MRAM in June 2006 [17]. The trend shows a rapid growth of capacity per chip.

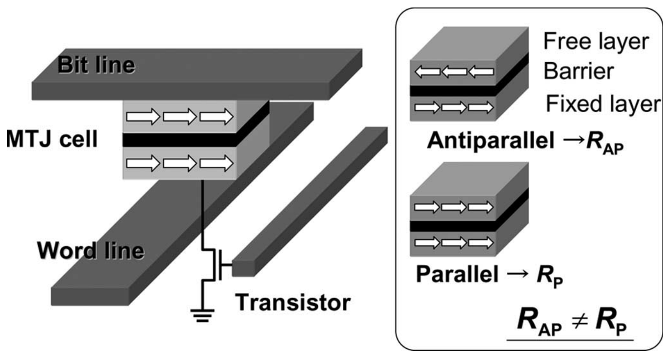

Fig. 1. Schematic diagram of a one MTJ–one Tr MRAM cell. The bit-line and the word-line currents together generate a magnetic field high enough to write a cell. For read operation, the bit-line and the (word) line connected to the Tr is used. Spin-injection write (see text) uses current passing through the MTJ; thus, it does not need the word-line. Right figure shows the two states of an MTJ. Free layer is the layer in which information is recorded. Fixed layer is engineered not to change its magnetization direction. A P magnetization configuration between the free layer and the fixed layer results (usually) in a low-resistance (R_P) state, while an AP configuration results in a high-resistance (R_{AP}) state.

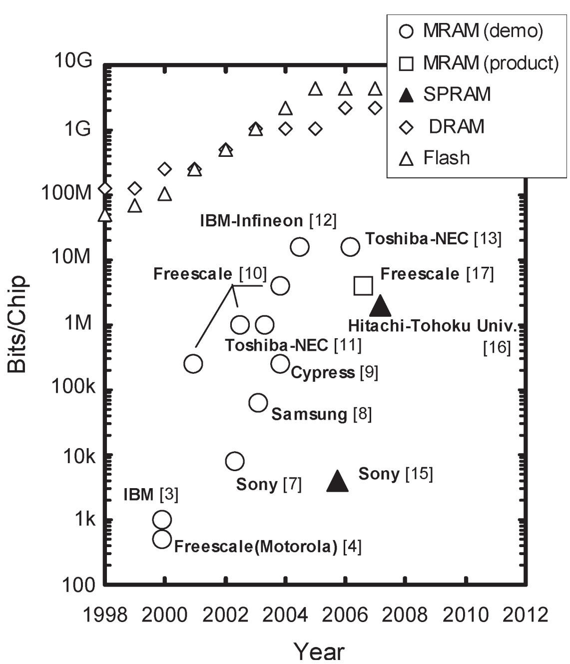

Fig. 2. MRAM development trend.

However, there have been two major obstacles to overcome before this approach becomes truly competitive at a gigabit scale and above. One is the output voltage of an MTJ; the maximum voltage swing produced by a conventional Al-O-barrier MTJ is, at most, 100 mV, not high enough to comfortably integrate them in a gigabit semiconductor circuitry. Another is its scalability. When magnetic fields generated by an electrical current are used to write the direction of a magnet (encoding), the required current increases with the reduction of the size of the magnet (keeping the thickness and magnetization the same). It becomes even more serious for those small magnetic elements designed to show a high thermal stability. The spin-current-write scheme is scalable; as the current needed to switch, a magnet reduces in proportion to the area of an MTJ, because the switching takes place at a certain threshold current density J_C. The problem is that the threshold current density has been generally high, on the order of 10^7–10^8 A/cm^2. As we will see in the later sections, the output-voltage barrier is now gone, and the second barrier, the high J_C, is being reduced considerably, both by the recent development of MgO-barrier MTJs. This new breed of MRAM, called SPRAM, Spin-RAM, or STT-RAM after its write scheme, still needs to go successfully through a number of check-points, which include the reliability of the insulator MgO for high endurance over 10^{15} and the uniformity of the barrier quality over a 300-mm wafer, before it becomes the major and indispensable technology of the semiconductor industry. However, once established, it appears that not only can it offer a fast, scalable, and nonvolatile memory with virtually unlimited endurance, which may not only dramatically reduce the power consumption of a chip, but also open a variety of new directions for integrated circuits. One of the new directions [18] is discussed in the last section of this paper.

II. Magnetic Tunnel Junctions

A. Brief History and Fundamentals of MTJ

An MTJ consists of two ferromagnets separated by a tunnel barrier and changes its resistance depending on the relative orientation of the two magnetization directions of the two magnets due to spin-dependent tunneling involved in the transport between the majority and minority spin states. This resistance change is called tunnel magnetoresistance (TMR), which is defined as $\Delta R/R = (R_{\mathrm{AP}} - R_P)/R_P$, where R_{AP} and R_P are the resistance for antiparallel (AP) and parallel (P) magnetization configurations between the two ferromagnets (see Fig. 1), respectively. In 1975, Julliere discovered TMR in an Fe/Ge/Co junction at low temperature; the TMR ratio was 14% [19]. Maekawa and Gafvert also succeeded in observing the TMR effect again at low temperatures in Ni/NiO/(Ni, Fe, or Co) junctions at the beginning of 1980 [20]. In 1995, the TMR ratios of over 10% at room temperature (RT) were reported in amorphous Al-oxide (Al-O)-barrier MTJs by two groups, Miyazaki and Tezuka at Tohoku University [21] and Moodera and coworkers at MIT [22]. Since these first RT demonstrations, many groups steadily improved the properties of Al-O-barrier MTJs, as shown in Fig. 3. The TMR ratio monotonically increased year by year and reached 70%. This is close to the limit of the TMR ratio expected from the Julliere's formula [19], in which the TMR ratio is given as $2P_1P_2/(1 - P_1P_2)$, where P_1 and P_2 are the spin polarization of the two magnetic layers. When one uses $P = 52\%$, measured at 0.2 K for CoFe [23], the TMR ratio becomes slightly over 70%, indicating that Al-O-based MTJs were reaching its limit, according to the simplest model. During the process of increasing the TMR ratio, a number of technologies have also been developed. These include spin-valve structure for stabilization of the AP configuration [24], optimization of ferromagnetic–electrode materials [7], [25]–[27], magnetic-field annealing [28], oxidization method [29], [30], and etching technique.

A typical unit structure of one MTJ–one Tr cell for MRAM is schematically shown in Fig. 1. A modern MTJ has a spin-valve structure (the layer stack, not shown in Fig. 1), which fixes

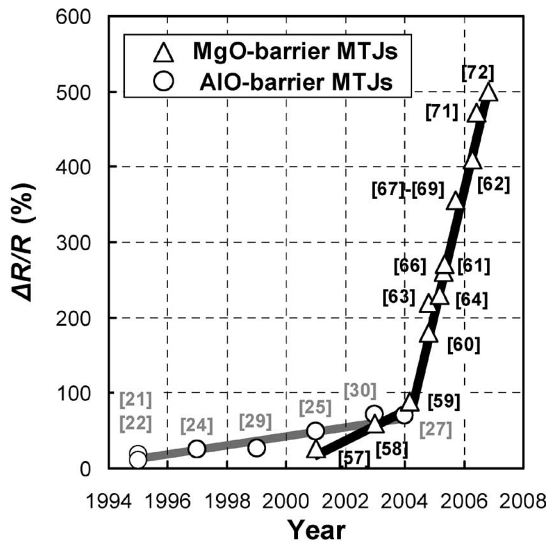

Fig. 3. Development of TMR ratio $(= \Delta R/R)$ for MTJs with Al-O and Mg-O tunnel barriers.

the magnetization direction of one of the ferromagnetic layer by the use of exchange interaction between the ferromagnetic layer and the neighboring antiferromagnetic layer; thus, the fixed layer is also called as the reference layer. The other ferromagnetic layer is the layer that changes its magnetization direction according to the input field/current and stores information, hence, called the free layer. Which of the top or bottom layer is fixed depends on the specific design of an MTJ.

B. Voltage Swing

To make the sensing circuit compatible with the ones used in DRAMs, the voltage swing ΔV of an MTJ needs to be $\Delta V \geq 200$ mV [31], [32]. Otherwise, more elaborate sensing circuitry has to be developed for the readout in the expense of speed. For an MTJ, ΔV for readout corresponds to absolute value of TMR ratio $\times V_P$ $(= |V_{\rm AP} - V_P|)$, where $V_{\rm AP}$ and V_P are the voltage for AP and P magnetization configurations, respectively. The TMR ratio is obtained at a constant bias current of $i = V_P/R_P$ $(= V_{\rm AP}/R_{\rm AP})$. As the bias voltage V_P increases (hereafter, we refer to it as V for simplicity, which corresponds to the horizontal axis of Fig. 4), the TMR ratio gradually decreases for the reasons not fully established at the moment [33]. As a result, ΔV first increases and then gradually decreases as V increases. This is shown in Fig. 4 for two different Al-O-barrier MTJs. In the case of a CoFe/Al-O/Co MTJ reported in one of the earliest reports [22], ΔV was about 10 mV. The ΔV for the MTJ with $Co_{75}Fe_{25}$/Al–O/$Co_{75}Fe_{25}$ spin-valve stacks [25] reached about 100 mV.

C. Write Current

Reduction of write current is one of the most critical factors to realize a small bit size while keeping the power consumption at a manageable level. Conventional magnetic-field writing is carried out by generating two "half-select" magnetic fields by electrical currents flowing through the word and bit lines, as depicted in Fig. 1. This allows one to access the free layer of the targeted MTJ, while keeping other MTJs intact. We note that considerable effort is required to reduce the distribution of the properties of MTJs to the level low enough for this scheme to be applicable even in the medium-scale integration [10].

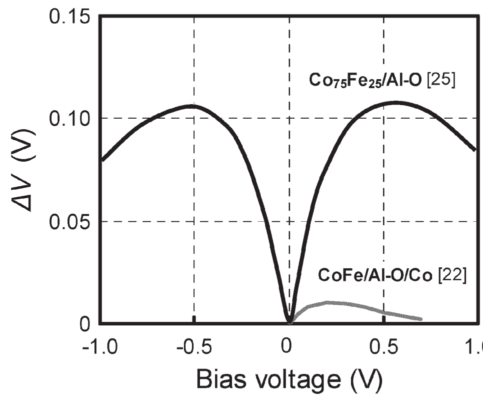

Fig. 4. Bias voltage dependence of the signal voltage ΔV for Al-O-barrier MTJs.

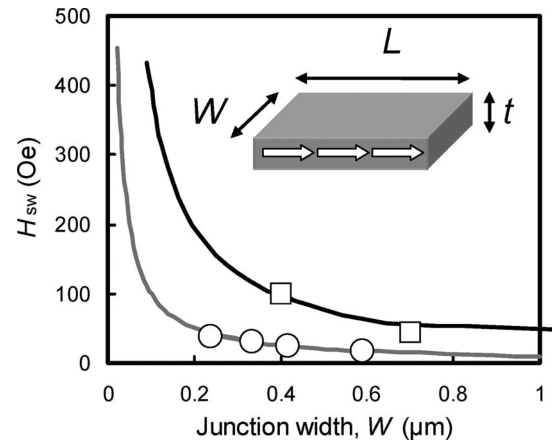

Fig. 5. $H_{\rm SW}$ as a function of junction width for single $Co_{90}Fe_{10}$ free layers with $t = 3$ nm and $k = (L/W) = 2$ (open square) and for $Ni_{81.5}Fe_{18.5}$ free layers with $t = 4$ nm and $k = 3$ (open circle).

The magnetic field $(H_{\rm sw})$ required to switch the free layer can be expressed as

$$H_{\rm sw} = CM_s t/W + H_k \tag{1}$$

where t and W are the free-layer thickness and the junction width, respectively, M_s is the saturation magnetization, C is a coefficient, and H_k is the anisotropy field, which includes the effect of crystal magnetic anisotropy and elastic magnetic anisotropy [34], [35]. Because there is not much room for reducing the thickness, (1) indicates that, eventually, $H_{\rm sw}$ becomes inversely proportional to W. As shown in Fig. 5, $H_{\rm sw}$ increases with reduction of W for 3-nm-thick $Co_{90}Fe_{10}$ magnetic layers with an aspect ratio $k = L/W = 2$ [35] and for 4-nm-thick $Ni_{81.5}Fe_{18.5}$ magnetic layers with $k = 3$ [36]. This shows that the write current (power consumption) for switching the free layer increases with increasing the density. The black solid line in Fig. 6 is the calculated value of write current required for conventional magnetic-field writing by using the

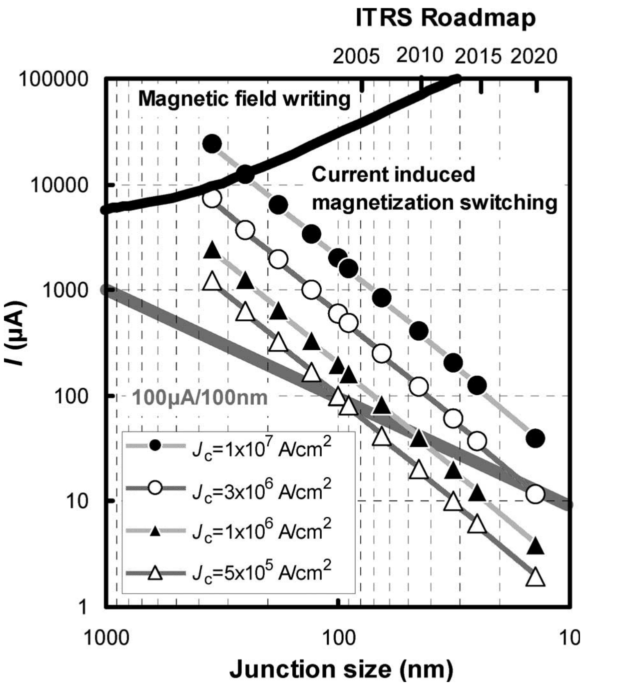

Fig. 6. Current required to observe CIMS as a function of junction size for four different critical current densities. The aspect ratio is assumed to be two. The black thick solid line shows the required current for the magnetic-field write. The gray thick line shows the current that a CMOS with the gate width equal to the junction size can provide (100 $\mu\mathrm{A}/100$ nm is assumed). The ITRS technology nodes are also shown. Symbols are guides for the eyes.

H_{sw} of the $\mathrm{Ni}_{81.5}\mathrm{Fe}_{18.5}$ layers in Fig. 5. Clearly, this is not scalable and one needs to find a different way of switching.

Theories developed by Slonczewski [5] and Berger [6] indicate that spin-polarized currents exert torque on magnetization and, eventually, may switch the magnetization direction once the current density become sufficiently high. This (spin-polarized) current-induced magnetization switching (CIMS) was first demonstrated on metallic current-perpendicular-to-plane giant magnetoresistance (CPP-GMR) pillars [37], [38] and later on MTJs. CIMS is scalable, because the required absolute current scales with the junction size of the MTJs. Assuming that the critical current density J_C for CIMS is independent on the junction size, the write current in the range of $J_C = 5 \times 10^5$–1×10^7 $\mathrm{A/cm^2}$ is calculated and plotted in Fig. 6, assuming the aspect ratio of two. As shown, in order for this approach to be viable in the 90-nm-technology node and beyond, J_C must be less than 10^6 $\mathrm{A/cm^2}$, as it has to be driven by a MOSFET that can deliver typically 100 $\mu\mathrm{A}/100$ nm gate width. This is also shown by a gray solid line in Fig. 6.

Fig. 7 shows the relationship between the TMR ratio $(= \Delta R/R)$ and $J_{C(C0)}$ in the devices for which CIMS were demonstrated (J_{C0} will be explained later). The Co/Cu/Co CPP-GMR nanopillars show J_C in the range of mid 10^6–10^8 $\mathrm{A/cm^2}$, depending on the employed structure, and exhibit magnetoresistance ratio of 0.5%–5% [37]–[43]. The Al-O-barrier MTJs have J_C similar to CCP-GMR pillars and exhibit TMR ratio of 10%–30% [44]–[47]. The MgO-barrier MTJs, which is the subject of the following section, have been shown to exhibit a high TMR ratio, together with CIMS, in a

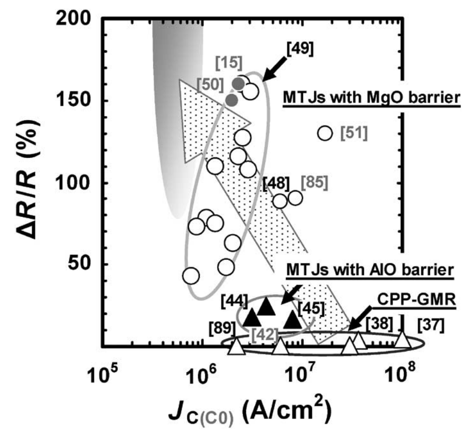

Fig. 7. Relationship between $\Delta R/R$ and critical current $J_{C(C0)}$ for the devices for which CIMS were demonstrated. The references, shown in black and gray, correspond to J_C (measured at RT at current pulsewidth ranging from 100 ms to 1 s) and J_{C0} [J_C at 1 ns (extrapolated), see text for details], respectively. The shaded area is the region of interest for MRAMs with CIMS writing.

wide range of $J_C = 8 \times 10^5$–2×10^7 $\mathrm{A/cm^2}$ [15], [48]–[51]. Note that J_C depends on the current pulsewidth as well. In order for this approach to be competitive, an MTJ has to show a low J_C on the order of 10^5 $\mathrm{A/cm^2}$ at reasonably fast pulsewidth and the TMR ratio of more than 150%, while not sacrificing the nonvolatility, i.e., the thermal stability. A high thermal-stability factor over 40 ($E/k_B T$, where E, k_B, and T are the energy potential between the two states, the Boltzmann constant, and temperature, respectively) is at least required, which corresponds to retention over ten years on a bit level.

III. MgO-Barrier MTJs

A. Emergence of MgO-Barrier MTJs

In 2001, Butler *et al.* [52] and Mathon and Umerski [53] pointed out the possibility of realizing high TMR ratios of 100% to even 1000% for fully ordered (001)-oriented Fe/MgO/Fe MTJs by calculations based on the first principle. The TMR ratios of body-centered cubic (bcc) Co (001) and FeCo (001) electrode systems were also predicted to be several times greater than the TMR ratio predicted for the Fe/MgO/Fe system [54]. The giant TMR originates from the fact that the electrons in highly spin-polarized Δ_1 band in (001) direction of bcc ferromagnetic electrodes can tunnel the MgO (001) barrier more easily than the electrons at other bands (Δ_2 and Δ_5). They have thus predicted that the effective spin-polarization of bulk bcc Fe, Co, and FeCo in the (001) direction can be dramatically enhanced by spin-filtering of a single-crystal MgO tunnel barrier [52]–[56].

It did not take too long to demonstrate these predictions experimentally [57], [58]. As shown in Fig. 3, the TMR ratio of 88% at RT was reported in 2004 by Yuasa *et al.* [59] for fully epitaxial Fe/MgO-barrier MTJs prepared using molecular beam epitaxy (MBE). This is higher than the highest reported for an Al-O-barrier MTJ (70%) [27]. Subsequent experiments have demonstrated giant TMR ratios of 180% and 410% in fully epitaxial Fe/MgO/Fe and Co/MgO/Co MTJs, respectively

[60]–[62], and of 220% in highly oriented (001) CoFe/MgO/CoFe MTJs [63]. Djavaprawira *et al.* demonstrated the TMR ratio of 230% for sputtered $Co_{60}Fe_{20}B_{20}/MgO/Co_{60}Fe_{20}B_{20}$ MTJs [64], [65], while Hayakawa *et al.* showed 260% for sputtered $Co_{40}Fe_{40}B_{20}/MgO/Co_{40}Fe_{40}B_{20}$ MTJs [66]. The latter developments are particularly notable because they deposited MTJs with a standard spin-valve structure on a thermal oxidized Si wafer using a conventional sputtering system and then annealed the MTJs to obtain a giant TMR ratio, starting from amorphous CoFeB ferromagnetic electrodes. It has also been demonstrated that the spin-valve-type MTJs with $Co_{40}Fe_{40}B_{20}/MgO/Co_{40}Fe_{40}B_{20}$ stack can show very high TMR ratios in a wide-resistance-area product RA, 27% at $RA = 0.8\ \Omega \cdot \mu m^2$ and over 361% from 500 to $10^5\ \Omega \cdot \mu m^2$ [67]–[69]. Recently, pseudo-spin valve MTJs with CoFeB/MgO/CoFeB stack are shown to exhibit a TMR ratio exceeding 450% [70], [71], reaching 500% at RT, and 1010% at 5 K [72]. These results were realized by direct sputtering of MgO, whereas other methods have been tried such as natural oxidation [73] and plasma oxidation [74]. It is worth noting that high TMR ratio over 100% can be obtained in MgO-based MTJs at temperatures as high as 300 °C [75].

For single-crystal Fe/MgO/Fe MTJs prepared by MBE, ΔV is reported to exceed 500 mV at the positive bias side, whereas it is 300 mV at the negative side [60]. This asymmetry is attributed to asymmetric structural defects such as dislocations at the interfaces and the lattice distortions generated during MBE growth. For sputtered $Co_{60}Fe_{20}B_{20}/MgO/Co_{60}Fe_{20}B_{20}$ MTJs, the reported ΔV is about 380 and 330 mV for the negative and positive bias, respectively [64]. By modifying the composition of the electrodes and sputter conditions, the ΔV in CoFeB/MgO/CoFeB MTJs is shown to reach 450–550 mV [66], [71], which is five times greater than that of Al-O-barrier MTJs and is high enough for many applications including high-density MRAMs. Employing a double-barrier structure has also been shown effective in increasing ΔV [76].

B. TMR Ratio of MgO-Barrier MTJs

To study the relationship between the TMR ratio and the structures as well as the processing conditions of MgO-barrier MTJs, we have fabricated systematically a number of MTJs and compared the TMR ratio, as summarized in Table I.

The MTJ multilayer structure studied here was Si/SiO_2 wafer/Ta(5)/Ru(50)/Ta(5)/NiFe(5)/MnIr(8)/CoFe(2)/Ru(0.8)/fixed layer(3)/MgO(1.5)/free layer(3)/Ta(5)/Ru(15) (in nanometers), deposited using RF magnetron sputtering, where $Co_{40}Fe_{40}B_{20}$, $Co_{20}Fe_{60}B_{20}$, $Co_{50}Fe_{50}$, and $Co_{90}Fe_{10}$ alloys (in atomic percent) were used for the fixed and free layers. Here, the bottom CoFe and the fixed layer are strongly coupled by an exchange interaction through Ru, the direction of which is stabilized by the underlying antiferromagnet MnIr. We also studied MTJs with modified structures: 1) $Co_{50}Fe_{50}(2.5)/Co_{40}Fe_{40}B_{20}$ (3) fixed layer, i.e., without the Ru spacer; 2) $Co_{40}Fe_{40}B_{20}(2)/Ni_{81}Fe_{19}(3)$ free layer instead of single free layer; and 3) a pseudospin-valve MTJ having a layer stack of Si/SiO_2 wafer/Ta(5)/Ru(20)/Ta(5)/$(Co_xFe_{100-x})_{80}B_{20}(4.3)$/MgO($t_{MgO}$)/$(Co_xFe_{100-x})_{80}B_{20}(4)$/Ta(5)/Ru(10). In CoFeB layer, the composition ratio x of Co and Fe was 25 at.% and 75 at.%. The MgO thickness t_{MgO} was varied from 1.5 to 2.1 nm. All MTJs were microfabricated by photolithography with a junction size of $0.8 \times 4.0\ \mu m^2$ and were annealed at $T_a = 250$ °C–500 °C in a vacuum under a field of 4 kOe. TMR ratios were measured using a dc four-probe method at RT in the magnetic-field range of ±1 kOe.

TABLE I
MAXIMUM TMR RATIO FOR THE MTJS WITH DIFFERENT REFERENCE AND FREE LAYERS ANNEALED AT OPTIMUM TEMPERATURE (T_a^{op}) THAT GIVES THE MAXIMUM TMR RATIO

Fixed layer	Free layer	T_a^{op} (°C)	TMR ratio (%)
$Co_{40}Fe_{40}B_{20}$	$Co_{40}Fe_{40}B_{20}$	400	355
$Co_{20}Fe_{60}B_{20}$	$Co_{20}Fe_{60}B_{20}$	400	351
$Co_{40}Fe_{40}B_{20}$	$Co_{50}Fe_{50}$	400	277
$Co_{40}Fe_{40}B_{20}$	$Co_{90}Fe_{10}$	350	131
$Co_{50}Fe_{50}$	$Co_{40}Fe_{40}B_{20}$	325	50
$Co_{50}Fe_{50}$	$Co_{50}Fe_{50}$	270	12
$Co_{90}Fe_{10}$	$Co_{40}Fe_{40}B_{20}$	300	75
$Co_{90}Fe_{10}$	$Co_{90}Fe_{10}$	270	53
$Co_{40}Fe_{40}B_{20}$	$Co_{40}Fe_{40}B_{20}$/NiFe	300	65
CoFe/$Co_{40}Fe_{40}B_{20}$	$Co_{20}Fe_{60}B_{20}$	325	181
(pseudo-spin valve)			
$Co_{40}Fe_{40}B_{20}$	$Co_{40}Fe_{40}B_{20}$	450	450
$Co_{20}Fe_{60}B_{20}$	$Co_{20}Fe_{60}B_{20}$	475	500

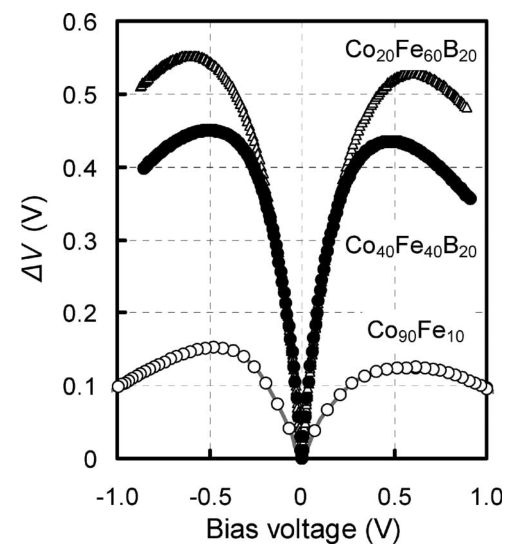

Fig. 8. Bias voltage dependence of the signal voltage ΔV for MgO-barrier MTJs with different ferromagnetic electrodes.

The maximum TMR ratio for the MgO-barrier MTJs with different fixed and free layers annealed at optimum temperature (T_a^{op}), defined as T_a that results in the highest TMR ratio, are summarized in Table I. The TMR ratio of the MTJ with $Co_{40}Fe_{40}B_{20}$ free and fixed layers increases with increasing T_a and reaches 355% at $T_a = 400$ °C. Similar TMR ratio of 351% is observed in the MTJs with $Co_{20}Fe_{60}B_{20}$. When $Co_{50}Fe_{50}$ or $Co_{90}Fe_{10}$ was used for the free and/or fixed layers, no giant TMR ratio was observed, e.g., for the MTJs with $Co_{40}Fe_{40}B_{20}$ free layer and $Co_{90}Fe_{10}$ fixed layer, the maximum TMR ratio was 75%. Fig. 8 shows the bias voltage dependence of the signal

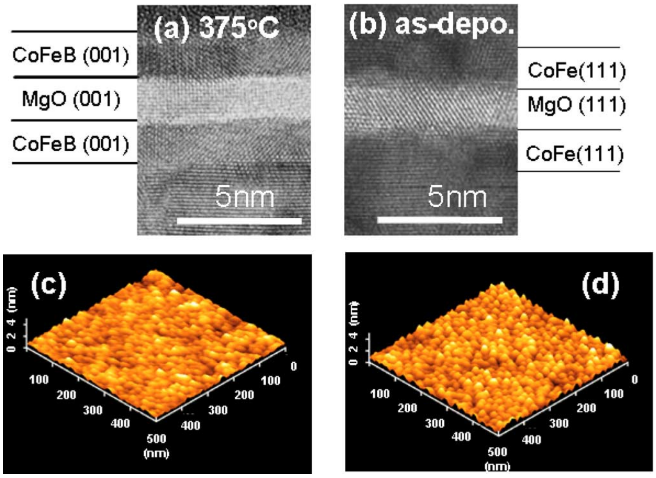

Fig. 9. Cross-sectional TEM images for (a) $Co_{40}Fe_{40}B_{20}$/MgO/$Co_{40}Fe_{40}B_{20}$ after annealing at 375 °C and (b) as-deposited $Co_{90}Fe_{10}$/MgO/$Co_{90}Fe_{10}$ junctions, and AFM images for Ta(5)/Ru(50)/Ta(5)/NiFe(5)/MnIr(8)/CoFe(2)/Ru(0.8)/X(3) samples consisting of $X =$ (c) $Co_{40}Fe_{40}B_{20}$ and (d) $Co_{90}Fe_{10}$.

voltage ΔV for MgO-barrier MTJs. The ΔV in the MTJ with the $Co_{40}Fe_{40}B_{20}$ free and fixed layers reached 450 mV. By increasing Fe concentration in the free and fixed layers, ΔV increases to 550 mV. MTJ with a $Co_{90}Fe_{10}$ fixed layer shows low ΔV of about 150 mV. High ΔV is not obtained only by adopting an oriented MgO-barrier but the combination with CoFeB electrodes is thus critical.

To understand the difference of the TMR ratios for the MTJs with different free and fixed layers, the crystalline structures and the surface morphology were measured using cross-sectional high-resolution transmission electron microscopy and atomic force microscope (AFM), respectively. A highly (001)-oriented MgO layer is found to form on the $Co_{40}Fe_{40}B_{20}$ amorphous fixed layer [64], [66]. Fig. 9(a) reveals that the MgO layer acts as a template for crystallization of initially amorphous $Co_{40}Fe_{40}B_{20}$ into highly (001)-oriented texture through annealing at high temperatures. When the underlying fixed layer forms an fcc (111)-oriented texture, as shown in Fig. 9(b), for the $Co_{90}Fe_{10}$ fixed layer, the MgO barrier also inherits the texture, resulting in low TMR ratio. The smooth surface of amorphous CoFeBe shown in Fig. 9(c) compared to CoFe [Fig. 9(d)] may also contribute to the (001)-textured MgO formation. Highly oriented (001) MgO barrier/$Co_{40}Fe_{40}B_{20}$ crystalline electrodes resulted in a high TMR ratio of 355%, whereas MTJs with polycrystalline fcc $Co_{90}Fe_{10}$ fixed layers did not show a high TMR ratio. This can be attributed to the absence of highly (001)-oriented MgO barrier/ferromagnetic electrodes. This supports the theoretical picture [52], [53] in which Δ_1 bands in bcc (001) electrodes and its selective tunneling in MgO (001) barrier are responsible for the high TMR.

Besides the fixed and free layers that are in direct contact with the MgO barrier, the TMR ratio depends critically on the way the layers are stacked. An MTJ that is composed of $Co_{40}Fe_{40}B_{20}(2)/Ni_{81}Fe_{19}(3)$ free layer showed a low TMR ratio of 65% at $T_a = 300$ °C, presumably because CoFeB under NiFe does not form a highly oriented (001) texture [77]. Another MTJ that is composed of $Co_{50}Fe_{50}(2.5)/Co_{40}Fe_{40}B_{20}(3)$ fixed layer without the Ru spacer exhibited a relatively low TMR ratio of 181% at $T_a = 325$ °C. This is because the as-deposited CoFe layer forms a bcc (110) texture, which acts as a template for the crystallization of the amorphous CoFeB layer during annealing [72]. A pseudospin-valve MTJ, in which the CoFeB layers are designed to crystallize only from the interface between the MgO barrier, has been shown to exhibit a high TMR of 500% at $T_a = 475$ °C. This shows that the engineering of the MTJ stack can result in an even higher TMR ratio in exchange-biased MTJs.

C. CIMS for MgO-Barrier MTJs

In order to fully utilize the potential of CoFeB/MgO/CoFeB MTJs for MRAM and other applications, reduction of the critical current density (J_C) for CIMS, while maintaining a high thermal-stability factor well over $E/k_BT = 40$, is necessary. While J_C is proportional to the product of magnetization and thickness (magnetic moment per area) in the free layer, the thermal-stability factor is proportional to the volume of the free layer. If one simply reduces the dimension of an MTJ to accommodate more bits on a given area, J_C remains constant, but the thermal-stability factor degrades. Synthetic ferrimagnetic (SyF) free layer, consisting of two ferromagnetic layers separated by Ru spacer, is expected to provide a high volume to withstand thermal fluctuations [78]–[81] while keeping the effective magnetic moment per area low. Previous study on CIMS in CPP-GMR nanopillars with SyF free layers reported J_C lower than that of conventional single free-layer MTJs [82]. We have thus investigated SyF free layers for CoFeB/MgO/CoFeB MTJs.

The MTJ film-layer structure studied was, starting from the substrate side, Ta(5)/Ru(50)/Ta(5)/NiFe(5)/MnIr(8)/CoFe(4)/Ru(0.8)/$Co_{40}Fe_{40}B_{20}(5)$/MgO(0.9)/$Co_{40}Fe_{40}B_{20}(2)$/Ru(0.7)/$Co_{40}Fe_{40}B_{20}(2)$/Ta(5)/Ru(5) (in nanometers). The nanopatterned MTJs with the dimension of 80×160 nm^2 were annealed at a temperature of 300 °C for 1 h under a magnetic field of 4 kOe. Again, the TMR loops of the MTJs were measured at RT using a four-probe method with a dc bias and a magnetic field of up to 1 kOe. CIMS was evaluated by measuring resistance by 50-μA-step current pulses with the pulse duration (τ_p) varying from 100 μs to 1 s. The current direction is defined as positive when the electrons flow from the top (free) to the bottom (fixed) layer.

Fig. 10(a) and (b) show the R–H loop and the R versus pulsed current I_p with $\tau_p = 10$ ms under an applied magnetic field of -32 Oe of SyF free MTJ with Ru (0.7) spacer, respectively. The TMR ratio is 90% comparable to the one reported for an MTJ with a 2-nm CoFeB single free layer [49]. The static bias field of -32 Oe was applied along the direction of the fixed CoFeB layer to compensate the offset field arising primarily from the stray fields of the edge of the patterned SyF pinned layer [see Fig. 10(a)]. The average critical current density ($J_C^{\mathrm{ave}} = (J_C^{\mathrm{P->AP}} - J_C^{\mathrm{AP->P}})/2$) to switch the magnetization is 6.8×10^6 A/cm^2 at $\tau_p = 10$ ms. Fig. 10(c) shows J_C^{ave} as a function of $\ln(\tau_p/\tau_0)$ for τ_p from 100 μs to 1 s. The intrinsic critical current density J_{c0} and the thermal-stability factor E/k_BT can be determined from this plot by

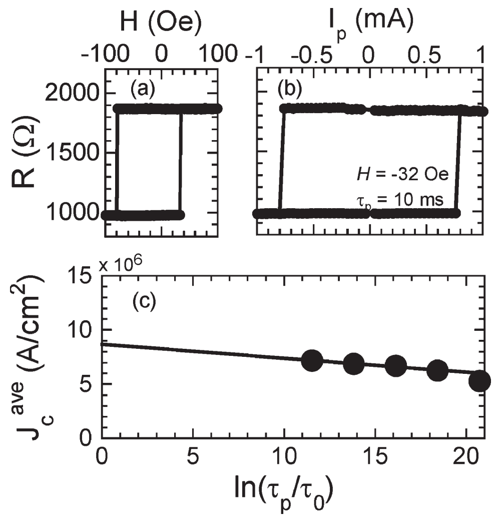

Fig. 10. (a) Resistance (R) versus magnetic-field (H) loops, (b) R versus pulsed current (I_p) loops at τ_p of 10 ms, and (c) the average critical current density $J_c^{\rm ave}$ $((J_c^{\rm P->AP} - J_c^{\rm AP->P})/2)$ as functions of $\ln(\tau_p/\tau_0)$ at RT for an MTJ with a CoFeB(2 nm)/Ru(0.7 nm)/CoFeB(2 nm) SyF free layer.

using the following Slonczewski's model [5] taking into account the thermal-activated nature of the magnetization switching [83], [84]:

$$J_C = J_{C0}\left\{1 - (k_BT/E)\ln(\tau_p/\tau_0)\right\} \quad (2)$$

$$J_{C0} = \alpha\gamma e M_s t(H_{\rm ext} \pm H_k \pm H_d)/\mu_B {\rm g} \quad (3)$$

$$E = M_s V H_k/2 \quad (4)$$

$$ {\rm g} = P/\left[2(1+(P^2\cos\theta)\right] \quad (5)$$

where α is the Gilbert damping coefficient, γ is the gyromagnetic constant, e is the elementary charge, t is the thickness of the free layer, $H_{\rm ext}$ is the external magnetic field, H_k is the in-plane uniaxial magnetic anisotropy, M_s is the saturation magnetization of the free layer, V is the volume of the free layer, H_d is the out-of-plane magnetic anisotropy induced by the demagnetization field, and P is the spin polarization. θ is zero for the P configuration and π for AP.

Using (2), one can determine E/k_BT from the slope of Fig. 10(c) to be 67. By extrapolating J_C to $\ln(\tau_p/\tau_0) = 0$, which corresponds to $\tau_p = 1$ ns (the inverse of ferromagnetic-resonance frequency at zero field), we obtain J_{C0} of 8.7×10^6 A/cm^2. For comparison, we performed the same measurements on MTJs with the 2.2- and 2.5-nm-thick single free layers [i.e., Ta(5)/Ru(50)/Ta(5)/NiFe(5)/MnIr(8)/CoFe(4)/Ru(0.8)/$Co_{40}Fe_{40}B_{20}$(5)/MgO(0.9)/$Co_{40}Fe_{40}B_{20}$(2.2, 2.5)/Ta(5)/Ru(5)]. Here, J_{C0} and E/k_BT were 7.6×10^6 A/cm^2 and 27 for the 2.2-nm MTJ, and 8.4×10^6 A/cm^2 and 36 for the 2.5-nm one, respectively. Having these numbers and using (2) and (4), we can evaluate J_{C0} and E/k_BT of an MTJ with a 4-nm-thick single free layer, i.e., of an MTJ that has a single free layer with the CoFeB thickness equal to the sum of the two CoFeB layers in the SyF free layer. This turned out to be 2.0×10^7 A/cm^2 and 56, respectively. It indicates that employing a SyF free layer increases E/k_BT as expected, with reduction of J_{C0} as compared to the equivalent single free MTJ. The enhanced E/k_BT is believed to be a result of high coercivity H_c and strong exchange coupling [85]. The origin of the reduction of $J_{C0}^{\rm ave}$ is not fully understood but it may be due to spin-accumulation in the free layer. Two antiferromagnetically coupled CoFeB layers, separated by a nonmagnetic Ru layer whose thickness is much thinner than the spin-diffusion length [86], are known to enhance the spin accumulation at the CoFeB and Ru interface [41], [87]–[89]. Spin accumulation can increase the efficiency of spin-torque acting on the CoFeB free layer and can contribute to the reduction of critical current density.

Although further reduction of J_{C0} is necessary to realize a current density below 10^6 A/cm^2, while maintaining the high thermal stability (i.e., high E/k_BT) for MRAM applications, there are a number of strategies one can employ to reduce J_{C0}. These include 1) dual-spin-filter structure consisting of a free layer sandwiched between the two fixed layers having opposite magnetization configuration, which can enhance the spin accumulation [90], [91], 2) reduction of M_s and α by adding other elements to CoFeB or by employing new magnetic materials [92]–[94], 3) employing a controlled pulse shape to realize precharging [95], 4) the use of a nanoaperture structure [96], 5) the use of perpendicular easy-axis [97], and 6) the use of a magnetic-field assisted CIMS [98], [99].

Finally, we note that there are two things to be established before fully exploiting the potential of CIMS for MRAM applications. One is the endurance of MTJs under CIMS. Although 10^{12} has already been shown [15], owing to the relatively low voltage for switching, one needs to demonstrate beyond 10^{15} to call it virtually unlimited. For this, we need to identify and control the failure modes. We also need to understand and control the stochastic nature of switching, particularly at the short pulse duration, where the switching is no longer thermally activated [83], [100], i.e., switching probability is a function of current-pulse magnitude, polarity, and duration [99].

IV. MTJ-Based CMOS Logic Circuit

By employing MgO-based MTJs, we have shown that one can achieve a high voltage swing and a scalable switching. The remaining technology issues have been outlined in the last part of the preceding section. Once established, the fast nonvolatile memory with high endurance will not only be a critical ingredient for the reduction of the static power of the advanced very large-scale integration (VLSI) but it will also open new possibilities of overcoming bottlenecks that are present in the current VLSI architecture, one of which is the MTJ-based CMOS logic circuits discussed in this section.

Since an MTJ is a variable two-level resistor, a logic circuit can be built having the logical AND and OR operations between an external input and an internal input stored in an MTJ by series and parallel connection of MTJs and MOS Trs [18]. Arbitrary logic functions with multiple-input variables can be realized by using such an MTJ-based logic-in-memory circuit where storage elements are distributed over a CMOS logic-circuit plane. This approach has been shown to be capable of reducing an effective silicon area and the total leakage

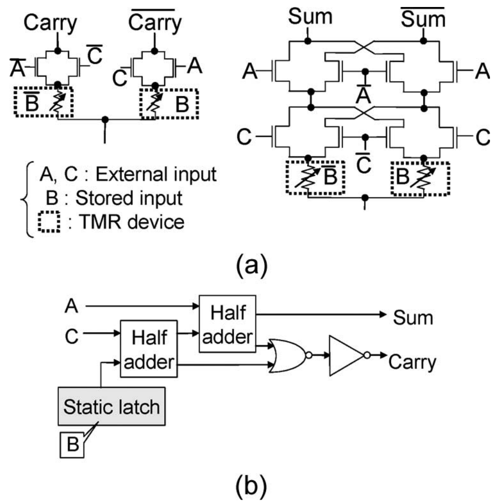

Fig. 11. Full adders. (a) TMR-based full adder. (b) CMOS full adder.

TABLE II
COMPARISON OF FULL ADDERS

	CMOS	TMR-based
Delay	310ps	310ps
Device counts	40Tr.	24Tr.+2C
Dynamic power	51μW	16μW
Static power	55nW	0.084nW

(0.18μm TMR/CMOS, V_{DD}=1.8V)

current [101]–[106]. The use of a dynamic current-mode-logic (DyCML) circuit [107] makes it possible to perform a high-speed switching operation in the MTJ-based logic network with less static power dissipation. As a typical example of an MTJ-based logic circuit, an MTJ-based full adder has been designed, as shown in Fig. 11(a), where a stored inputs B and B− are directly represented by the resistances of MTJs. Since storage functions are compactly integrated into a logic-circuit network by using MTJs, the total number of Trs in the full adder has been greatly reduced, where the area penalty of the MTJs is not existent because MTJs are stacked on the MOS-Tr plane. Therefore, one can view them as a functional interconnect. Furthermore, the combination of MTJ-based nonvolatile storage elements and DyCML circuit makes it possible to reduce the power dissipation of the designed MTJ-based logic network compared to corresponding CMOS implementation indicated in Fig. 11(b). Table II summarizes the comparison of full adders under a 0.18-μm TMR/CMOS technology. In this evaluation, the minimum and maximum resistances of TMR devices are set to be 60 and 90 kΩ, respectively, i.e., the MR ratio used here is 50%. The total number of Trs, the dynamic power dissipation, and the static power dissipation are reduced to 60%, 31%, and 0.15%, respectively, of the corresponding CMOS counterpart. The static power dissipation becomes zero if the power supply is removed at the standby mode.

The implementation of the MTJ-based CMOS logic-circuit network depends on the MR ratio of MTJs. When the MR ratio becomes sufficiently high, the total Tr counts can further

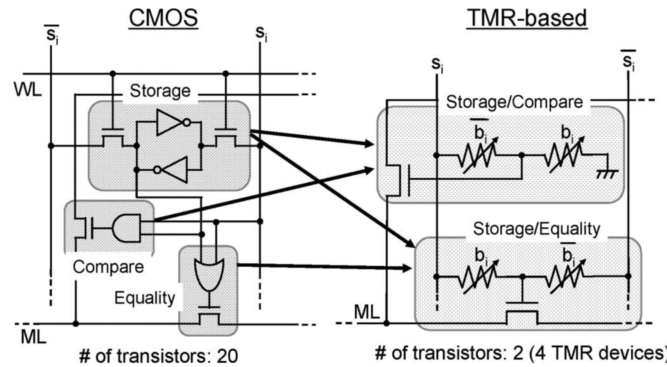

Fig. 12. Design example of CAM cell circuits.

TABLE III
COMPARISON OF 16-b-WORD CAMS

		CMOS	TMR-based
Delay (ns)		0.69	0.61
Power (μW)	Dynamic	275	193
	Static	16.2	0
# of transistors		5	1

(MR ratio: 1000%)

be reduced, because the output of an MTJ network can be directly used as an input of a MOS-Tr network. For example, Fig. 12 shows a 1-b cell circuit in a fully P content-addressable memory (CAM), where magnitude comparison between an input word and stored words in a CAM is performed in a bit- and word-parallel fashion [18], [108]–[111]. Two kinds of logic functions, 1-b magnitude comparison and equality operations are performed in each CAM cell. Here, the TMR-ratio is assumed to be 1000%. The use of the MTJ-based logic circuit makes a cell circuit compact. Since the leakage-current path is also reduced by using the MTJ-based logic circuit, the static power dissipation can be reduced dramatically. Table III summarizes the comparison of 16-b-word CMAs under a 0.18-μm TMR/CMOS technology.

These evaluations show that the use of high TMR MTJs is a promising pathway for realizing a compact hardware and static power saving that allows us to overcome the bottleneck arising from the long interconnects in the current VLSI.

V. CONCLUSION

We have shown that MgO-barrier-based MTJs show a very high TMR ratio and a low J_C for CIMS. The TMR ratio in an MTJ with sputtered $Co_{40}Fe_{40}B_{20}$ fixed and free layers using industry-standard exchange-bias structure reached 361% at the postdeposition annealing temperature of $T_a = 400$ °C. The ΔV in the MTJ reached 550 mV, which is more than five times than that of MTJs with amorphous Al-O barriers. The key to realize a high TMR ratio is shown to have highly oriented (001)-MgO-barrier/CoFeB crystalline electrodes. The highest TMR ratio, obtained so far in this system, is 500% at $T_a = 475$ °C in a pseudospin-valve MTJ. We found that high antiferromagnetic coupling between the two CoFeB layers in a SyF free layer results in reduced J_{C0} in CIMS with high

E/k_BT compared to single free-layer MTJs. Memory-in-logic CMOS architecture using MgO-based MTJ is also presented, which may overcome a number of bottlenecks present in the current integrated circuits.

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