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Magnetotransport Properties of Epitaxial Ge/AlAs Heterostructures Integrated on GaAs and Silicon

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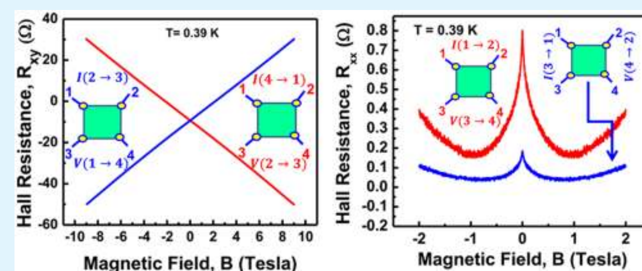
ABSTRACT: The magnetotransport properties of epitaxial Ge/AlAs heterostructures with different growth conditions and substrate architectures have been studied under ±9 T magnetic field and at 390 mK temperature. Systematic mobility measurements of germanium (Ge) epilayers grown on GaAs substrates at growth temperatures from 350 to 450 °C allow us to extract a precise growth window for device-quality Ge, corroborated by structural and morphological properties. Our results on Si substrate using a composite metamorphic AlAs/GaAs buffer at 400 °C Ge growth temperature, show that the Ge/AlAs system can be tailored to have a single carrier transport while keeping the charge solely in the Ge layer. Single carrier transport confined to the Ge layer is demonstrated by the weak-localization quantum correction to the conductivity observed at low magnetic fields and 390 mK temperature. The weak localization effect points to a near-absence of spin−orbit interaction for carriers in the electronically active layer and is used here for the first time to pinpoint Ge as this active layer. Thus, the epitaxial Ge grown on Si using AlAs/GaAs buffer architecture is a promising candidate for next-generation energy-efficient fin field-effect transistor applications.



KEYWORDS: *germanium, transport, epitaxy, molecular beam epitaxy, heterostructure*

INTRODUCTION

Germanium (Ge) is an attractive material due to its higher electron and hole mobilities than silicon (Si) for future generation low-power and high-speed nanoscale logic transistors. In the last several decades, transistors using Ge directly deposited on Si,[1,2] Ge on Si using graded SiGe buffer,[3,4] Ge-on-insulator-on-Si (GeOI) by bonding,[5] compressively strained Ge in a quantum well (QW) configuration on Si,[6] and bulk Ge,[7] all have been studied. Yet these methods have not achieved higher valence band and conduction band offsets for carrier confinement. Very recently, epitaxial Ge heterogeneously integrated on Si using composite metamorphic AlAs/GaAs buffers[8,9] obtained by molecular beam epitaxy (MBE) illustrated a promising path to understand the effect of growth temperature, the role of an AlAs buffer layer underneath the Ge layer and their effect on the magnetotransport properties of epitaxial Ge. It has been well-documented that the large bandgap semiconductor buffer layers such as GaAs, InAlAs,[10,11] or oxide buffer layer[12] can be considered to eliminate the parallel conduction either from the substrate or through the buffer layer to the active device layer of interest. For example, in a metamorphic InGaAs QW transistor structure on Si, the composite GaAs/$In_xAl_{1-x}As$ buffer eliminates the parasitic conduction to the active InGaAs channel.[10,11] In order to achieve a device-quality epitaxial Ge layer on large bandgap buffer, it is necessary to understand the role of the buffer layer, the growth temperature, and the growth pause that provides the film quality.

The temperature-dependent mobility as measured by the van der Pauw technique and subsequent analysis by the quantitative mobility spectrum (QMSA) are often used to determine the (1) channel mobility, (2) parallel conduction to active channel, and (3) the carrier freeze-out for high mobility III−V materials.[10,11,13,14] However, the QMSA method fails for materials with mobility below 1000 $cm^2/(V\ s)$. Therefore, it is necessary to find an alternative way to determine the mobility and carrier density contributed solely by the Ge layer grown on a large bandgap material, such as AlAs, where carriers are confined within the Ge layer. Furthermore, a well-controlled heterointerface between the epitaxial Ge and the large bandgap AlAs buffer layer is crucial to realize high-performance nanoscale Ge transistors. Here, we report on the growth by MBE of a series of Ge/AlAs/GaAs structures as well as a Ge/AlAs/GaAs/Si structure and their characterization. In particular, we discuss the effect of (1) the AlAs buffer layer, (2) the duration of the growth pause, (3) the growth temperature, (4) the different annealing temperatures, and (5) the reliability of repeated mobility measurements from 90 to 315 K of the Ge layers. The structures were grown using two solid-source MBE chambers, connected via an ultrahigh vacuum transfer chamber. We also note that the in situ growth process of Ge following

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the large bandgap AlAs buffer is mandatory since the AlAs layer is prone to oxidize once removed from the ultrahigh vacuum chamber prior to epitaxial Ge layer growth. The Ge/AlAs/GaAs/Si structure was characterized at low temperatures (down to 390 mK) under magnetic fields up to 9 T to investigate the carrier transport behavior inside the Ge layer. The magneto-transport measurements demonstrate single carrier confinement inside the Ge layer. Furthermore, the Ge/AlAs/GaAs/Si structure exhibited weak-localization, pointing to a near absence of spin−orbit interaction. This observation in turn suggests that only carriers within the Ge layer contribute to transport. The weak localization quantum correction to the conductivity was obtained by careful sweeps of the magnetic field at the lowest measurement temperatures. Furthermore, X-ray analysis was performed to ascertain interface quality, surface morphology was visualized by atomic force microscopy (AFM), and defect/interface properties were evaluated using cross-sectional transmission electron microscopy (TEM), all to establish pathways for Ge based materials and their device structures.

RESULTS AND DISCUSSION

Structural Analysis of Epitaxial Ge on GaAs with AlAs Buffer. Figure 1 shows the schematic of layer structures

(a)	(b)
80 nm Ge (350°C, 400°C, 450°C)	240 nm Ge (400°C)
170 nm AlAs	170 nm AlAs
250 nm GaAs	2.0 μm GaAs
(100)/2° GaAs (a)	(100)/6° Si (b)

Figure 1. Schematic of epitaxial Ge layers grown on (a) GaAs and (b) Si substrates, respectively. Ge epitaxial layers were grown at 350, 400, and 450 °C on GaAs substrate, and at 400 °C on Si substrate.

studied in this work. The 80 nm epitaxial Ge layers were grown on semi-insulating (100)/2° offcut GaAs substrates at growth temperatures of 350, 400, and 450 °C with the growth rate of approximately 25 nm/h. The growth temperature in this study refers to thermocouple temperature during growth. The low growth rate was selected to prevent interdiffusion at the Ge/AlAs heterointerface.[8,9] The 240 nm Ge layer was grown on (100)/6° Si substrate using the composite metamorphic AlAs/GaAs buffer shown in Figure 1b. The detailed material analysis of Ge on Si using AlAs/GaAs buffer was reported earlier.[8] The structural quality and the relaxation state of each Ge layer structure on GaAs were evaluated using high-resolution (004) X-ray rocking curves as shown in Figure 2. The peak positions of Ge, AlAs, and GaAs substrate are clearly visible in these figures. The angular separation $\Delta\theta$ between the (004) diffraction peaks of GaAs and Ge resulting from the difference in lattice plane spacing $\Delta d/d$ can also provide the micro-structural quality. Both the AlAs and Ge peak positions with respect to the GaAs substrate attest to the lattice matched nature of the layer structure, as expected. The full width at half-maximum (FWHM) of Ge layers were found to be 50, 51, and 47 arcsec for the growth temperatures of 350, 400, and 450 °C, respectively. The X-ray analysis thus suggests that there is a wide range of growth temperature window for the epitaxial Ge layer. However, the higher growth temperature must be avoided to minimize the interdiffusion of Ga, As, and Ge atoms at the heterointerface.

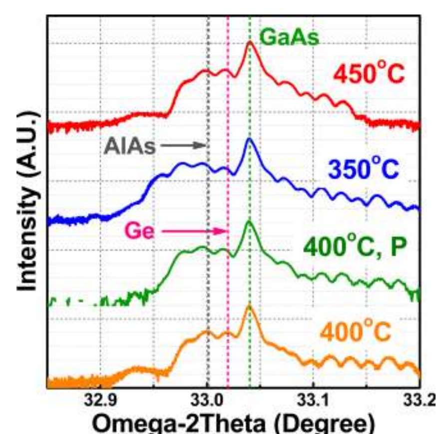

Figure 2. X-ray rocking curves for the 80 nm Ge layer grown on (100)/2° GaAs substrates at 350, 400, and 450 °C, respectively. The Pendellösung oscillations from these samples show the superior epitaxial crystalline quality. The X-ray curves were shifted vertically for clarity. The “P” represents the long growth pause prior to Ge layer growth.

The structure was further investigated by AFM to quantify the surface roughness and other growth- related defects. Figure 3 shows the AFM surface morphology of the epitaxial Ge layer grown at three growth temperatures on GaAs substrates using AlAs buffer layers without any long growth pause prior to the Ge layer growth. The AFM data reveals a root-mean-square (rms) roughness of ∼1.8−2.5 nm over 20 × 20 μm for the Ge, which is about 5 times higher than the Ge layer grown on (100)/6° GaAs substrate using MBE.[15] The anticipated uniform and low surface roughness is an indication of high-quality two-dimensional epitaxy of Ge on AlAs/GaAs. The increase in surface roughness could be due to the growth of the AlAs layer on GaAs. The same growth rate (25 nm/h) and growth temperature (400 °C) exhibited a surface roughness of about 0.38 nm for the Ge grown on (100)/6° GaAs substrate.[15] This is also consistent with reflection high energy electron diffraction (RHEED) observation during growth, which displayed a streakier (2 × 2) surface reconstruction pattern for Ge.[15]

During MBE growth, the active device layer is typically grown after a time pause of variable duration following growth of underlying layers. To understand the effect of a long growth pause prior to the growth of the Ge layer on the structural and electrical transport properties of the Ge layer, we kept the AlAs/GaAs sample under a vacuum of $\sim 10^{-9}$ Torr at 150 °C temperature inside the MBE chamber for about 12 h after the growth of AlAs, prior to the growth of the Ge layer. Figure 4 shows the AFM surface morphology of the epitaxial Ge layers on (100)/2° GaAs substrate grown at 400 °C with the growth pause. The measured surface roughness was ∼2.21 nm, similar to the Ge layer grown at 400 °C without long growth pause (rms roughness of ∼2.25 nm), as shown in Figure 3b. The surface roughness of Ge layers with and without the growth pause after the growth of AlAs layer, are almost identical. The X-ray analysis of this structure is shown in Figure 2. The electrical transport properties of these Ge layers would provide information whether the long growth pause prior to the Ge layer impacts the carrier mobility and ultimately the device properties. The insight will help device and process engineers by providing flexibility for designing Ge-based nanoscale transistor structures where a long growth pause in the process

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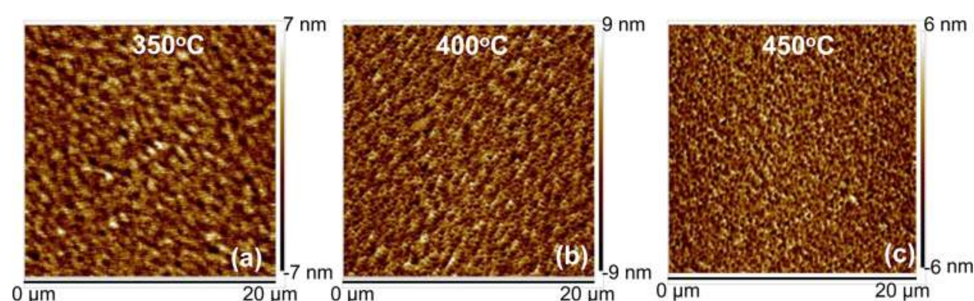

Figure 3. Surface morphology of the epitaxial Ge layers grown at three different growth temperatures on (100)/2° GaAs substrates. The measured surface roughness are in the range of 1.8−2.5 nm.

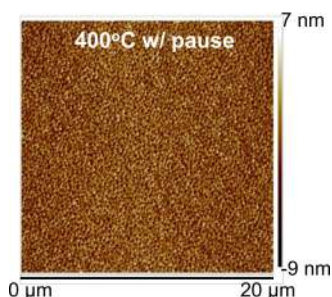

Figure 4. Surface morphology of the epitaxial Ge layer on (100)/2° GaAs substrate grown at 400 °C with 12 h growth pause after the AlAs layer growth. The measured surface roughness was 2.21 nm.

cannot be avoided. Table 1 shows the summary of the results obtained from these samples.

Table 1. Summary of Growth Parameter, Structural Analysis, And Electrical Transport Parameters of Ge Layers Grown on GaAs Substrates Presented in This Study

Ge growth temperature (°C)		Ge FWHM (arcsec)	RMS roughness (nm)	sheet carrier density (cm^{-2})	electron mobility ($cm^2/(V\ s)$)
350	no pause	49.93	1.96	1.34×10^{14}	202.84
400	no pause	50.98	2.55	2.84×10^{13}	280.44
400	pause	49.10	2.21	5.86×10^{13}	252.05
450	no pause	47.23	1.78	2.07×10^{13}	202.75

The structural quality and the defect properties of the 80 nm Ge/170 nm AlAs/GaAs and 240 nm Ge/170 nm AlAs/2.2 μm GaAs/Si structures were examined by cross-sectional TEM. Figure 5 shows a typical cross-sectional bright field TEM micrograph of the Ge/AlAs/GaAs and Ge/AlAs/GaAs/Si structure, respectively, showing the interfaces between Ge and AlAs as well as AlAs and GaAs. The layer structure shown in Figure 5 was grown at 400 °C without long growth pause. The image in Figure 5 shows a high contrast at each heterointerface and the Ge/AlAs/GaAs structure is lattice matched, as expected since the lattice constants of Ge, AlAs, and GaAs are almost identical (the lattice mismatch between Ge and GaAs is 0.07%). The lattice matched nature of the Ge layer revealed by the TEM micrograph is consistent with the results from the X-ray analysis above, demonstrating the significant achievement toward correlated synthesis−structure−property behavior. We also note that the AlAs layer will provide carrier confinement inside the Ge layer via the large band offsets of Ge/AlAs.[8] A sufficiently high barrier for holes and electrons is indeed desired for carrier confinement. Further, the AlAs layer can serve as an etch stop layer when fabricating nanoscale Ge transistors.

Electrical Transport Properties. *Effect of Growth Temperature and Growth Pause on Ge.* To further investigate the quality of Ge layers grown at different temperatures, we measured the carrier mobility of the Ge films using electronic transport measurements in the van der Pauw configuration over a temperature range of 90−315 K. The transport measurements assess the quality and the carrier density in the semiconductor layers, with the mobility as an important figure-of-merit. Additionally, the mobility and the sheet carrier density obtained as a function of temperature are important design parameters for the next-generation nanoscale transistors. It is important that the carrier freeze-out be minimal at lower temperature and that transport in the layers be dominated by a single carrier.

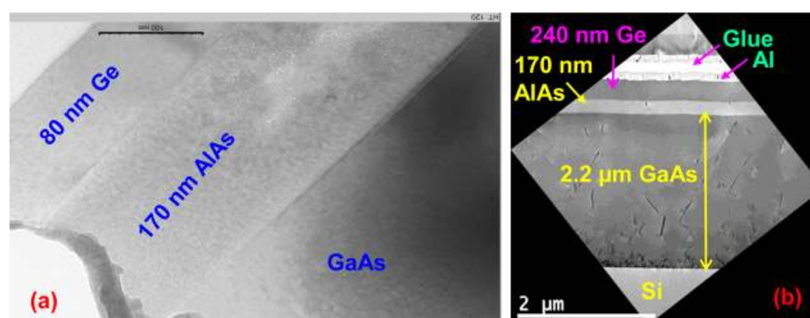

Figure 5. (a) Cross-sectional TEM micrograph of 80 nm Ge grown on GaAs substrate using a 170 nm AlAs buffer layer. The granular spots in some areas of AlAs layer are due to the damage during ion milling process. (b) Cross-sectional TEM micrograph of the Ge/AlAs/GaAs/Si structure. The TEM measurement was performed after depositing the aluminum metal.

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Figure 6 shows the electron mobility and sheet carrier density as a function of temperature in Ge layers grown at different

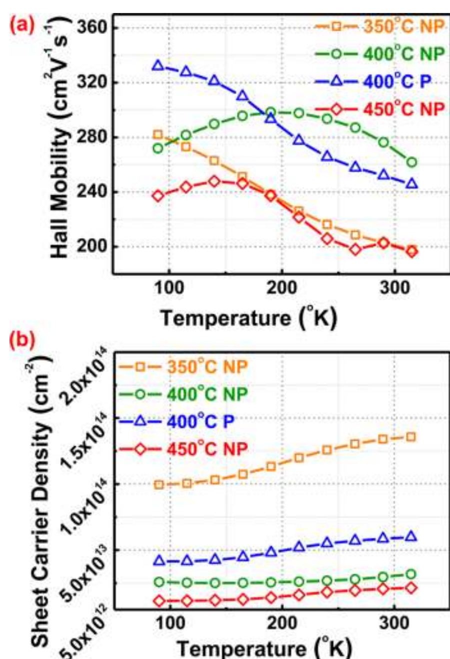

Figure 6. (a) Hall mobility and (b) sheet carrier density as a function of temperature in Ge layers grown at 350, 400, and 450 °C, respectively. Ge layers were grown with without pause (NP) and with a long growth pause (P).

temperatures. The mobility at 290 K was ∼280 $cm^2/(V\ s)$ for the sample grown at 400 °C compared to ∼200 $cm^2/(V\ s)$ for samples grown at 350 and 450 °C without any long growth pause. However, at 290 K the sample grown at 400 °C with long growth pause exhibited a mobility value of about 255 $cm^2/(V\ s)$. The sheet carrier density at 290 K is about 3×10^{13} cm^{-2} for a 400 °C growth temperature without growth pause. The lower mobilities at both 350 and 450 °C growth temperatures measured at 290 K rule out the possibility of growing high-quality Ge epitaxial layers on GaAs at these temperatures. However, these Ge layers exhibited similar X-ray FWHM and surface roughness as the sample grown at 400 °C (between the results from structural analysis and electrical transport properties, the electrical transport properties should be given preference). The complex dependences of mobility on temperature in Figure 6a are due to competing effects of phonon scattering, scattering on Coulombic impurities and dislocations, and interface scattering at the Ge/AlAs heterointerface. It is interesting to compare the two samples grown at 400 °C. Above 180 K, the mobility is higher for the sample grown without growth pause than for the sample grown with growth pause and slowly increases with decreasing temperature. Below 180 K, the mobility in the sample without growth pause decreases with decreasing temperature, whereas the mobility in the sample with growth pause keeps increasing. Of the competing scattering mechanisms, phonon scattering has the most pronounced temperature dependence. Phonon scattering increases with increasing temperature. Phonon-limited scattering will thus lead to a mobility decreasing with increasing temperature. A phonon-limited mobility denotes a good sample quality, since it implies other scattering mechanisms, originating in sample defects, do not dominate. The temperature dependence of the mobility in the sample with growth pause indicates just such phonon-limited behavior, indicative of improved quality. The lower mobility from 180 to 315 K for the sample with growth pause (compared to without), could be due to the effect of the complex balance between phonon scattering, and the other scattering mechanisms, particularly interface scattering at Ge/AlAs heterointerface. The sheet carrier densities do not change substantially over temperatures from 90 to 315 K for all samples. These results suggest an ideal growth temperature of 400 °C for the Ge layer, omitting the long growth pause. The sheet carrier density and the electron mobility of these samples measured at 290 K are also summarized in Table 1.

Effect of Forming Gas Annealing on Ge/AlAs/GaAs. To investigate the effect of forming gas annealing on the mobility and the sheet carrier density of a Ge layer grown at 400 °C without growth pause, we annealed a van der Pauw sample for different durations but at same annealing temperature of 350 °C under forming gas. After each measurement, the sample was annealed in forming gas (95%N_2/5%H_2) for a prescribed time. Figure 7 shows the mobility and sheet carrier density of the Ge

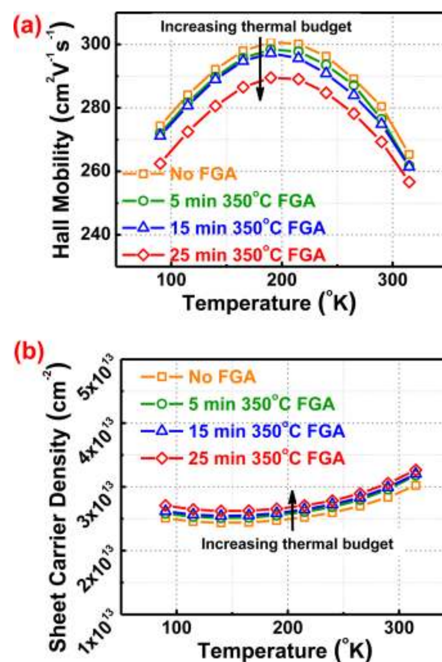

Figure 7. (a) Hall mobility and (b) sheet carrier density as a function of temperatures in Ge layers grown at 400 °C without long growth pause under different forming gas annealing (FGA) time at fixed annealing temperature of 350 °C, respectively.

epilayer for annealing durations of 5, 15, 25 min, and without annealing. The 15 min annealing duration was a cumulative time of a 5 min annealing followed by a 10 min annealing. After 15 min annealing and measurement, the sample was further annealed for another 10 min (25 min total). In each case, the Hall mobility measurement was performed from 90 to 315 K. The shape of the mobility vs temperature graph is almost identical for different annealing durations at this fixed annealing temperature, while the mobility value decreases for longer annealing duration. The decrease is attributed to the effect of interface intermixing, creating defects within the Ge film. The sheet carrier density increases with annealing time, as shown in Figure 7b. Therefore, there exists a need to carefully balance the

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annealing duration and ultimately the total thermal budget for the epitaxial Ge layer, such that device fabrication avoids mobility degradation. It is interesting to note that the repeated thermal annealing and temperature cycle measurements from 90 to 315 K (low-temperature thermal cycle or cryogenic stress) on the same Hall sample have minimal effect on the carrier mobility and density, indicating that the mobility of this structure is not affected by the cryogenic stress.

Effect of Forming Gas Annealing on Epitaxial Ge on Si Using AlAs/GaAs Buffer. Results on mobility measurements on the epitaxial Ge grown on Si using large bandgap AlAs/GaAs buffer layers were provided in earlier work.[8] In order to understand the effect of annealing in forming gas on the mobility and carrier density, a van der Pauw sample was repeatedly annealed in forming gas and measured over the temperature range of 90−315 K, as described above. One purpose of these measurements is to understand the effect of hydrogen on the passivation of the shallow donors and the concomitant effect on carrier density. These experiments also allow us to ascertain the reliability of repeated mobility measurements data after cryogenic stressing on this sample. During the repeated measurements, the sample might generate a crack due to the thermal mismatch of the Ge/III−V layer and the Si substrate by the differences in thermal expansion in the aforementioned structure. Figure 8 shows the mobility and the carrier density as a function of measurement temperature and forming gas annealing conditions. One can find from Figure 8a that the mobility value increased from 370 to 420 $cm^2/(V\ s)$ at 290 K when the sample was annealed for an additional 10 min. This increase in mobility is attributed to the reduction of the point defects by the thermal annealing. However, the further forming gas annealing by an additional 10 min reduces the mobility, similar to Figure 7a. Thus, a crucial total thermal budget exists for the transport properties of Ge layer either grown on GaAs or on Si substrates. The carrier density is almost constant over temperature for different annealing temperatures, suggesting that the carriers are confined to the Ge layer, with the AlAs layer acting as a parallel conduction blocking barrier over this temperature range. Furthermore, comparing the electron mobility of Ge layer grown on Si as well as on GaAs, one can find that the electron mobility is higher on Si substrate than on GaAs substrate. One might expect better crystalline quality of Ge on GaAs than on Si and hence higher electron mobility. However, the mobility may not correlate one-on-one with the crystal quality, and optimization of mobility is the ultimate aim. Depending on the scattering mechanism induced by crystal defects, the mobility may not severely be affected. For instance, small-angle scattering mechanisms, as due to extended Coulombic scattering potentials, will not much affect mobility since small-angle scattering is ineffective at diffusing forward momentum. We presume that the lower crystal quality obtained on Si still affords a higher mobility since the scattering mechanisms induced by the lower crystal quality can be ineffective at reducing mobility, whereas effective scattering mechanisms have been reduced.

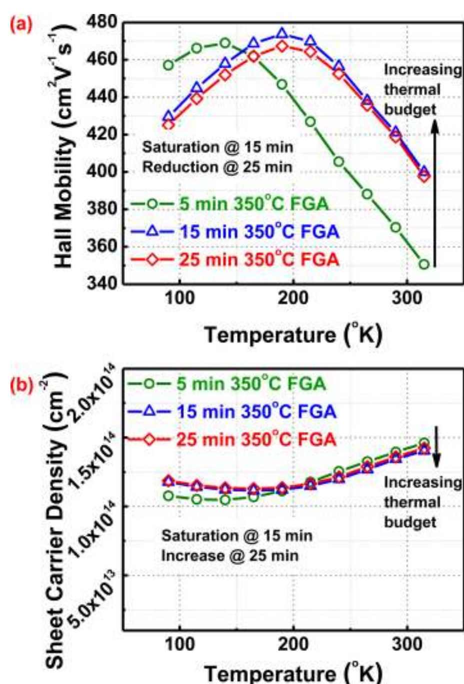

Figure 8. (a) Mobility and (b) sheet carrier density as a function of temperature in the Ge layer grown at 400 °C under different forming gas annealing FGA time, respectively, on Si using a composite AlAs/GaAs buffer layer.

Magnetotransport Measurement of Epitaxial Ge on Si using AlAs/GaAs Buffer. To confirm the single carrier conduction,we performed magnetotransport measurements at 390 mK and over ±9 T magnetic field applied normally to a sample in the van der Pauw geometry. Figure 9a shows the antisymmetric component of the Hall resistance (off-diagonal component R_{xy}) up to ±9 T magnetic field with the different configurations of current and voltage contacts as depicted schematically in the insets for the van der Pauw geometry. The Hall resistance R_{xy} is linear up to high B in both the field directions and shows minimal intermixing with the symmetric component of Hall resistance R_{xx}. The linearity in B indicates single carrier conduction in the Ge layer. According to the linear slope, the Hall mobility measured at this temperature yielded a carrier density of N_B = 1.42 × 10^{14} cm^{-2} and an electron mobility of μ_B = 392 $cm^2/(V\ s)$, respectively, which is in agreement with the measurements depicted in Figure 8a,b. With a different contact configuration as depicted in Figure 9a, also yielding a linear slope, very nearly the same carrier density is obtained. Assuming one dominant carrier for conduction, at 390 mK it is found that the sheet resistance is 112.72 Ω/□, the sheet carrier density 1.42 × 10^{14} cm^{-2}, and the mobility 392 $cm^2/(V\ s)$ for the epitaxial Ge on Si using AlAs/GaAs buffer.

Magnetotransport measurements at low temperatures (below ~1 K, here at 390 mK) reveal quantum corrections to the conductivity in materials with moderate disorder, called weak-localization and antilocalization.[16−19] The quantum correction of weak-localization is observed in the measurements depicted in Figure 9b,c, as discussed below. Weak localization is a manifestation of the near-absence of spin−orbit interaction, in contrast to antilocalization which is a manifestation of the presence of spin−orbit interaction.[18−22] The quantum corrections result from quantum interference of time-reversed closed-loop scattering trajectories. A negative magnetoresistance at low magnetic fields is a hallmark of weak-localization, whereas a positive magnetoresistance is a hallmark of antilocalization.[20] An initial decrease in resistance with increasing magnetic field (negative magnetoresistance, weak-localization at low fields) is indeed observed in Figure 9b,c. The existence of weak-localization, and not antilocalization, points

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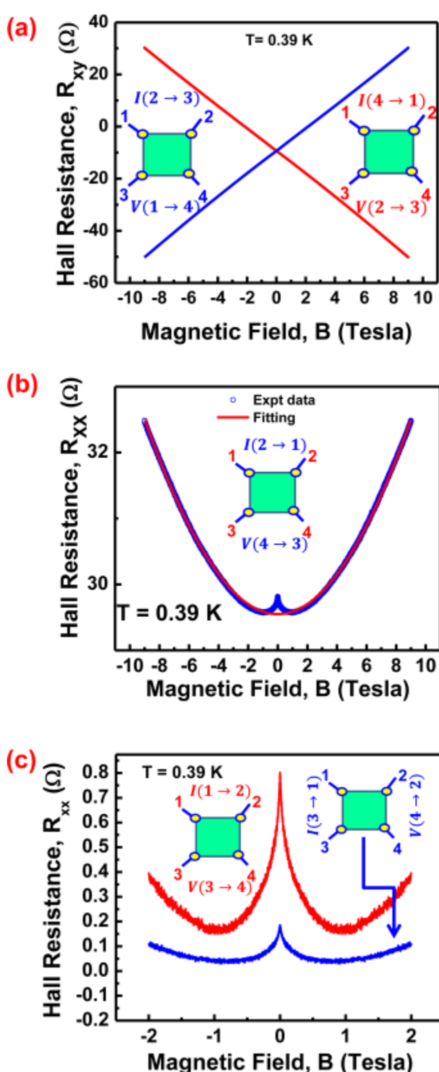

Figure 9. (a) Antisymmetric component of the Hall resistance, R_{XY} as a function of magnetic field over ±9T, with the very linear dependence on magnetic field demonstrating single carrier behavior. (b) Symmetric component of the Hall resistance, R_{XX} as a function of magnetic field over ±9T. (c) High-resolution traces, with different resistance offsets subtracted, emphasizing the weak-localization behavior at low magnetic fields.

to the fact that the carriers responsible for transport experience a near absence of spin−orbit interaction. As explained below, in the Ge/AlAs heterostructure this observation indicates that the carriers responsible for transport are electrons confined to the Ge layer, and excludes transport contributions due to carriers in the AlAs layer. Figure 9b,c show the symmetric component of the Hall resistance (diagonal component R_{xx}) up to ±9 T magnetic field with the different configurations of current and voltage contacts as depicted schematically in the insets for the van der Pauw geometry. Figure 9b shows the weak-localization negative magnetoresistance at low field (below ∼1T). Figure 9c shows high-resolution traces at low fields (resistance offsets were subtracted during the measurement to obtain higher measurement resolutions). Figure 9c clearly shows the existence of the negative magnetoresistance characteristic of weak-localization. As mentioned above, the carriers responsible for transport thus must experience negligible spin−orbit interaction. Spin−orbit interaction occurs due to a broken spatial inversion symmetry,[23] either in the bulk crystal (Dresselhaus effect[24,25]) or due to heterostructural asymmetry (Rashba effect[26,27]). The AlAs, as a III−V compound semiconductor, has a lack of inversion symmetry in the bulk crystal and thus carriers in AlAs necessarily experience spin−orbit interaction, while in contrast, specifically electrons in Ge experience only negligible spin−orbit interaction.[23−25] Thus, the transport in the Ge/AlAs heterostructure must occur by electrons only in the Ge layer. This confirms the single carrier conduction and pinpoints the Ge layer as the electronically active layer. The single carrier conduction and the detailed magnetotransport properties of the epitaxial Ge demonstrated above illustrate the strong potential for low-power transistors as well as optoelectronic devices.

CONCLUSIONS

The growth, structural, and magnetotransport properties of epitaxial Ge/AlAs heterostructures with different growth conditions and substrate architectures have been studied under ±9 T magnetic field and at 390 mK temperature. Systematic mobility measurements of Ge epilayer on GaAs substrates with growth temperatures from 350 to 450 °C demonstrated the highest electron mobility at 400 °C without long growth pause prior to Ge deposition, which is corroborated by structural and morphological studies. Our results on Si substrate using a composite AlAs/GaAs buffer architecture at 400 °C Ge growth temperature demonstrates that the Ge/AlAs shows single carrier transport with the charge solely confined to the Ge layer. The prominent negative magnetoresistance at 390 mK temperature is indicative of the weak-localization effect in this Ge/AlAs heterostructure and points to the near absence spin−orbit interaction, a first demonstration in this heterostructure indicating that carriers responsible for transport must be electrons confined to the Ge layer. Hence, epitaxial Ge grown on Si using an AlAs/GaAs buffer architecture shows a great promise for next-generation low-power and high-performance field effect transistor applications.

MATERIALS AND METHODS

Material Synthesis. The undoped epitaxial 80 nm-240 nm thick Ge layers were grown using an in situ growth process on epi-ready semi-insulating (100)/2° GaAs and (100)/6° offcut Si substrates using separate solid source molecular beam epitaxy growth chambers for the Ge and III−V materials, connected via an ultrahigh vacuum transfer chamber. The growth temperature and growth rate of epitaxial Ge were in the range of 350−450 °C and 0.1 Å/s, respectively. The details of the growth procedure are reported elsewhere.[8,15]

Materials Characterization. To determine the structural quality and the relaxation state of epitaxial Ge layers, we recorded high-resolution triple axis X-ray rocking curves. Cross-sectional high-resolution transmission electron microscopy (HR-TEM) was used to characterize the interface between the Ge and AlAs as well as AlAs and GaAs substrate. The HR-TEM imaging was performed on a JEOL 2100 transmission electron microscope. For this purpose, the electron transparent foil of thin film cross-section of Ge/AlAs/GaAs was prepared by a standard polishing technique, that is, mechanical grinding, dimpling, and Ar^+ ion beam milling.

Carrier Transport Measurement. Au/Ti (600 Å/200 Å) ohmic contacts required for the Hall mobility measurements were made on Ge/AlAs/GaAs and Ge/AlAs/GaAs/Si in a Kurt J. Lesker PVD 250 physical vapor deposition system. The four corner contacts were defined using positive photoresist and prebaked at ∼85 °C prior to the deposition of Au and Ti metals. The deposited contacts were annealed at 350 °C for 5, 15, and 25 min under a mixture of N_2/H_2 (95:5 v/v).

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The carrier density and Hall mobility were measured as a function of temperature from 90 to 315 K with a fixed magnetic field of 0.55T using an Ecopia HMS5000 Hall measurement system. The magneto-transport measurements at 390 mK, and high magnetic fields were performed in a ^{3}He cryostat, with the sample submerged in liquid ^{3}He. The ^{3}He system is equipped with a superconducting magnet allowing the magnetic field to be varied over 9 T in both polarities normal to the sample surface. The weak localization data was obtained in the same system using a magnet power supply capable of slow sweeps with subgauss resolution.

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Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Krishnamohan, T.; Krivokapic, Z.; Uchida, K.; Nishi, Y.; Saraswat, K. C. High-Mobility Ultrathin Strained Ge MOSFETs on Bulk and SOI With Low Band-to-Band Tunneling Leakage: Experiments. *IEEE Trans. Electron Devices* **2006**, *53*, 990−999.

(2) Krishnamohan, T.; Kim, D.; Nguyen, C. D.; Jungemann, C.; Nishi, Y.; Saraswat, K. C. High-Mobility Low Band-to-Band Tunneling Strained-Germanium Double-gate Heterostructure FETs: Simulations. *IEEE Trans. Electron Devices* **2006**, *53*, 1000−1009.

(3) Ho, B.; Nuo, X.; Tsu-Jae King, L. pMOSFET Performance Enhancement With Strained $Si_{1-x}Ge_x$ Channels. *IEEE Trans. Electron Devices* **2012**, *59*, 1468−1474.

(4) Chleirigh, C. N.; Theodore, N. D.; Fukuyama, H.; Mure, S.; Ehrke, H.-U.; Domenicucci, A.; Hoyt, J. L. Thickness Dependence of Hole Mobility in Ultrathin SiGe-channel p-MOSFETs. *IEEE Trans. Electron Devices* **2008**, *55*, 2687−2694.

(5) Hutin, L.; Le Royer, C.; Damlencourt, J.-F.; Hartmann, J.-M.; Grampeix, H.; Mazzocchi, V.; Tabone, C.; Previtali, B.; Pouydebasque, A.; Vinet, M. GeOI pMOSFETs Scaled Down to 30-nm Gate Length With Record Off-state Current. *IEEE Electron Device Lett.* **2010**, *31*, 234−236.

(6) Pillarisetty, R.; Chu-Kung, B.; Corcoran, S.; Dewey, G.; Kavalieros, J.; Kennel, H.; Kotlyar, R.; Le, V.; Lionberger, D.; Metz, M.; et al. High Mobility Strained Germanium Quantum Well Field Effect Transistor as the p-Channel Device Option for Low Power (V_{cc} = 0.5V) III-V CMOS Architecture. *Technical Digest International Electron Devices Meeting-IEDM* **2010**, 6.7.1−6.7. 4.

(7) Zhang, R.; Yu, X.; Takenaka, M.; Takagi, S. Impact of Channel Orientation on Electrical Properties of Ge p- and n-MOSFETs With 1-nm EOT $Al_2O_3/GeO_x/Ge$ Gate-Stacks Fabricated by Plasma Post oxidation. *IEEE Trans. Electron Devices* **2014**, *61*, 3668−3675.

(8) Hudait, M. K.; Clavel, M.; Goley, P.; Jain, N.; Zhu, Y. Heterogeneous Integration of Epitaxial Ge on Si using AlAs/GaAs Buffer Architecture: Suitability for Low-power Fin Field-Effect Transistors. *Sci. Rep.* **2014**, *4*, 6964−6969.

(9) Nguyen, P. D.; Clavel, M.; Goley, P.; Liu, J.-S.; Allen, N.; Guido, L. J.; Hudait, M. K. Heteroepitaxial Ge MOS Devices on Si Using Composite AlAs/GaAs Buffer. *IEEE J. Electron Devices Soc.* **2015**, *3*, 341−348.

(10) Hudait, M. K. Heterogeneously Integrated III-V on Silicon for Future Nanoelectronics,. *ECS Trans.* **2012**, *45*, 581−594.

(11) Hudait, M. K.; Dewey, G.; Datta, S.; Fastenau, J. M.; Kavalieros, J.; Liu, W. K.; Lubyshev, D.; Pillarisetty, R.; Rachmady, W.; Radosavljevic, M.; Rakshit, T.; Chau, R. Heterogeneous Integration of Enhancement Mode $In_{0.7}Ga_{0.3}As$ Quantum Well Transistor on Silicon Substrate Using Thin (2μm) Composite Buffer Architecture for High-speed and Low-voltage (0.5V) Logic Applications. *IEEE International Electron Devices Meeting (IEDM) Technical Digest* **2007**, 625−628.

(12) Lubyshev, D.; Fastenau, J. M.; Wu, Y.; Liu, W. K.; Bulsara, M. T.; Fitzgerald, E. A.; Hoke, W. E. Molecular Beam Epitaxy Growth of Metamorphic High Electron Mobility Transistors and Metamorphic Heterojunction Bipolar Transistors on Ge and Ge-on-Insulator/Si Substrates. *J. Vac. Sci. Technol. B* **2008**, *26*, 1115−1119.

(13) Hudait, M. K.; Lin, Y.; Sinha, P. M.; Lindemuth, J. R.; Ringel, S. A. Carrier Compensation and Scattering Mechanisms in Si-doped $InAs_yP_{1-y}$ Layers Grown on InP Substrates Using Intermediate $InAs_yP_{1-y}$ step-Graded buffers. *J. Appl. Phys.* **2006**, *100*, 063705−1−9.

(14) Lindemuth, J. R. Parallel Conduction in Semiconductors. *III-Vs Review* **2006**, *19*, 28−32.

(15) Hudait, M. K.; Zhu, Y.; Jain, N.; Hunter, J. L., Jr. Structural, Morphological, and Band Alignment Properties of GaAs/Ge/GaAs Heterostructures on (100), (110) and (111)A GaAs Substrates. *J. Vac. Sci. Technol. B* **2013**, *31*, 011206−1−14.

(16) Bergmann, G. Weak Localization and its Applications as an Experimental Tool. *Int. J. Mod. Phys. B* **2010**, *24*, 2015−2052.

(17) Bergmann, G. Weak Localization in Thin Films, a Time-of-flight Experiment With Conduction Electrons. *Phys. Rep.* **1984**, *107*, 1−58.

(18) Kallaher, R. L.; Heremans, J. J. Spin and Phase Coherence Measured by Antilocalization in n-InSb Thin Films. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2009**, *79*, 075322.

(19) Kallaher, R. L.; Heremans, J. J.; Goel, N.; Chung, S. J.; Santos, M. B. Spin-orbit Interaction Determined by Antilocalization in an InSb Quantum Well. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2010**, *81*, 075303.

(20) Bergmann, G. Weak Anti-localization - An Experimental Proof for the Destructive Interference of Rotated Spin 1/2. *Solid State Commun.* **1982**, *42*, 815−817.

(21) Iordanskii, S. V.; Lyanda-Geller, Y. B.; Pikus, G. E. Weak Localization in Quantum Wells With Spin-orbit Interaction. *JETP Lett.* **1994**, *60*, 206−211.

(22) McPhail, S.; Yasin, C. E.; Hamilton, A. R.; Simmons, M. Y.; Linfield, E. H.; Pepper, M.; Ritchie, D. A. Weak Localization in High-quality Two-dimensional Systems. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2004**, *70*, 245311.

(23) Winkler, R. Spin-orbit Coupling Effects in Two-dimensional Electron and Hole Systems. *Springer Tracts in Modern Physics*; Springer-Verlag: Berlin, Heidelberg, 2003.

(24) Dresselhaus, G. F. Spin-orbit Coupling Effects in Zinc Blende Structures. *Phys. Rev.* **1955**, *100*, 580−586.

(25) Faniel, S.; Matsuura, T.; Mineshige, S.; Sekine, Y.; Koga, T. Determination of Spin-Orbit Coefficients in Semiconductor Quantum Wells. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2011**, *83*, 115309.

(26) Bychkov, Y. A.; Rashba, E. I. Oscillatory Effects and the Magnetic Susceptibility of Carriers in Inversion Layers. *J. Phys. C: Solid State Phys.* **1984**, *17*, 6039−6045.

(27) Pfeffer, P.; Zawadzki, W. Spin Splitting of Conduction Subbands in III-V Heterostructures Due to Inversion Asymmetry. *Phys. Rev. B: Condens. Matter Mater. Phys.* **1999**, *59*, R5312−R5315.

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