Managing Signal and Power Integrity Using Power Transmission Lines and Alternative Signaling Schemes

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***Abstract*— Signal and power integrity are crucial for ensuring good performance in high speed digital systems. As the operating frequency of digital systems increases, the power and ground bounce created by simultaneous switching noise (SSN) becomes a limiting factor for the performance of these devices. SSN is caused by parasitic inductance that exists in the power delivery network (PDN), and voltage fluctuations on the power and ground rails can lead to reduced noise margins and can limit the maximum frequency of a digital device. A new PDN design has been suggested that achieves significantly reduced SSN [1] by replacing the power plane structure with a power transmission line (PTL). Previous works have demonstrated the validity of the Power Transmission Line concept in terms of SSN reduction and power consumption reduction [1-4]. However, these works focused on small systems with just a few bits. This paper shows the effectiveness of the PTL concept on a large scale system with a large number of I/O pins through an FPGA implementation to simulate the memory interface such as DDR3.**

I. INTRODUCTION

The rapid increase in data rates and transistor density in digital integrated circuits (ICs) introduces significant challenges for signal and power integrity. A critical problem in these areas is switching noise due to the high current transients of digital devices. Most power delivery networks (PDNs) in digital systems utilize power and ground planes, as this provides a low-impedance path between the system power supply and the power pin of an IC. As signal currents flow from the transmitters to the receivers, corresponding return currents are created traveling in the opposite direction on the reference plane. In order to form a closed circuit loop, the return current always follows the path of least impedance on the reference plane closest to the signal transmission line. However, the return current can be disrupted by via transitions, apertures on power/ground layers, or split planes [6]. Disruptions in the current return loop induce parasitic inductance on the PDN, and coupled with large current transients, this can lead to simultaneous switching noise that adversely affects the signal quality [7]. A common solution to this problem is to add large decoupling capacitors between the power and ground planes to suppress voltage fluctuations across the parasitic inductance, as well as to ensure current continuity. In addition, differential signaling can also be used to reduce the amount of power and ground bounce. However this requires double the amount of input pins which can pose a serious limitation for some systems. In addition, differential signaling itself does not address the issue of return path discontinuities.

To combat the SSN problem, a new I/O signaling scheme is proposed and tested. This solution is based on the power transmission line (PTL) concept [6], in which a transmission line is used in place of a power plane to transfer power from the VRM to an IC on the PCB. The PTL-based PDN allows both power and signal transmission lines to be referenced to the same ground plane so that a continuous current loop is established, and therefore removes return path discontinuity (RPD) effects and cavity resonances [6].

While using PTLs helps solve the RPD issue, it presents additional difficulties. One such issue that arises with the PTL-based signaling scheme is the dynamic DC drop due to the terminating resistance between the voltage supply and the PTL [6]. The state of the output data dictates how much current the I/O drivers draw from the PDN. In the case of a voltage-mode driver, the high state of the output data induces current to flow from the PDN toward the signal transmission line, while the low state of the output data draws much less current. Thus, the DC drop that occurs on the PDN is data-dependent and can degrade the performance of the driver. Consequently, a concept known as pseudo-balanced encoding is applied to address this issue, and is described in the next section.

The amount of noise on the PDN is proportional to the current on the power rails and the PDN impedance, as well as the number of I/O drivers that are switching. As opposed to the commonly used power and ground planes in conventional PDNs, a power transmission lines based PDN has a relatively high impedance due to the series resistor and transmission line, and therefore the current capacity and scalability of the number of I/Os are important for determining the feasibility of implementing a PTL based PDN in real applications. In this paper, we show the design steps to build a new test vehicle which is capable of supporting multiple switching buffers. For the test vehicle, an FPGA (Field Programmable Gate Array) is a good alternative to multiple driver chips or a custom Application Specific Integrated Circuit (ASIC) product. The concept of the test vehicle is described in following sections.

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II. PSEUDO-BALANCED POWER TRANSMISSION LINE

Constant current flowing through the PTL can address the issue of a fluctuating voltage drop across the PDN. The constant current removes the dynamic characteristics of the dc drop by inducing a fixed amount of voltage drop across the PTL-based PDN, and keeps the PTL fully charged at all times. In order to induce a constant current flowing through the PTL, a signaling scheme known as pseudo-balanced PTL (PB-PTL) is used.

PB-PTL is similar to differential signaling in that it induces a constant current to flow in the PDN. However, in contrast to differential signaling, the input data is encoded prior to transmission. In this scheme, the input data, which is N bits long, is mapped to M bits by satisfying the following equation [4]:

$$\binom{M}{\frac{M}{2}} + \binom{M}{\frac{M}{2}-1} \geq 2^N, \text{ if M is even} \quad (1)$$

$$\binom{M}{\frac{M-1}{2}} + \binom{M}{\frac{M-1}{2}-1} \geq 2^N, \text{ if M is odd} \quad (2)$$

For example, if the original data word consists of 4 bits, $N = 4$, then by (2), $M = 5$, and the encoded word is 5 bits long. With M = 5, the number of 1s and 0s fluctuates between 2 and 3, so an extra output is added to keep the current flowing through the PDN constant. This extra bit is not transmitted, but instead simply used to keep the current constant. More information regarding this encoding concept can be found in [4].

III. PREVIOUS PTL RESULTS

Previous works have shown the efficacy of using a power transmission line as a viable PDN topology on small scale systems. In [5] it was shown that by utilizing a PTL, the transition jitter, which can degrade timing margins, can be reduced by up to a 20% in a prototype PCB board. In addition, the amount of voltage fluctuation on the V_{DD} was measured to be 28% less on the board utilizing the PTL PDN compared to the standard planar structure [5]. One can see that the use of the power transmission line with the switching resistance network significantly improves the shape of the waveform, as it reduces return path discontinuities and results in less power and ground bounce, as seen in the waveforms in Figure 1.

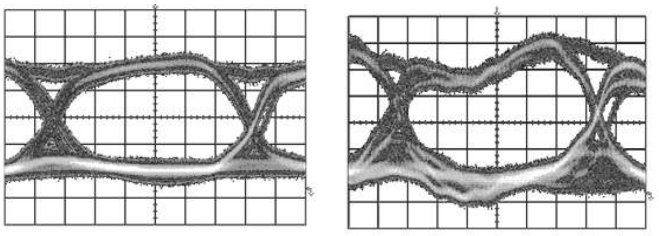

Figure 1. Measured output eye diagram from PTL circuit (left) conventional power/ground plane circuit (right) [4]

IV. FPGA-BASED TEST VEHICLE

High speed interfaces use multiple voltages rails. For example, DDR3 (Double Data Rate Generation 3) memory modules use core voltage (VDD), I/O voltage (VDDQ), termination voltage (VTT), and reference voltages (VREFs) [8]. Thus, the PTL concept can be used to substitute one or more power rails. In addition, the PDN noise associated with switching I/Os is critical because it can degrade system performance. To validate scalability of PTL, we considered compatibility to real applications, such as high speed memory modules.

A test vehicle with an integrated memory module would need over 200 components, thus the complexity of bill of materials (BOM) is not appropriate to verify the concept. Also, those components need surface mount assembly equipment. In contrast, FPGA products provide system integration capabilities, low power support, and multiple I/O standards. Commercially available FPGAs operate at wide voltage range and data rates, and support multiple I/O interface standards [9]. Furthermore, FPGA chips are capable of easily programmable integrated logic blocks for additional functions, such as embedded coding schemes. The additional functions also reduce bill of materials (BOM) of test vehicle because less number of passive devices are used for additional circuitry. Therefore, it was decided to use an FPGA device to verify the PTL concept. It is simpler to work with and will help us to reach the same conclusions. Table I shows compatibility of the test vehicle comparing with a real memory module application.

TABLE I. COMPATIBILITY BETWEEN TEST VEHICLE (FPGA) AND APPLICATION (DDR3 MEMORY)

	Test Vehicle	***Application***
Driver	1 FPGA	8 DRAMs
Voltage	1.2 - 3.3 V	1.35 - 1.5V
I/O	CMOS	SSTL-1.5
Max Freq.	800 MHz	800 MHz
Bus Width	30 bit	64 bit
Termination	Open, PD, PU, & CTT	CTT (ODT)
Channel Length	2" - 3"	5" - 7"
PCB	4-5 layers, 3" x 3"	6-8 layers, 1.2" x 6.25"

V. DESIGN DETAILS OF FPGA TEST VEHICLE

A. Design Parameters/Specs

The voltage supplies for Xilinx Spartan-6 LX45 FG(G) 484 are *VCCINT*, *VCCAUX*, *VCCO_#* and *VREF*. The function and required voltage of each voltage supply are shown in [9]. Moreover, an additional 3.3V supply voltage is used to drive IC chips for the user interface. The PTL supplies power to VCCO_# voltage supplies which control the I/O buffers.

The Xilinx chip used in the research has 338 I/O driver pins in 4 I/O banks. Bank 3, where we implemented PTL, has 88 I/O drivers. These I/O driver pins consist of differential pair. It was decide to use 30 output I/O drivers with using 4-to-6 pseudo-balanced coding scheme in order to achieve PBPTL. In addition to the PTL board, another prototype board was created utilizing standard power and ground planes.

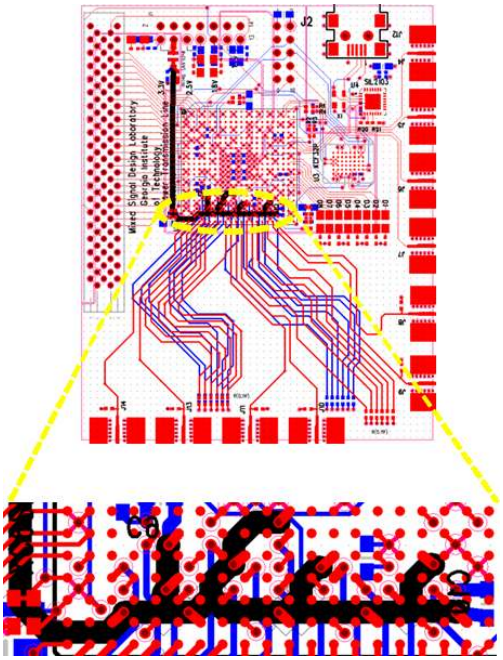

Figure 2. The layout design of the test vehicle based on the power transmission line.

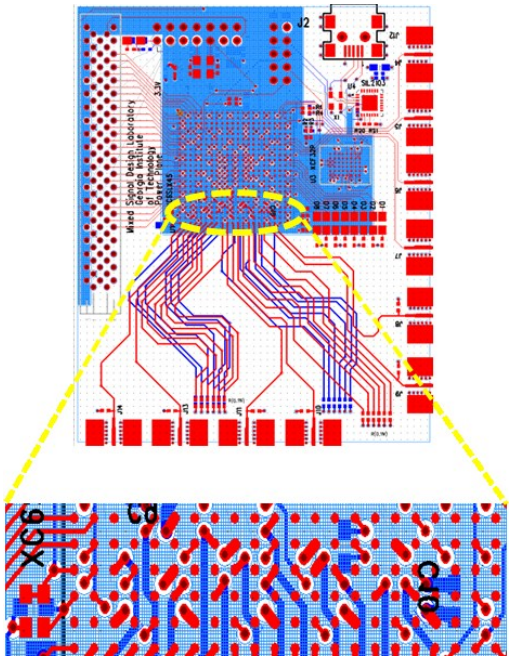

Figure 3. The layout design of the test vehicle based on the power and ground plane.

B. Test Vehicle Layout

Figure 2 shows a layout design of the test vehicle based on the PTL and Figure 3 is the layout of the test vehicle based on power plane. The board consists of an 80-pin connector as an input so that the entire system can be controlled by an Automatic Test Equipment if needed, a JTAG interface, a USB interface, flash memory, voltage regulator, LEDs for debugging, series resistors for PTL termination and a Xilinx Spartan-6 FPGA. The characteristic impedance of microstrip outputs is 50Ω. The PTL's characteristic impedance was chosen to be 10 Ω.

Figure 4 and Figure 5 show the layer stack-up of both prototype boards. The copper layers are 1 oz. layers. Power ground plane based test vehicle uses conventional 4 layers and PTL is inserted in inner1 layer in Figure 4.

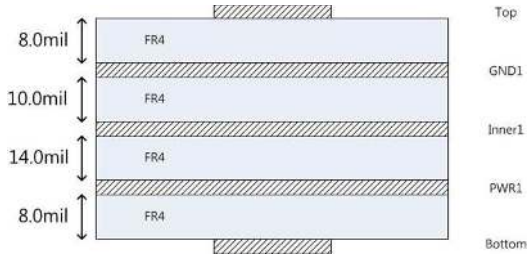

Figure 4. Stack-up layer of test vehicle based on power transmission line

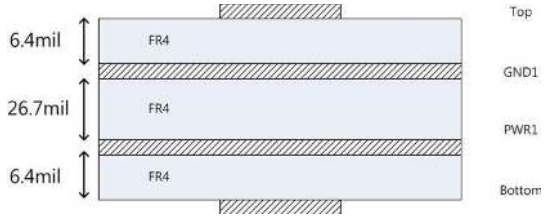

Figure 5. Stack-up layer of test vehicle based on power/ground plane

VI. Simulation Results

In order to demonstrate the effectiveness of this PDN topology on the FPGA implementation, the I/O buffers were simulated in Agilent Advanced Design Systems utilizing both the PB-PTL case and the conventional power plane case, with details on each shown in the following sections.

A. Power Transmission Line Simulation

The schematic of the PTL based on the layout design is shown in Figure 6 and was simulated using a commercial 2.5D EM simulator**.** In the system level simulation, the power transmission line powers 30 I/O buffers found in the FPGA. The I/O buffers are powered by 11 V_{CC} pins in the FPGA's ball gate array that power the I/O buffers. The buffers are 2.5V SSTL buffers.

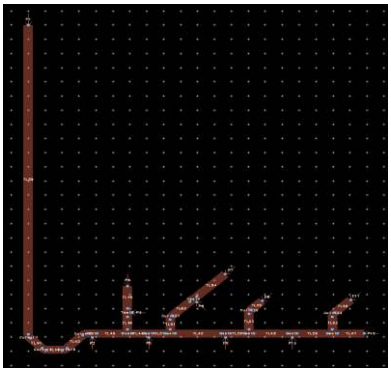

Figure 6. PTL layout as simulated in ADS

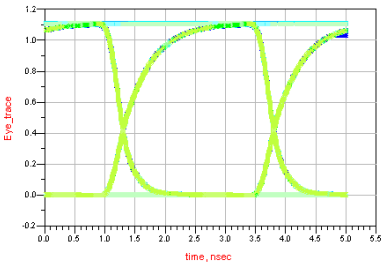

Figure 7. Simulated eye diagram for PTL case

The resulting eye diagram is shown in Figure 7. The eye height is determined to be 1.0258V. In addition, the eye width is 2.51ns and the peak-to-peak jitter is 155.2ps.

B. Conventional PDN Simulation

For the conventional PDN scheme involving a power plane, the layout of the board, as simulated in a commercial 2.5D EM simulator is shown below.

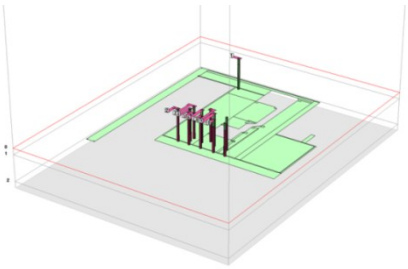

Figure 8. Simulated power and ground plane for FPGA prototype board

In the simulation, ports were placed in 12 locations, 1 port at the power supply voltage location, and the other 11 ports at the V_{CC} pins located on the FPGA ball grid array that power the I/O buffers. The resulting S-parameters were then simulated with the Spartan-6 IBIS models provided by Xilinx. In addition, a 10nF decoupling capacitor was placed at the power supply voltage port (port 1).

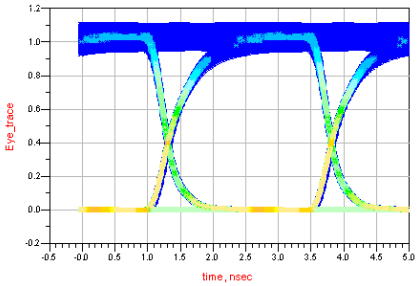

Figure 9. Simulated eye diagram for conventional power plane case

The resulting eye diagram is shown in Figure 9. The eye height is determined to be 0.926V, which is an 11% decrease from the eye height from the PTL circuit. In addition, the eye width is 2.4722ns and the peak-to-peak jitter is 221.73ps. The peak-to-peak jitter is a 52% increase from the jitter exhibited by the PTL circuit. This can present significant performance issues with respect to timing margins and signal skew at the reciever side.

VII. CONCLUSION

This paper discusses the possibility of utilizing the power transmission line concept on a system with a large number of I/O buffers to mimic the functionality of a memory module. This signaling scheme provides power through a transmission line in place of a power plane. Consequently, this reduces the effects of return path discontinuities and can improve the quality of output signal by reducing power and ground bounce. Two test boards were designed, one with conventional power and ground planes, and the other with the PTL-based power delivery network. The test boards measured with a PRBS input signal that is encoded using a bus inversion encoding scheme. Both power distribution schemes were simulated in EM simulation software and integrated with buffer models to compare the signal quality of the output waveform in both cases. The simulations show that significant reduction in simultaneous switching noise can be achieved by using the power transmission line concept in terms of voltage fluctuation on the voltage rails as well as transition jitter.

ACKNOWLEDGMENT

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