Manufacturing Metrology for c-Si Module Reliability and Durability

Part III: Module Manufacturing

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Abstract

This article is the third and final article in a series dedicated to reviewing each process step in crystalline silicon (c-Si) photovoltaic (PV) module manufacturing process: feedstock, crystallization and wafering, cell fabrication, and module manufacturing. The goal of these papers is to identify relevant metrology techniques that can be utilized to improve the quality and durability of the final product. The focus of this article is on the module manufacturing process. The c-Si PV module fabrication process can be divided into three primary areas; (1) stringing and tabbing, (2) lamination, and (3) integration of junction box and bypass diode(s). Each of these processing steps can impact the reliability and durability of PV modules in the field. The ultimate goal of this article is to identify appropriate metrology techniques and characterization methods that can be utilized within a module manufacturing facility to improve the reliability and durability of the final product. Additionally, a gap analysis is carried out to identify areas in need of further research and a discussion is provided that addresses new challenges for advanced materials and emerging technologies.

Keywords

Silicon solar cell; Photovoltaic module; Reliability; Durability; Stringing and tabbing; Interconnects; Lamination; EVA; Encapsulation; Bypass diode; Junction box

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2.   Introduction

With an increased attention to the environment and the limited supply of fossil fuels, production of electricity through harnessing of renewable energy sources is critical to meeting future energy demands. Although energy needs will likely be met through a variety of renewable sources, electricity produced through solar photovoltaics (PV) will be a significant contributor. In order to make this technology cost-effective, PV module output must maintain high performance for long periods of time (i.e. over 25 years). By increasing the lifetime of the PV module, the levelized cost of electricity (LCOE) will decrease [1].

It has been well documented that the energy production of a PV module will decrease over time as a result of one or more degradation modes [2-5]. These degradation modes depend both on the module construction and use environment. The often complex interactions that result in performance loss take years to manifest so it is critical for manufacturers to understand and address reliability issue as early as possible in the product lifecycle. Once a product design is qualified as reliable, quality control during the manufacturing process is essential to ensure that each module will perform as expected.

This article is the third and final article in a series dedicated to reviewing the impact of each processing step on PV module performance and reliability and identifying relevant metrology techniques that can be utilized to improve the quality and durability of the final product. The previous articles in this series had a focus in the areas of silicon feedstock, crystallization and wafering (Part 1) and cell manufacturing (Part 2). The focus of this article is the module manufacturing process (see **Error! Reference source not found.**). The goals of this work are to:

1.   Identify known failure modes and degradation mechanisms induced during module manufacturing

2.   Provide a review of the current state of metrology used during module manufacturing for improved PV reliability and durability

3.   Perform a gap analysis and identify where improvements can be made
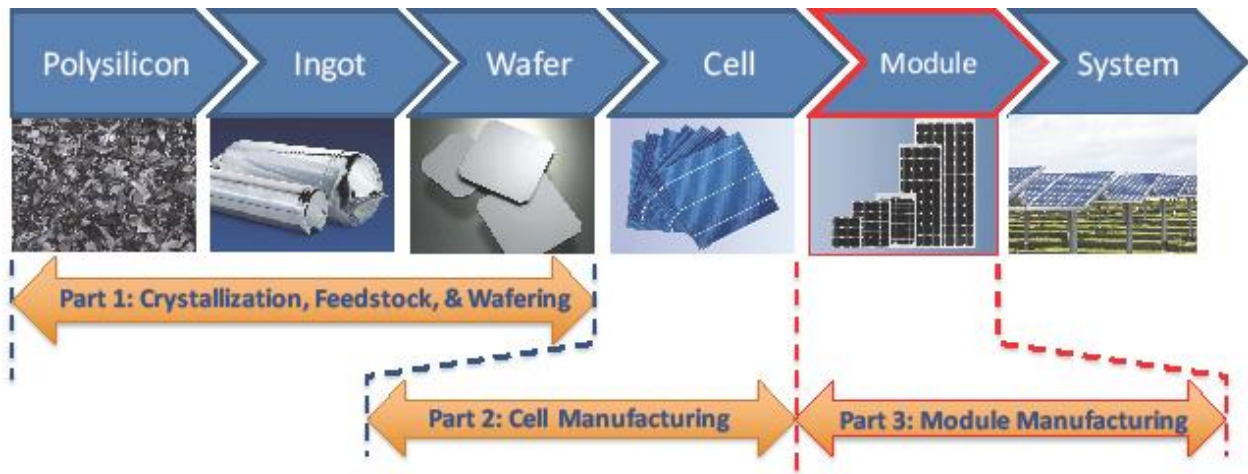
Figure 1. Depiction of c-Si PV manufacturing production areas across the supply chain highlighting module manufacturing as the focus of this article.

Within this article, fundamental properties of materials and components used during module manufacturing will be discussed with regards to their influence on module performance and reliability. The failure modes associated with each material, component, or processing step will be discussed with a focus on identifying the underlying physical and chemical degradation mechanisms. The ultimate goal of this article is to identify appropriate metrology techniques and characterization methods that can be utilized within a module manufacturing facility to improve the reliability and durability of the final product. Additionally, a gap analysis is carried out to identify areas in need of further research and a discussion is provided that addresses new challenges for advanced materials and emerging technologies.

Photovoltaic (PV) module manufacturing is the process of converting completed solar cells into a single, functional unit that is ready for field deployment. For PV modules based on standard crystalline silicon (c-Si) solar cells this process can be divided into three primary categories: (1) stringing and tabbing, (2) lamination, and (3) integration of the junction box and bypass diode(s). This module fabrication process has been in use for over three decades and is effective in producing standardized solar panels with sufficient power and durability for use in a variety of applications.

Because the power produced from a single solar cell is relatively small, several cells must be electrically connected together to form a practical PV module. Typical configurations for screen-printed, Aluminum back surface field (Al-BSF) cells involve the serial connection of cells, with the front contact of one cell connected to the back contact of the adjacent cell. This interconnection process is known as stringing and tabbing. Once the cells are electrically configured, they are encapsulated within a protective package to ensure reliable operation in the outdoor environment. This packaging scheme includes a frontsheet, backsheet, and encapsulant secured together during a lamination step. Finally, a junction box is secured to the backside of the module. The junction box is typically where string interconnections are made, module connector leads are attached, and bypass diodes are incorporated.

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3. Stringing and Tabbing

3.1 Background

Single silicon solar cells typically produce around 0.6 V in direct sunlight. In order to achieve sufficiently high voltages required by system electronics (i.e. inverters), individual cells with similar current characteristics are connected in series through the "stringing and tabbing" process. In this step, tin plated copper ribbon (or tabs) are soldered to the cell busbars on the front side, with sufficient length extending beyond the edge of the cell to provide contact to the rear of the adjacent cell. A string is formed when several cells are placed in series and the excess ribbon from one cell is soldered to the metallic back contact of the adjacent cell. Conventional interconnects are soldered onto the cell busbars, extending much of the length along the busbar to improve the conductivity [6] and provide a fault tolerant connection in the event of cell fracture or solder joint failure. There are typically several strings of cells in a single module. Strings can be connected in series to further increase the voltage or in parallel to increase the current and may be formed internally (i.e. within the laminate) or externally within the junction box.

Two approaches to stringing and tabbing have been conducted: discrete and simultaneous. In the discrete method, the tabs are formed on the front surface, followed by stringing to the back surface. Simultaneous tabbing and stringing, where soldering to the front and back occur concurrently, has also been accomplished, resulting in a single thermal cycle, which could reduce the bow experienced by the wafer due to a balancing effect of the front and back surfaces. In 2006, Gabor *et al.* stated that the trend was towards combined tabbing and stringing, and reported that using a combined tabber-stringer resulted in no additional damage to the cells [7]. The soldering itself may be done with a hot soldering bar, infrared, induction, hot air, or lasers. Alternatively, conductive adhesives can be used in place of solder.

Several failure modes exist related to stringing and tabbing, evidenced both during the manufacturing steps as well as in the field. These include crack formation in Si during tabbing [8], poor solder joint formation resulting in solder bond failure, ribbon failure in the field due to mechanical fatigue, and corrosion of the ribbon. Predominantly, these failure modes are driven by the differences in the coefficient of thermal expansion (CTE) between copper (17×10^{-6} K^{-1}), silicon (3×10^{-6} K^{-1}) and glass (9×10^{-6} K^{-1}). For example, after soldering, the difference in CTE between silicon and copper will cause a buildup of internal stresses as the copper and silicon cool. Because of the increased contraction of copper during cooling, stress will form in the silicon wafer. Furthermore, the total current generated by the cells is increasing because of advances in cell efficiencies and the use of larger wafers. As attempts are made to limit the width of the ribbons, so as to reduce the shadowed area, thickness of the ribbons tends to increase. As the ribbon thickness increases, it becomes stiffer, thereby increasing the internal stress on the cell upon cooling after soldering [9]. On the other hand, the wafer thickness is being reduced to decrease silicon consumption, reducing the wafer's tolerance to internal stress. The overall effect of the reduced wafer thickness and increased ribbon thickness is a greater tendency of wafer breakage following the stringing and tabbing process.

A good solder joint is one where the solder wets the surface well and provides good adhesion between the two metals. In the case of solar cells, the two metals of interest are Ag (from the cell busbar) and Cu (from the interconnect). In theory, failure of the solder bond may occur at three different locations: (1) at the Cu interconnect/solder interface; (2) at the Ag busbar/solder interface; or (3) within the solder itself. In practice, failures at the Ag/solder interface, as well as within the solder itself appear to be the dominant modes [10, 11]. These failures were reproduced after thermal cycling experiments, indicating that thermal stresses due to CTE mismatch are the main driver for these modes. It should also be noted that for the solder to adequately bond to the Ag busbars, any oxides must be properly removed with the use of a flux.

In the field, diurnal heating and cooling will cause additional expansion and contraction of the copper, silicon and front glass. For example, since the CTE of glass is higher than that of silicon, an increased temperature will cause the glass to expand more than the silicon, thereby applying strain on the silicon as well as enlarging the gap between the cells. This increased gap width will strain the copper ribbons, which will subsequently apply stress to the wafer. This stress will be applied to both the ribbon and the bond between the ribbon and the busbar on the cell. The applied stress could cause the ribbon to fracture, the bond to fail, or possibly even the silicon substrate to crack. As was already noted, ribbon thicknesses are increasing, which could lead to greater field failures, since thicker ribbons are more susceptible to thermal fatigue. It should also be noted that the encapsulant plays a key role in determining the amount of stress experienced by the copper ribbon in the field, as the encapsulant can either couple or reduce the impact of the expansion of the glass front cover to the copper ribbon, depending on the encapsulant modulus of elasticity and its thickness [12].

Additionally, corrosion of interconnects will cause failure of the module. In 2008, Wohlgemuth reported [13] on module field failures between 1994 and 2005, wherein interconnect corrosion accounted for 45% of failures and cell or interconnect breakage accounted for 41% of failures. Current cycling has also been observed to cause burning at interconnects [14]. Techniques to mitigate interconnect failure include the use of lower CTE materials, stress relief bends, thinner ribbon, more pliable materials, and built-in redundancy [15].

The balance of this section will describe the failure modes associated with stringing and tabbing, with an emphasis on the manufacturing steps, and a few comments about field-failures. Following the failure mode descriptions, some details will be provided on in-line and off-line metrology techniques that can be used to assist in product development, process control and quality management.

3.2 Failure Modes

3.2.1 Microcrack Formation and Cell Fracture

Additional stress may be applied to the silicon cell itself, at the point of the busbar, due to the high CTE of copper over Si [7]. Microcracks will become a larger issue with the reduction of wafer thickness to below 150 µm, making the choice of the ribbon very important. In particular, the selection of ribbon with a high yield strength can cause significant cell bowing and ultimately lead to cell fracture after soldering [16]. Lower yield strength allows the ribbon to elongate (i.e. yield) during cooling, reducing the stress on the wafer. The ribbon thickness also impacts breakage rates, as thicker ribbons tend to give

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rise to more wafer breakage [17]. Applied pressure from the soldering tool can also result in high stress. It has been shown that the presence of defects near the busbar, due to soldering, result in a lower peel force of the copper ribbon from the busbar [18]. Gabor *et al.* demonstrated the impact of ribbon selection on cell damage, and concluded that ribbons with lower yield strength had a greater positive impact on cell quality than ribbons with lower CTE [7].

Cells will experience additional stress during lamination due to thermo-mechanical forces and in the field due to mounting stress, snow or wind loads, and thermal cycling. These stresses will allow microcracks that developed during stringing and tabbing to propagate and may ultimately lead to complete cell fracture. Cell fracture may result in current mismatch and hot spot formation significantly compromising module performance [19]. Therefore, minimizing microcrack formation is essential to improve module reliability. Examples of cell fracture as detected from electroluminescence images are shown in figure 2.
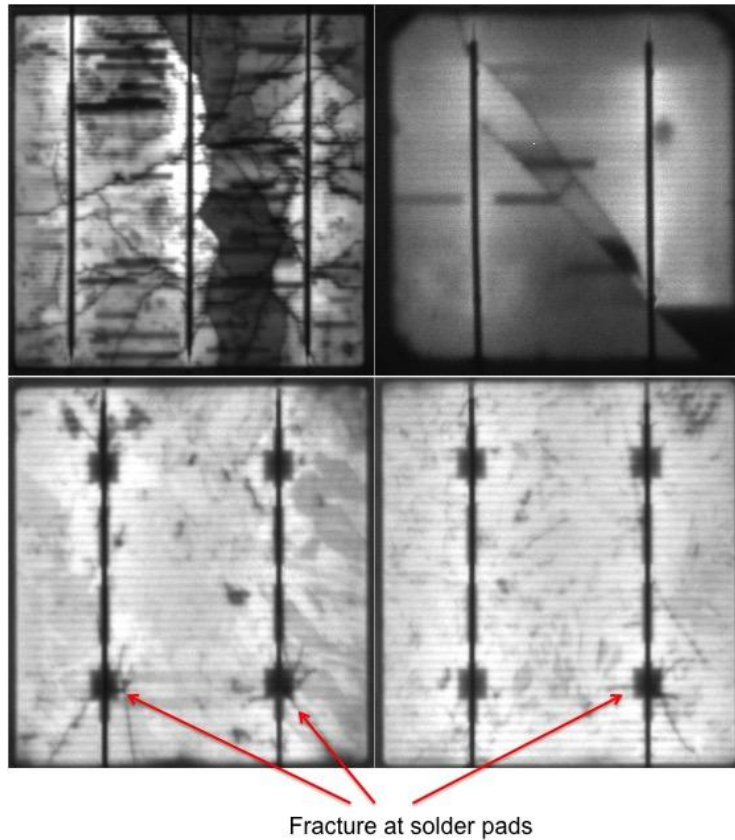
Figure 2. Electroluminescence images of fracture (top left) in a multicrystalline cell, (top right) in a monocrystalline cell, and (bottom) at the solder pads on two multicrystalline cells.

3.2.2   Poor Solder Joint Formation/Solder Bond Failure

Ex situ testing of the ribbon-busbar bond through peel testing revealed that the selection of the silver contact paste (screen printed) can have an impact on results [7]. In this study, for one paste, the peel test resulted in separation at the Ag/Cu interface, while another paste resulted in damage to the Si

below the busbar. Sunpower reported a 3% failure rate for hot solder joints, possibly due to weak solder bond [20]. Long lifetime of the module, as it relates to the solder and ribbons, was attributed to: using expanded metal interconnects, good solderability of the cell metallization, and using a compatible solder metal alloy. In addition, the size of the solder bond is relevant, as too small a solder joint will result in premature failure, while too large a bond results in greater stress applied to the wafer. Ribbon with lower yield strength will also reduce the stress on the solder bond, as the metal ribbon will deform more to accommodate the applied stress.

The morphological structure of the solder bond also plays a key role in durability. Metal diffusion from the solder has been implicated in bond failure due to coarsening effects [21]. One study found tin and silver between gridlines, indicative of diffusion from the ribbon over a 20 year period, suggesting that the solder bond strength will change with time [22]. Over time, metallic diffusion within the solder joint will cause increased grain size that can exacerbate thermo-mechanical failure, particularly in the presence of voids and cavities. In addition to field-related effects, soldering conditions will impact metallic diffusion. For example, both solder composition and time above liquidus during soldering tend to impact the leaching of Ag from the busbar to the solder. In an effort to reduce Ag leaching from the busbar, a small amount (~2%) of Ag is added to the solder [11]. For longer times above the solder liquidus state, greater amounts of Ag will leach into the solder, causing less adhesion to the busbar. In addition, the microstructure of the fired metallization has an impact on Ag leaching, with more porous metallization leading to greater Ag loss [23].

As the cell ages long-term stress relaxation and intermetallic diffusion can occur. The thermal stresses introduced during the soldering step can be mitigated somewhat through the relaxation of the solder over time. By using a thicker solder layer on the wire, a greater degree of relaxation occurs, which can improve the durability of the solder/busbar interface [23]. It should be noted that the adhesive forces observed in these tests showed a dependency on time, with significant increases in adhesion observed within 24 hours after soldering [23]. In the field, over longer time periods, thermal cycling will cause Sn and Pb crystallites to form within the solder, creating a more resistive interface and increasing the susceptibility to fracture [24].

One report indicated that loose connections are also possible in degraded modules, where intermittent contact is made with individual cells. EL images showed the same cell with different halves of the cell emitting light after successive thermal cycling [25]. Many interconnect systems are designed with several bonds along the length of the ribbon, such that failure of a few bonds does not significantly impact performance. However, a high fraction of bond failures will lead to an increased power loss, and subsequent heating of the cell, which can accelerate additional failure modes. It should be noted that an increase in current flowing through the cell interconnect would result in an increase in Joule heating, thereby accelerating coarsening of the solder joint for that cell interconnect. Thus, solder bond failure that effectively eliminates one cell interconnect will cause an increase in current flow through the remaining "good" cell interconnect(s), accelerating solder bond coarsening and potentially leading to further solder bond failures.

3.2.2.1 Impact of Lead-Containing and Lead-Free Solders

Cavities have been observed within the ribbon/busbar interface, due to poor soldering technique [11]. The use of lead within solder improves the solder bond for two reasons: improved wettability (to reduce the presence of cavities) and reduced soldering temperature (to reduce thermal contraction after soldering). However, lead is a toxic metal with a potential to cause harmful effects on brain, nervous system, liver and kidneys. Using solders containing lead can result in a hazardous waste classification for PV modules at the end of life, thus increasing the overall costs. This has caused a worldwide movement to altogether ban the use of lead in electronic products. 96.5%Sn/3.5%Ag and alloys with varying compositions of Sn-Ag-Cu have been proposed as a viable choice for Pb-free solder [26]. However, this variety of Pb-free solder has certain disadvantages over standard lead-containing solder such as about 40˚C higher melting point, poor wettability of certain variants, decreased life expectancy of soldering equipment like soldering tips [27]. Therefore, aggressive reliability studies have been performed on Pb-free solder in order to ensure durability of solder bonds in PV modules.

A US PV module manufacturer (ASE Americas) has used Pb-free solder in the modules since 1993 and independent reliability studies carried out at Arizona State University and Florida Solar Energy Center have shown that 96.5%Sn/3.5%Ag solder is at least as reliable as standard lead-containing solder [26]. In a comparative study of interconnects containing Pb-free (Sn3.5Ag) and standard (Sn36Pb2Ag) solders, Cuddalorepatta *et al.* have found that the void density from pre-test scanning electron microscopy (SEM) image analysis was 19% and 39% for Sn36Pb2Ag and Sn3.5Ag solders respectively [28]. This was attributed to lower wettability of Pb-free solder. However, during thermal cycling, the lead containing solder showed a linear increase in series resistance with the number of cycles while the Pb-free solder displayed a bilinear increase. A linear, non-conservative extrapolation of results observed during 1000 thermal cycles showed that Pb-free solder is about 3.5 times more durable than standard Pb containing solder.

The advantage of SnAgCu solder over 96.5%Sn/3.5%Ag solder are slightly lower melting point and better mechanical and wetting properties [29]. In a relative wettability study of two lead containing (SnAgPb and SnPb) and one Pb-free (SnAgCu) solder, Hsieh *et al.* observed that the Pb-free solder SnAgCu had lower contact angle and hence better wettability on Ag paste substrates than the lead containing variants [30]. However, the backscattered electron beam micrographs showed that significantly higher amount of intermetallic compounds were observed at solder/busbar interface for Pb-free solder than lead-containing solder; indicating potential reliability issues after thermal cycling. In another study, Hsieh *et al*. found that compared to the lead-containing solder (SnAgPb), the use of Pb-free solder (SnAgCu) resulted in higher series resistance of solar cells due to formation of uneven layer of intermetallic compounds [31].

The choice of Pb-free solder also impacts durability, with several reports of the Pb-free outperforming typical SnPb solder [10, 32]. The removal of Pb from solder causes a decrease in creep during thermal cycling, which contributes to its prolonged lifetime. However, by removing Pb from the solder, the number of voids increases, due to the lower wettability of the Pb-free solder on Ag. The use of more aggressive flux during soldering can improve the solder wettability, however it can have a detrimental effect on the lamination step. Ultimately, Cuddalorepatta *et al.* demonstrated that the effects of the

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void fraction within the Pb-free solder are not as great as the creep effects from SnPb solder, justifying the use of Pb-free solder on the basis of improved thermal cycling tolerance.

3.2.3 Ribbon failure

Ribbon failure is defined as fracture of the ribbon itself. Fatigue of a metal is defined as a reduction in material strength through repeated cycling, and can result in ultimate failure of the object under test. As noted previously, diurnal heating causes expansion of the gap between cells, which can strain cell interconnects. A sufficiently high number of cycles can lead to fracture of the cell interconnects. Meier conducted lifetime tests for the copper ribbon by determining the degree of strain experienced by the ribbon in a real PV module during thermal cycling, and then conducting high frequency stress/strain experiments on just the ribbon. He predicted a lifetime of about 5000 cycles [33]. Jeong *et al.* also discusses thermal cycling, but attributed failure to solder cracking, rather than ribbon failure [11].

Ex situ testing of the copper ribbon showed that the thermally-driven stresses applied to the ribbon could cause the ribbon to fracture within 30 years [34]. Bosco indicated that ribbon lifetime can be extended through inclusion of a sufficiently long non-soldered region between cells. Meier also stated that sufficient cycles will cause ribbon fracture, which may be exacerbated by the hardening experienced by interconnects during soldering [33, 35]. These papers note that there is sufficient deflection during thermal expansion and mechanical loading to apply significant stress to the ribbons. Notwithstanding the cycle fatigue experienced by the ribbon, solder bond failure appears more common than interconnect fracture in recent field-aged modules [21, 36]. It has been noted that two interconnect ribbons are used for redundancy, thereby maintaining performance in the event of a single interconnect failing. However, Shimizu *et al.* demonstrated differences in electroluminescence (EL) images for cells with one failed interconnect [37]. In this case, when one of the two interconnects failed (through busbar or back contact adhesion loss), only half of the cell was illuminated in EL. This process also results in loss of fill factor and therefore of power. This event will further lead to current crowding, where greater current is carried by one busbar than the other. As a result, the busbar and ribbon carrying the current will experience higher temperatures, thereby increasing the risk for failure. Current cell/module designs utilize three interconnect ribbons, which has further increased redundancy and reduced the risk of complete failure.

3.2.4 Corrosion

High system voltages, due to series connection of module in field-deployed systems, can result in large potential differences between the cell circuit and the module frame. Several tests have indicated that damp heat with positive voltage bias leads to significant corrosion of the interconnects, while negative voltage bias leads to interconnect oxidation and peeling of the solder bond [38, 39]. This corrosion is closely tied to the conductivity of the laminate used between the front glass and the silicon wafers. As it relates to the laminate effects, Kuitche *et al.* found that there was a strong correlation between delamination and broken cells or interconnects failure [40]. These effects clearly demonstrate that the material properties of one component can have a significant impact on the durability of others. Therefore, as durability testing continues, it may be necessary to look beyond the component in question (e.g. interconnects) and examine interactions with other module components (e.g. laminate).

3.3   Emerging Technologies

The previous sections dealt with the most widely manufactured cell technologies, namely *p*-type Al-BSF cells with screen-printed silver based metallization. As PV technology advances, novel cell architectures and interconnection technologies will be presented that enable higher efficiencies and lower costs than the current state of the art. These new technologies may exhibit the same degradation modes, new modes may be introduced, or accepted modes may be diminished. This section discusses very briefly some new cell architectures and interconnection strategies that show promise.

Rear side interconnects have been demonstrated that employ laser welding of the interconnect ribbon directly to the aluminum back contact [41-43]. The advantage of this technology is that it eliminates the need for screen printed silver pads on the rear side of the cell, which results in a reduction of the material costs and processing steps required for cell manufacturing. Additionally, laser welding has the potential to reduce the time and energy associated with stringing and tabbing process during module manufacturing. Initial aging data suggests this technique does not impact cell performance over time [42], however more reliability studies are needed to understand how this technology performs with respect to common failure modes such as cell fracture and interconnect durability.

Since the majority of the internal stress at the interconnect/wafer interface is due to heating during soldering and CTE mismatch, forming electrical connections at low temperature is desirable. Additionally, high efficiency heterojunction cells require low temperature interconnect formation to prevent a reduction in passivation quality at the a-Si:H/c-Si interfaces on the front and rear of the cell [44]. As an alternative to hot-solder bonding, ultrasonic bonding is a non-standard technique that shows good promise in terms of reliability [45]. In this method, ultrasound is able to join metals without excess heat being generated, and without the use of solder. By reducing the heat, the internal stress build-up has been reduced, and the lack of solder eliminates intermetallic diffusion of tin. While this approach was used to attach aluminum ribbons to thin-film Si cells, it may not be suitable for c-Si cells, which may suffer high breakage rates due to ultrasonic vibrations and the pressure of the ultrasonic tool on the cell. Conductive pastes have also been used for these purposes [46-51]. These pastes have shown good electrical contact, some with peel strengths comparable to soldering [46, 51], but long-term durability remains uncertain. Schwertheim *et al.* reports *ex situ* thermal cycling of conductive adhesive-bonded interconnects showing an increase in contact resistance after 50 cycles. However, this same report showed laminated heterojunction solar cells with conductive adhesives exhibiting very little change after 200 thermal cycles [48]. Owing to the more complex nature of conductive adhesives (e.g. filler to epoxy ratio, curing temperature and time, bleeding [52]), a great deal more work needs to be conducted before industrial implementation. Additional research on the aging and reliability of conductive adhesives as it relates to fielded modules is also required.

In recent years, novel metallization schemes have been proposed to increase cell efficiencies and reduce cost [53]. Due to price pressures in cell manufacturing, there is a growing interest in the ability to replace silver metallization with a copper based alternative [54, 55]. Alternatively, newer device architectures that allow for improved device efficiencies, such as *n*PERT (*n*-type passivated emitter, rear totally diffused cell), demand new metallization pastes in order to reduce recombination at the contacts. Although several challenges must be overcome before these technologies are implemented in large

scale cell manufacturing, it is important to identify how this might influence the stringing and tabbing step. This may require refined solder compositions, reduced processing temperatures, or alternative soldering techniques to ensure reliable solder bonds and cell interconnects. Reliability studies of modules that have successful passed standard IEC qualification protocols are beginning to emerge for modules that incorporate copper based metallization [56, 57]. Before widespread adoption of these novel metallization strategies can occur, further research investigating the reliability of interconnection schemes for these cells is required.

Another approach to reduce costs and enable higher efficiency cell architectures is to eliminate metallized busbars and utilize a multi-wire cell interconnection [58, 59]. This technique, used mainly for silicon-heterojunction devices, reduces costs by lowering silver consumption and improves performance by reducing series resistance and increasing the active area of the cell. There are also advantages in terms of reliability due to the increase in the number of interconnect between cells. There is growing interest in this multi-wire approach to cell interconnections, with the adoption rate in industry expected to increase in the coming years [60].

3.4   Relevant Metrology techniques

The materials and processing used for stringing and tabbing have a significant impact on the reliability and durability of modules in the field. This section discusses the various metrology methods available to evaluate potential materials and processing techniques to ensure reliable cell interconnection schemes are being used in the manufacturing process.

3.4.1   Electrical Characterization Techniques

Determining interconnect degradation may be accomplished via increases in series resistance (R_s), since failure can lead to larger contact resistance and/or increased current concentration along single interconnects. One of the methods employed to determine series resistance is to analyze the illuminated or dark I-V curves of the cell and to extract series resistance using an appropriate model (e.g. the two diode model). Several techniques have been proposed [61]. These techniques each suffer from various limitations based on the assumptions of each model, such as requirements that short circuit current (I_{sc}) vary linearly with illumination, that the cell be illuminated at different levels while maintaining constant temperature, or that series resistance is invariant with current (which is incorrect) [62]. Additionally, series resistance is a function of several factors, such as emitter resistance, metallization resistance, and emitter/metal contact resistance. Therefore, not only does this method produce series resistance values with varying degrees of uncertainty, it is difficult to separate the solder bond resistance values from the series resistance of the cell. Within a string of cells, it is possible to use I-V curves to identify weak cells, through sequential shading. As each cell is shaded, the subsequent reduction in I_{sc} is monitored, and for those cells with poor performance (due to e.g. high series resistance), the drop in I_{sc} will be lower. The cells with higher performance (due to e.g. lower series resistance) will have a greater impact on I_{sc} [63].

Field-testing of interconnects may be achieved through the use of a cell line checker tool. A transmitter is connected to the leads of the module, which then applies an ac-signal to the circuit. By scanning a

receiver over the surface of the module, high resistance and failed interconnects can be identified [64, 65].

3.4.2   Imaging Techniques

High-resolution images of the solder/wafer interface have been obtained using SEM techniques. In this approach, the cell is removed from the module, mounted in an epoxy and the cross-section is exposed through polishing. Chemical analysis is also possible through energy dispersive x-ray analysis (EDX), permitting an in-depth study of the metallic phases near the bond [66, 67]. Clearly, this technique requires destroying the original cell, but useful information about the solder bond quality, such as voids and cracks, may be obtained, which could then be used for process optimization.

Meier *et al.* measured the expansion of solar cells in a PV module by digital image correlation (DIC), which required creating a spray pattern on the surface of the cells [33]. By measuring the expansion of the cells, the strain on the ribbons could be determined. This technique does not lend itself to relevant testing in the factory or field, but rather to diagnostic testing in the lab.

Infrared (IR) thermography has been used to identify hot spots in solar panels for several years. Often, the hot spots are due to reverse bias of a shaded cell or to areas of low shunt resistance. However, Joule heating of the solder ribbon as a result of weak or failed solder bonds may also produce hot spots [68-71]. These measurements can be made indoors (typically in the dark) under forward or reverse bias, or under illumination (typically outdoors) with the cell or module either under short circuit conditions or under load. Dark infrared imaging eliminates the heat generation due to cell mismatch (i.e. eliminates reverse biasing of individual cells) and allows for better resolution of interconnect issues. In this approach, current flows through the cell or module and areas of increased temperature are imaged using an IR-sensitive camera, with wavelength sensitivity typically in the 3-10 μm range. In series-connected cells, weak or failed solder joints will cause an increased current density through the remaining good joints, which will cause a subsequent increase in temperature [70]. Therefore, the hot spots actually correlate with regions of good solder joints, while the poor solder joints must be inferred. The front glass of a module will cause thermal diffusion, effectively broadening the signal and reducing the precision of this method. Imaging through the backsheet can reduce this effect, however the junction box and module frame may obstruct the cells or interconnects. Pulsing the current while obtaining a sequence of IR images, then digitally combining these images utilizing the pulsing frequency, known as lock-in thermography, significantly increases the signal to noise ratios. This technique allows for extremely precise imaging of the thermal sources within the module.

EL Imaging has also been used to extract information regarding series resistance and interconnect failure as shown in figure 3. EL imaging, which utilizes the near infrared (NIR) radiation produced from band-to-band recombination in the active semiconductor layer, has been used at both the cell and module level to provide localized visualization of resistance and to help quantify of the degree of failure [72-74]. In this method, an electric potential is applied to the cell or module, generating a current through recombination. This recombination process generates photons that are detected with an NIR-sensitive CCD camera to provide spatial resolution of the device quality. In general, EL shows areas of lower intensity for those regions with high resistance, as less current is able to flow. These darker areas

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have been correlated to power losses by Gazuz *et al.* [72]. A modified version of EL imaging, labeled as R_s-EL imaging, was used to detect poor solder joints by extracting the luminescent and ohmic (i.e. series resistance) component for each pixel from images taken at two voltages [75]. Differential EL imaging easily revealed the location of cracks in the silicon after mechanical load tests, either parallel or perpendicular to the busbars [76]. The locations of these cracks revealed which areas of the cells were rendered inactive due to electrical discontinuities, allowing a "criticality" factor to be applied to the types of cracks. For example, cracks parallel to the busbar were more detrimental to cell performance than cracks perpendicular. Grid-finger failures have also been identified with EL, where rectangular dark regions in EL were attributed to finger failures [76].
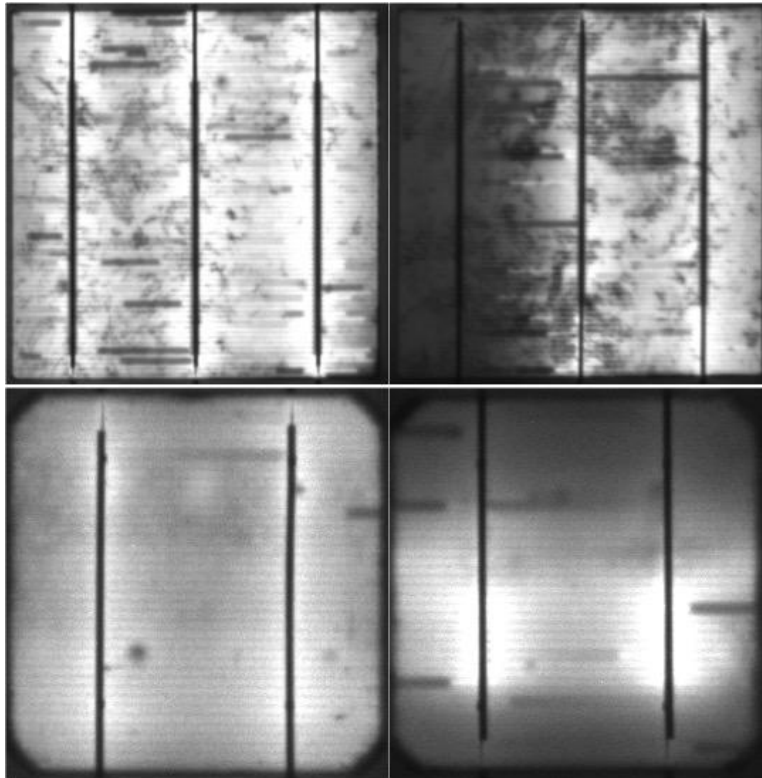
Figure 3. Electroluminescence images of (top left) typical multicrystalline cell, (top right) multicrystalline cell with a broken interconnect, (bottom left) typical monocrystalline cell, and (bottom left) monocrystalline cell with variable contact resistance along the busbar.

3.4.3   Mechanical/Thermo-Mechanical Metrology Techniques

A common method of determining adhesion strength between the interconnect and the silicon cell is the peel test, where one end of the ribbon is pulled while the wafer is held still. The force required to separate the ribbon from the wafer is indicative of the solder strength and hence the quality of the bond, although damage to the silicon wafer through improper soldering can also impact results [77]. The pull test can be useful during the optimization of the soldering process to assure that up to a certain stress level the solder bond does not fail, however this test results in damage to the cell [78]. Hence it cannot be used for routine in-line testing, although module manufacturers often use this technique to qualify processes and equipment.

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In terms of the cycle fatigue of the ribbon itself, dynamic mechanical analysis (DMA) has been conducted, where the ribbon is mounted between two clamps and a cyclic force is applied to the ribbon until failure occurs [33]. This test is useful for determining ribbon cycle lifetime, provided the applied stresses and geometry are relevant to the field. However, as for the pull test, DMA provides good input for process optimization, but is not applicable for real-time process or quality control.

Temperature cycling of modules has been shown to demonstrate failure through thermo-mechanical modes, similar to what would be expected in the field, but at an accelerated rate. Additionally, thermal cycling with applied current has identified weak solder joints faster than thermal cycling alone [20, 79]. Simple thermal cycling will screen modules for issues related to thermal expansion, but will not discriminate against poor solder bonds. By applying current to the module (at or near short circuit), modules with poor solder bonds will be identified. A second method proposed by Aoki *et al*. demonstrated an ability to predict solder bond failure through increased resistance [80]. The use of thermal cycling as a quality control method has been employed for several years, and the International PV Module Quality Assurance Task Force (PVQAT) is working to extend this qualification test. For example, Task Force 2 has identified that 200 thermal cycles is not sufficient as module with durable interconnection schemes have been shown to survive several hundred thermal cycles [81]. Test protocols that incorporate additional stressors prior to or after thermal cycling, including dynamic mechanical loading, may lead to more stringent requirements for solder bonds quality and as a result extend module lifetimes.

3.5   Gap Analysis

The PV and electronic industries have adopted some variant of the Pb-free solder as a material of choice over standard Pb-containing solder due to toxicity of lead. The 96.5%Sn/3.5%Ag Pb-free solder has approximately 40˚C higher melting point than Pb-containing solder, however it has proven to be at least as reliable as Pb-containing solder, if not more. The SnAgCu solder has advantages of slightly lower melting point and better wettability than 96.5%Sn/3.5%Ag solder. Further research is required to predict if the higher amount of intermetallic compounds found in SnAgCu have a detrimental impact on the long-term reliability of solder bonds.

Thermal cycling with current through the module has been used to test the durability of interconnects and solder bonds in PV modules. Once interconnect breakage, solder joint failure, or cell fracture occurs during thermal cycling, the state and distribution of mechanical loading on the modules can influence the electrical connection at that point [7]. Also, it has been recently shown that the cracks generated in c-Si cells during thermal cycling can heal themselves in subsequent thermal cycles [82]. These effects can introduce a certain degree of uncertainty in the results of I-V measurements and EL imaging. There is a need to further understand the effect of mechanical loading and subsequent thermal cycling on state of electrical connection of broken interconnects and opening and closing of cracks in c-Si cells so as to better interpret the results from I-V measurements and EL imaging.

A metric that is commonly used to compare the reliability of various soldering techniques and interconnection materials is pull strength. This metric, although useful in the evaluation of new solder techniques, is not necessarily indicative of the reliability of a particular interconnect. Because the

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module encapsulation provides mechanical support for the cells and interconnects, it is possible for poorly adhered interconnects to continue to provide good electrical conduction over time. With the ever growing need to reduce costs, research that investigates how various interconnection schemes perform over time in terms of electrical conductivity are required. Various studies have shown that issues such as corrosion, metal migration, and creep are responsible for degradation of interconnects[83-85]. The relationship between the pull strength and these more fundamental mechanisms is unclear and may vary depending on the materials and interconnection scheme, therefore a more fundamental understanding of the relationship between adhesion and electrical performance over time is required.

4.   Lamination

4.1   Background

Photovoltaic (PV) modules rely on packaging materials to provide protection from external mechanical, environmental and system induced stresses in order to ensure reliable performance over the operational lifetime. The module packaging must also prevent potential hazards (e.g. electrical arcs, ground faults, exposed circuitry) and ensure safe operation of the photovoltaic device. Packaging materials, as depicted by the cross-sectional diagram in Figure 4, include protective frontsheets, backsheets, internal encapsulants, and sealants/adhesives (both between the edge of the laminate and the frame and as mounting adhesives on the backside for the junction box).

All packaging materials must withstand the environmental condition in which the module will be operating. This includes high temperatures, humidity, rain, UV exposure, wind loading and others depending on the location (e.g. ammonia vapors, salt water, dust). In many cases the packaging must not just withstand these conditions, but must also prevent these conditions from reaching the active internal components. Together these materials must remain mechanically secured and provide adequate electrical insulation to prevent operational hazards. The following sections will discuss the various module packaging components and the specific requirements for each.
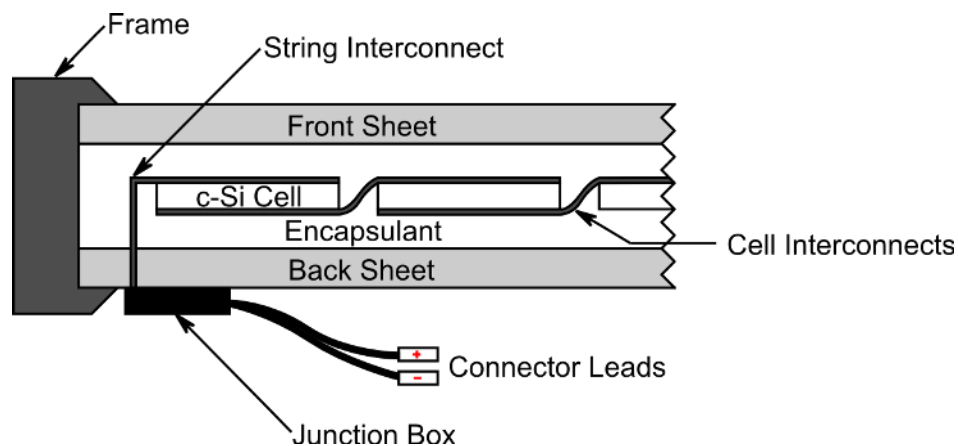
Figure 4. Cross-sectional diagram of a typical module packaging configuration.

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4.1.1 Frontsheet

In addition to providing protection to the active internal components, the frontsheet, or front cover, has several unique functions within the packaging scheme. Because it is located above the PV cells, the frontsheet must provide suitable transmission of the solar spectrum, low reflectance at oblique angles and have an appropriate index of refraction based on the properties of the encapsulant. Beyond the mechanical loading due to high winds and/or the mounting configuration, the front sheet is the first line of defense from any mechanical impact such as hail or other small debris. This requires a material with high impact resistance and sufficient tensile strength. Also, because this material is on the topside, it will experience extremely wet conditions due to rain and condensation. The frontsheet should also allow for sufficient interface adhesion with the encapsulant. Therefore the essential requirements for the frontsheet include high optical transmission (UV-VIS-NIR), low coefficient of thermal expansion, good UV stability, excellent weatherability, high impact resistance, and high electrical resistivity (i.e. good electrical insulation).

Typically, glass is used as the frontsheet material. Glass, specifically low iron soda-lime glass, exhibits all of the required electrical and optical properties. It is also impervious to water and water vapor and can be made very strong by heat strengthening. c-Si based modules almost exclusively utilize glass as the front cover, however there are some cases in which a flexible frontsheet may be required, such as building integrated photovoltaics (BIPV). Advantages of polymeric frontsheet are the lower weight constructions and the elimination of glass breakage. On the other hand, many polymeric films do not retain good light transmission over long time periods outdoors, and are generally permeable to water vapor. Fluoropolymers have been shown to retain good light transmission outdoors and are used in a number of flexible PV packages, although they are generally used with alternative PV technologies such as amorphous silicon (a-Si) or Copper Indium Gallium Selenide (CIGS) [86].

4.1.2 Backsheet

Backsheets, or back covers, provide protection to the PV cells from the rear side. Because they are behind the cells they are not required to be optically transparent. They are however, still exposed to the outdoor environment. Therefore, they must be moisture resistant and have adequate UV stability, as they will be exposed to UV radiation through the package and from diffuse light on the back surface. They should have sufficient mechanical properties in order to be scratch resistant and withstand puncture. Additionally, the internal surface of the backsheet must allow for adequate adhesion to the encapsulant and the external side must provide a surface in which a junction box can be attached and sealed to prevent water penetration.

Backsheets are typically multilayer structures comprised of three polymeric films. The middle layer is the core material that acts as the main permeation barrier and provides the required electrical isolation. The outer layer provides adequate protection from weathering and the inner-most layer is chosen to have good adhesion to the encapsulant. These layers are typically glued together with adhesives such as epoxy or polyurethane.

The core layer has traditionally been a polyester such as polyethylene terephthalate (PET) because it provides adequate performance at reasonable costs. Other possible core layers include other

thermoplastics such as polyamide (PA) or polyolefin (PO) materials. Thin inorganic films such as alumina or silicon oxide can been deposited on the inner core layer to reduce permeation and improve the barrier properties of the backsheet [87-89]. In some cases aluminum foil has also been used for this purpose [89]. The outer layers are often fluoropolymers, due to their resistance to environmental effects. Specifically, the DuPont Tedlar® polyvinyl fluoride (PVF) film has been used extensively within PV module backsheets over the past 30 years [90, 91]. Other fluoropolymers that have been used include polyvinylidene fluoride (PVDF), tetrafluoroethylene hexafluoropropylene vinylfluoride (THV), and polychlorotrifluoroethylene (PCTFE) [92, 93]. Although fluoropolymers are the most common outer layer, some configurations utilize a stabilized PET or PA on the external surface. The inner layer is either another fluoropolymer or a tie layer, which is typically an ethylene vinyl acetate (EVA) formulation that provides good adhesion to the encapsulant.

Interestingly, most backsheet films have relatively high water vapor transmission rates allowing water vapor to penetrate into the module. Along with water vapor, other gases and liquid vapors are also permeable such as oxygen or acetic acid [94, 95]. This has a significant impact on the occurrence and progression of degradation and will be discussed further in Section 4.2.5. In contrast, glass back covers are impermeable to such gases and liquid vapors and provide a much different operating environment for the PV cells[96]. Such glass-to-glass packages can also employ edge seals to further prevent moisture from entering the module. This type of packaging is however, much more common for alternative PV technologies in which moisture is much more detrimental to the cells[97]. There is also evidence to suggest a glass back cover may induce more strain within the cell interconnects affecting reliability [98].

4.1.3   Encapsulant

An encapsulant, or pottant, is the material sandwiched between the front and back covers that is in direct contact with the cells of the module. The role of the encapsulant is to provide protection to the cells from physical, electrical, or chemical stressors during operation. Mechanically, encapsulants must provide flexibility to prevent expansion or contraction of the package from applying mechanical stress to the cells or interconnects while also maintaining its own mechanical integrity and adhesion to the front and back covers, cells, busbars, and interconnects. Electrically, encapsulants must have high resistivity to ensure proper electrical isolation of the active components. Additionally, adequate thermal conductivity must be provided by the encapsulant to prevent excessive heating of the components. Because the encapsulant is located directly on the top of the cell, the material must be optically transparent, provide adequate optical coupling, and be UV resistant. Finally, the encapsulant must prevent corrosive or destructive contaminants from reaching the cell surface.

Encapsulants are typically in the form of a polymeric sheet consisting of a resin, curing agent, and other various additives. Additives generally include cure accelerators, adhesion promoters and primers, antioxidants, and UV stabilizers or absorbers. Upon heating the mixture cures, mechanically securing the cells within the front and back cover. Because of this curing or lamination step, additional material requirements are introduced for the encapsulant. The curing process should occur in a timely manner at sufficiently low temperatures (less than 160 ^{o}C) to avoid stress introduced from differences in the coefficients of thermal expansion for the internal components (i.e. copper interconnect ribbon and

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silicon cell). Another factor that must be considered is the volume change due to curing. The material should not shrink or expand to a point in which additional stress will be applied to the cells. Additionally, the encapsulant should exhibit a relatively long shelf life, retain its desired properties after storage or transportation, and cure in a repeatable and reproducible manner.

In the PV industry, ethylene vinyl acetate (EVA) is the most predominantly used encapsulant with the use of certain formulations dating back to the early 1980's [90, 99]. Although there are various formulations that may exhibit somewhat different properties, EVA has been shown to perform all of the required functions of the encapsulant [100]. Other polymers, including poly-ethylene-co-methacrylic acid (ionomer), polyvinyl butyral (PVB), thermoplastic urethane (TPU), poly-α-olefin, poly-dimethylsiloxane (PDMS) or other polysiloxanes (silicone) have been proposed for the same application.

4.2   Failure Modes and Degradation Mechanisms

A loss in the basic functions of the module packaging can lead to catastrophic failure of the PV module. This packaging breakdown may result in complete failure of the module through electrical performance loss or operational safety hazards. Generally, failure within the packaging scheme itself does not reduce the electrical performance of the module. Instead, this failure results in the acceleration of a secondary degradation mechanism, which the module packaging was meant to suppress. This section will review the various failure modes of the module packaging materials themselves along with a discussion of relevant failure modes influenced by the properties of the module packaging.

4.2.1   Encapsulant Discoloration
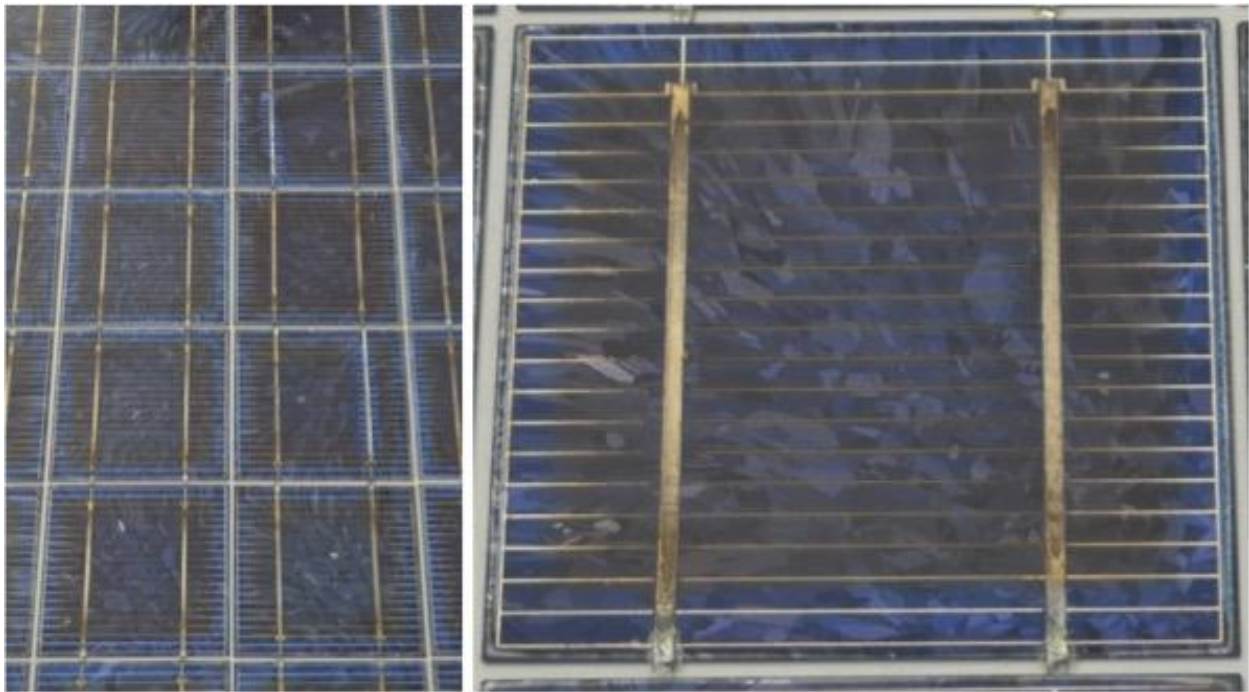
Figure 5. Image of encapsulant discoloration above the center region of each cell in a field deployed module.

Discoloration of the encapsulation materials is a visual indicator of chemical degradation within the polymers. Because the encapsulant is above the cell, discoloration results in optical losses and a

reduction in the light incident on the PV cell. Such discoloration of encapsulant materials, known as yellowing or browning, has been linked to extended UV exposure [101]. Studies have shown that UV exposure at elevated temperatures results in photochemical degradation of specific additives within the EVA through the generation of chromophores [102, 103]. As aging continues, discoloration progresses from light yellowing to more severe browning. In fielded modules, discoloration has been observed almost exclusively above the center of the cell [104], as can also be seen in Figure 5. It was found that oxidative destruction of the previously formed chomophores, known as photobleaching, occurred wherever oxygen diffused into the encapsulant through the backsheet. This resulted in degraded but non-discolored EVA. The occurrence of this type of degradation has been reduced significantly by careful selection of EVA additives. Fluorescence imaging has been suggested as a method to detect this type chemical degradation before visual discoloration takes place [105]. There is, however, little knowledge of the actual chemical processes linking fluorophore (detected during fluorescent imaging) and chromophore formation. Therefore, fluorophores should not be assumed to be a precursor chromophore formation. In fact, flourophores typically operate in the UV region where they could act beneficially as a UV blocker or by dropping non-absorbed wavelengths down to where they could produce energy in the PV cell. An example of a fluorescence image captured using a UV light source and a standard optical camera is shown in figure 6.
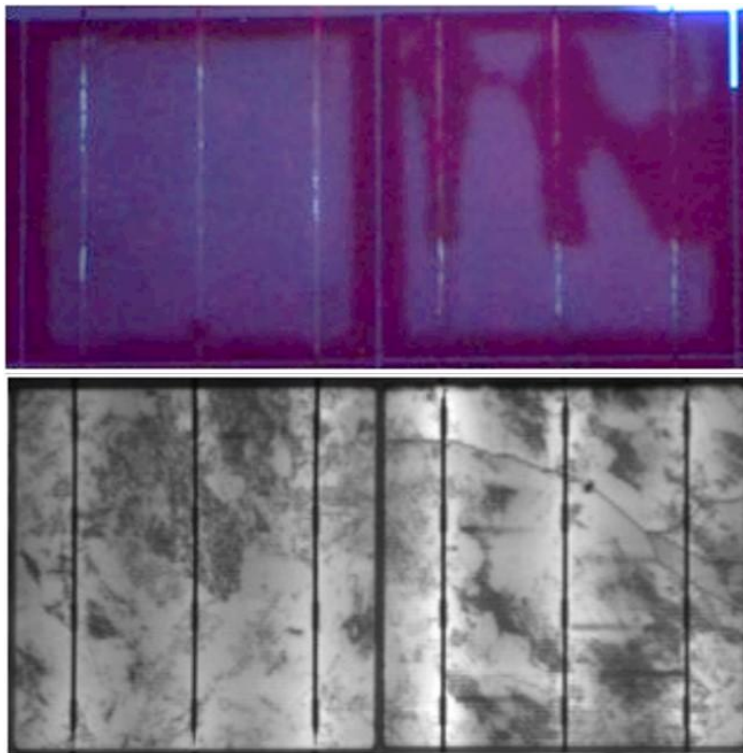
Figure 6. (Top) Flourescence image of two adjacent cells and (bottom) an electroluminescence image of the same two cells. No fluorescence can be seen in the region above the crack and in between the cells due to oxidative photobleaching in these regions.

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4.2.2 Backsheet Degradation

Backsheet degradation is generally observed as cracking, discoloration, or inter-layer delamination [106, 107]. Unlike yellowing of the encapsulant, discoloration of the back sheet material will not directly impact module performance, as it is not within the optical path of the solar radiation. Although backsheet yellowing itself is not detrimental, it is often accompanied with other chemical or mechanical degradation of the backsheet [108]. As was the case for the encapsulant, UV exposure has also been linked to the discoloration in backsheet materials. UV degradation also causes embrittlement of the material, and often leads to cracking. UV radiation reaches the inner surface of the backsheet through the spaces in between cells, and also affects the back surface from diffuse reflection. Fluoropolymers often have very good UV-stability, so care should be taken when utilizing other polymers as the inner or outer backsheet layers. UV stability of all layers in the backsheet is recommended to ensure reliable operation.

Thermal and moisture instability has also been shown as a cause of chemical and mechanical degradation in backsheet materials. Typically this is observed as embrittlement and cracking of the backsheet [109]. Hydrolytic degradation under extended damp-heat conditions is a well-known failure mechanism for PET [110]. Failure of PET after several thousand hours in damp heat (85° C - 85% relative humidity) through a breakdown of the mechanical properties (e.g. cracking or reduction in tensile strength) has been observed by several groups [111-113]. Other work has suggested that PA and PO core layers exhibit less hydrolytic and thermal degradation than PET, and as expected most flouropolymers show very little loss in mechanical properties after damp-heat [114]. It is important to note that Kempe and Wohlgemuth have shown, in regards to PET hydrolysis, that extended damp-heat correlates to hundreds or even thousands of years of field conditions depending on the operating environment meaning this type of degradation is irrelevant for PV applications[115]. This work emphasizes that accelerated testing can potentially lead to unnecessary over-engineering of the encapsulation, so correlation to field conditions should always be considered when evaluating a particular packaging scheme. When unstabilized polymers (e.g. non-fluoropolymers) are used as the outer layer, degradation has been observed in relatively short time-periods [116].

Delamination internally within the backsheet is another potential failure mode for backsheets [117, 118]. This is generally the result of mechanical degradation of one of the polymer layers, although it may also be a result of failure in the adhesive used between the layers. The multilayer structure is typically secured together with the use of a thin (3-6μm) adhesive layer [93, 119]. Studies have shown that delamination within the backsheet is less likely than delamination at interfaces with EVA because the adhesive fracture energy forces are much higher [88]. If however, degradation of the adhesive occurs, backsheet delamination may result. Adhesive degradation has been shown to accelerate with UV, humidity, and ammonia vapors [119, 120].

Finally, burn spots in the backsheet have also been observed in degraded modules [109, 117]. These burn spots are a result of excessive heating, typically at a cell interconnect. This is not a failure of the backsheet however; this is a failure of the cell or of the interconnection scheme. Although backsheets should be designed to withstand high temperatures in excess of 150° C, is not economically feasible to engineer backsheets to withstand extreme temperatures due to cell level failures.

4.2.3   Delamination

Delamination is one of the most documented failures in fielded PV modules [90, 109, 117, 118, 121, 122]. This can occur at any interface within the packaging including the frontsheet/encapsulant, encapsulant/cell, or encapsulant/backsheet interfaces. Delamination above the cell has a direct impact on the performance due to a reduction in incident radiation from light scattering and reflection at the exposed interface. Although not all delamination events directly influence performance, they significantly compromise the reliability of the PV module. Cell degradation and interconnect corrosion are accelerated as these delaminated interfaces become direct paths for moisture ingress within the module [123, 124]. Delamination, specifically on the backside of the cell or at the backsheet/encapsulant interface, is also a potential safety hazards as this often exposes the active circuitry and reduces the insulation resistance of the package.

There are a number of factors that influence delamination at a particular interface. When studying aged modules from harsh coastal climates, Dhere *et al.* has shown a correlation between impurity accumulation, specifically sodium and phosphorus, and a reduction in adhesion strength at the cell/EVA interface [125]. Although these modules did not exhibit delamination, other studies have confirmed that delaminated interfaces do in fact have high concentrations of impurities [122]. Furthermore, these studies identified that other driving forces in addition to elemental impurities, such as high levels of moisture and high temperatures, were required for delamination to occur [126].

The surface preparation of the glass prior to lamination can also have a significant impact on the quality and reliability of the interfacial adhesion. Depending on the type of contaminants that are to be removed, different cleaning procedures can be employed and may include mechanical processes, acid or base cleaning, ultrasonic baths, or detergent cleaning. In general, good adhesion is achieved when the glass surface exhibits a high surface energy. It was observed that even though industrial detergents resulted in lower surface energies (i.e. hydrophobic surfaces) the adhesion was equivalent to that observed in hot-acid rinses [89]. To further improve the adhesion between the glass and EVA, adhesion promoters, or primers, have been added within the EVA [127]. These primers are generally the least stable additive in EVA and can be the limiting factor in terms of the shelf life of the EVA. It may also be necessary to prepare the cell surface prior to lamination. Residual flux from the stringing and tabbing step may result in very poor adhesion to the cell. This is generally observed in the field as delamination near the cell busbars [109] as shown in figure 7.

Figure 7. Image of module with delamination of the encapsulant near the busbars on each cell.

Poor surface preparation may result in the formation of voids, or bubbles, in the encapsulant during lamination and these regions may become nucleation sites for delamination during operation. The lamination processing steps utilized during manufacturing should effectively minimize the occurrence of voids to ensure reliability. The temperature profile used during lamination is also critical in ensuring sufficient mechanical bonding of the laminate. Recent work indicates that an accelerated cooling process can improve the interfacial adhesion [128].

The mechanical properties of the encapsulant can also affect the occurrence of delamination. Encapsulants are required to have a relatively high elastic modulus to accommodate for any variations between the expansion and contraction of the cells, interconnects, or glass. A reduction in the elastic properties of the encapsulant may result in delamination in addition to increasing the stress levels within the cells and interconnects [40, 122].

4.2.4 Mechanical Failure of the Encapsulant

One typical failure mode identified in a number of field-deployed systems is broken or shattered module glass. Broken glass can pose a significant safety hazard not only from the sharp broken glass pieces, but also electrically through the loss of insulation resistance. Additionally, this provides a direct route for moisture and other contaminants to enter the module. The use of heat strengthened, tempered glass provides a significant increase in the fracture strength as compared to other non-tempered glasses. To provide assurance against this failure, the c-Si module qualification sequence, IEC 61215, includes an impact test for hail and large loads. Even with these qualification tests there may still be glass breakage in the field due to human interaction, extreme weather, or simply from thermo-mechanical forces. The use of a flexible front sheet may provide protection from this failure mode, however the optical, electrical, or permeation properties provided by the front glass may be compromised.

Permanent deformation or movement of the encapsulant due to mechanical stresses, defined as creep, has been identified as a potential issue when utilizing thermoplastic materials. The magnitude of creep is dependent on the viscosity of the encapsulant at module operating temperatures and the stress distribution within the module. A recent NREL experiment indicated that the dangers from creep have been overestimated and that it may not be relevant for typical module installation environments [129]. It was shown that only modules with unrestrained front glass were susceptible to creep and that mechanical support (i.e. module frame), or non-uniform temperature distributions, acted to resist the occurrence of creep.

The encapsulation also plays an important role in providing adequate mechanical support, and flexibility. The elastic nature of the encapsulant is required to prevent stress build-up from the expansion and contraction of the internal components within the laminate, as well as to absorb any external stress from the mounting structure, or from snow or wind loads [12, 82]. It has been shown that the elastic modulus significantly affects the ability of an encapsulant to protect the cell from mechanical stress [130]. Since EVA exhibits a glass transition temperature within the operational range for PV modules, the mechanical properties can vary significantly depending on the temperature [131]. If mechanical stress is applied when the module is at sufficiently low temperatures (i.e. when the elastic modulus is significantly increased) the potential for cell fracture or interconnect failure will increase which will negatively impact module performance.

4.2.5 Influence of Encapsulation on Corrosion of Cells and Metallic Interconnects

One main function of the module packaging is to prevent harmful or corrosive contaminants from reaching the PV cells. Corrosion, or oxidation, of the active components depends largely on the presence of oxygen and water vapor [89, 103]. Therefore, it is essential that the encapsulation prevent significant amounts of these reactants from reaching the cell surface, metallic gridlines or interconnects. The permeation properties of water vapor and oxygen have been studied for a number of backsheet materials and encapsulants [94, 132-134]. It has been shown that the permeation and diffusion processes for water vapor and oxygen exhibit strong temperature dependence, even above glass transition temperatures, allowing for an Arrhenius relationship to be applied. In one study it was identified that PA-based backsheets exhibited a much stronger temperature dependence that resulted in a comparatively lower permeability at lower temperature and comparatively higher permeability at higher temperature than PET-based backsheets [94]. Because of the large temperature dependence of the various encapsulant and backsheet materials, Hulsmann *et al.* recommended that materials suppliers provide not only a single value for permeability and diffusivity, but include temperature dependence as well.

The level of moisture within a module encapsulant is governed not only by the water vapor transmission rate of the backsheet and encapsulant but also, and often more dominantly, by the water vapor diffusion coefficient of the materials and saturation limits of the encapsulant [133-136]. Kapur *et al.* studied the properties of several encapsulants and identified that ionomer encapsulants exhibited much lower diffusion coefficients than EVA and PO. This data was then utilized to predict the moisture content during extended damp-heat testing (85° C - 85% relative humidity). The simulations show that at the

center of a typical 15.6 x 15.6 cm cell, 1000 hours of damp heat resulted in 65 percent saturation of the EVA and less than 2 percent saturation for the ionomer.

Wohlgemuth and Kempe have shown, however, that extended damp-heat testing is not representative of conditions experienced in the field, and testing beyond 1000 hours may result in unnecessary over-engineering of the module packaging [137]. Moisture ingress simulations were carried out utilizing historical weather data for a module with EVA and a typical backsheet. It was assumed that the diffusion coefficient of the EVA is much less than that of the backsheet, and it was calculated that the moisture content in the EVA at the back of the cell equilibrates in timescales of less than a day. Therefore, the moisture content follows daily cycles of relative humidity. On the other hand, the moisture on the front surface of the cell must diffuse sideways from the regions between cells and, depending on the distance from the cell edge, the moisture profile will equilibrate on timescales of months or years [135, 138]. It was shown that beyond the initial rise in moisture content in the EVA on the front side, the moisture profile would deviate only slightly along with seasonal variations. This is due to the fact that the source of moisture on the topside (i.e. the moisture content within the encapsulant at the back) fluctuates throughout the day and is effectively much lower than would be observed for a steady state damp-heat condition.

Therefore, in regards to the properties of the backsheet, mild improvements in the water vapor transmission rate are unnecessary and may in fact be detrimental as daily or seasonal temperature variations may result in supersaturation, or trapping, of moisture within the encapsulant. Only once a backsheet material with extremely low permeability is used, such as glass, will the moisture profile be further enhanced. In this case however, moisture entering from the sides of the laminate will dominate, and the properties of the edge seal will dictate the moisture content in the encapsulant[135]. The use of glass-to-glass packages with edge seals, as is dominantly used for thin-film PV technologies, may be the route to c-Si module lifetimes in excess of 30 years.

Additional properties of the encapsulant should also be considered, as other reactive species, besides water vapor and oxygen, may be present within the module. Acetic acid is a well-known by-product of hydrolysis within EVA [131, 139], and will act as a catalyst in the corrosion of the cell metallization and metallic interconnects. Acetic acid formation occurs in the presence of moisture, heat and UV. As mentioned previously, the moisture content is generally low on the front of the cell where the majority of UV radiation is present. In addition, typical EVA formulations contain UV blockers. Both of these factors have significantly impeded acetic acid production and subsequent corrosion. It was also generally believed that the "breathable" nature of the backsheet allowed for removal of any acetic acid that was produced [139]. Recent studies have shown that as UV blockers degrade, the amount of acetic acid significantly increases [140]. The same study has shown that the diffusion coefficients of acetic acid in EVA are orders of magnitudes lower than for water vapor and oxygen. This has brought into question the validity of whether acetic acid can actually diffuse out of the module packaging. Although more research is required, the use of encapsulants that do not form acetic acid, such as PO or ionomer encapsulants, may lead to improved module reliability in the long-term.

4.2.6   Influence of Encapsulation on Potential Induced Degradation

The module encapsulation has a significant influence on the occurrence of potential induced degradation (PID) in c-Si PV modules [141]. High system voltages, resulting from serial connection of modules into strings, leads to a potential difference between the cell circuitry and the module frame. The potential difference drives current from the active components through the encapsulation to the grounded frame. This leakage current varies in response to the ambient conditions, including the module temperature and relative humidity, as the resistivity of the corresponding materials vary with temperature and absorbed moisture [142, 143]. Under wet conditions such as rain or dew formation, the leakage current increases significantly due to a reduction in the surface resistivity of the glass and a change in the potential field distribution in the module [144]. This leakage current consists of two components, an electronic current and an ionic current.

Ions, typically sodium ions originating from the soda-lime glass, are driven into the module and accumulate on the cell surface and within the cell. The observed electrical performance loss has been attributed to the presence of these ions within the cell [145]. The reader is referred to Part II of this work in which a detailed discussion of the mechanisms driving cell degradation is presented. The remaining discussion will focus on the influence of the encapsulation on the ionic transport within the packaging.

Standard safety and performance qualification requires that PV modules maintain adequate insulation resistance in both dry and wet conditions. However, when considering a module containing cells that are prone to PID, the encapsulation must adequately prevent ions, specifically sodium ions, from migrating to the cell surface in the presence of an electric field. This can be achieved by multiple methods. The first option is to eliminate the source of the sodium ions (i.e. the soda-lime front glass). This can either be accomplished through chemical treatment or by replacement with borosilicate glass, or other low-sodium containing glasses. Secondly, the encapsulant can be replaced with a high resistivity material that will reduce the overall leakage current and prevent ions from reaching the cell surface. Examples include ionomer or PO encapsulants. Recent work by Kapur *et al.* has demonstrated that incorporation of a thin-ionomer layer, between the glass and EVA, may be sufficient to prevent sodium ions from reaching the cell [146]. Lastly, surface treatment of the glass on the front side may be effective in reducing the effect of rain or condensation from significantly increasing the module leakage currents. This method may only have limited impact depending on the operation environment (e.g. desert climates), and may not completely prevent ion mobility during dry conditions.

4.3   Emerging Technologies

As the focus of the PV industry changes from reducing production costs (i.e. $/W) to reducing the cost of energy produced (i.e. $/kWh), an emphasis will be placed on developing a package that can withstand many years in the field. It is important to note that typical module constructions including fluoropolymer backsheets, EVA encapsulants, and low-iron soda-lime front glass have been effective in achieving module lifetimes in excess of 30 years [90]. In spite of the advances in EVA formulations over the years, EVA does continue to have properties that make it non-ideal, including variable mechanical properties with respect to temperature, relatively low resistivity, and the potential for acetic acid production. It

has, however, remained the most economical choice for manufacturers and continues to provide adequate performance.

If the goal is to reach beyond 30 years, newer packaging schemes may be required. This may incorporate encapsulants that exhibit superior mechanical properties, higher electrical resistivity, and lower water vapor transmission and diffusion rates such as ionomer or PO based encapsulants. Other studies have shown that a methodically matching of the backsheet and encapsulant based on their chemical properties can result in effective economical solutions [132]. The best approach may even be to employ a nearly hermetic seal that is provided by glass-to-glass packages and appropriate edge seals. Although higher up front cost are often required for superior packaging schemes, the value gained in energy production over the operational lifetime will general exceed the initial investment.

In addition to improving the encapsulation properties for typical screen printed c-Si solar cells, newer device architectures, such as back contact solar cells or advanced metallization schemes, may pose new challenges that must be met by the module-packaging scheme.

4.4   Relevant Metrology Techniques

Qualification of materials prior to incorporation into the module manufacturing line is essential to ensure reliability of the final product. Several techniques are available to quantify various properties of the encapsulation materials. This includes methods for independent materials characterization as well as characterization of the materials when laminated together within a test specimen or complete module. This section will review the various techniques available for examining in-coming raw materials, examining materials after lamination, and for failure analysis or degradation studies.

4.4.1   Chemical Characterization Techniques

Thermal analysis through differential scanning calorimetry (DSC) and thermal gravimetric analysis (TGA) are typical baseline measurements performed on encapsulant materials to identify characteristic temperatures associated with glass transitions, crystal melting transitions and curing/cross-linking [147-152]. For EVA, and similar encapsulants, the level of cross-linking may be important for determining the effectiveness of a particular lamination process. Some studies have suggested however, that the cross-link density may be unimportant as the encapsulant will crosslink when deployed [129]. Along with DSC several additional techniques are available to quantify the cross-link density or level of curing. These include gel content test using the solvent extraction method [149, 153-156], size exclusion chromatography with multi angle laser light scattering [129], viscometric detection, or rheological measurements [155, 157]. Generally, these methods are destructive in nature or involve specialized sample preparation that may only be useful for qualifying a potential encapsulant material or lamination process prior to incorporation into the module manufacturing line. Non-destructive techniques, which may be suitable for in-line evaluation of curing, include ultrasound monitoring [157] or optical transmission methods [154]. Other relevant analysis techniques for encapsulants include X-ray diffraction for evaluation of crystallinity [122] and the determination of water vapor transmission rate and moisture diffusion coefficient [89, 132].

During aging studies, several characterization techniques can be utilized to identify chemical changes within the material to provide insight into the specific degradation mechanisms at work. The chemical structure of the encapsulation materials including the encapsulant and backsheet can be determined through Fourier transform infrared spectroscopy [155, 158-161]. Moisture ingress is often a crucial parameter to monitor to assess module degradation, and can be quantified though the use of Raman Spectroscopy [162-165], as well as through optical transmission/reflectance measurements [166]. As discussed in Section 4.2.5, the formation of acetic acid is known to lead to corrosion within the module. Typically destructive methods such as ion chromatography are used to quantify the amount of acetic acid within the encapsulant [122, 140, 160]. Asaka *et al.* have recently proposed a method in which a pH-sensitive fluorescent dye is introduced within the encapsulant so that fluorescent spectroscopy could be used to determine the acid content non-destructively [167]. Fluorescent spectroscopy has also been used to identify the formation of luminescent fluorophores, which may be linked to the chromophore formation that results in EVA yellowing [100, 105, 168]. Once visual discoloration has occurred, a color index is used to quantify the level of browning or yellowing [103].

4.4.2 Electrical Characterization Techniques

Electronic properties of individual materials, such as volume resistivity and dielectric strength, can be measured using test specimens with known dimensions and standard electrical measurement equipment. Close attention should be given to the environmental conditions, including temperature and humidity, as these factors are known to affect the results.

Measurements of insulation resistance can be performed on modules following the lamination process. Insulation resistance is a measure of how well the module packaging insulates the active internal components of the PV module and is used as pass/fail criteria within the standard qualification testing sequence for crystalline silicon PV Modules (IEC 61215). Test conditions including the polarity, applied voltage, duration and external ambient conditions (i.e. temperature and relative humidity) can affect the measured value of insulation resistance [169]. Additional variations to this test include wet insulation resistance and surface grounding with aluminum foil in order to expose flaws such as water penetration or weak insulation. Long term insulation resistance testing, or high voltage bias testing, in controlled environmental chambers or outdoors, has also been used as a tool to identify module susceptibility to PID [39].

4.4.3 Mechanical Characterization Techniques

When investigating the use of a specific encapsulation or packaging material, the mechanical properties of the individual material, both initially and after aging, must be considered. Dynamic Mechanical Analysis (DMA) can be used to extract parameters such as the storage modulus and viscosity [147, 149, 170, 171]. A nanoindenter or durometer allows for a measurement of hardness [122, 156, 158]. Stress-strain characteristics and subsequent determination of tensile strength, elastic modulus, and elongation can be extracted with the use of a mechanical tension tester, or pull tester [134, 149, 158, 172, 173]. Additional measurements for glass specimens are also available. This includes four point bending method to measure the fracture strength and grazing angle surface polarimetry to measure surface stress in the glass.

Once encapsulation materials are incorporated into the module, additional quantitative information about the stress state of the module may be useful to evaluate a particular packaging scheme or lamination process. Severe levels of stress can lead to fracture of the cell or to interconnect damage, which can often be detected using electroluminescence or photoluminescence imaging. These techniques, however, only identify extreme cases of stress. Measurements of laminate thickness or relative distance of the front glass from an arbitrary back plane can be used to gauge the level of strain within the module packaging materials. This analysis has been carried out with a series of measurements using a high precision depth gauge or micrometer across the entire area of the module, or through a non-contact method such as a laser surface geometry scan [174, 175]. These techniques also provide a method to quantify the magnitude of encapsulant displacement, or creep, within a module after aging as shown by Kempe *et al.* [129]. Further characterization of strain or material/component displacement within a module can be carried out utilizing digital image correlation on specially prepared samples, a technique which has been used for interconnect reliability studies [176]. Finally, grazing angle surface polarimetry can also be used as a non-destructive technique to quantify the surface stress in the glass following the lamination process.

A quantitative measurement of the adhesion between the various interfaces within a module is one potential method to estimate the durability of a specific packaging scheme against failure due to delamination. Obtaining accurate and relevant adhesive measurements has however, remained a challenge within the PV community. For new or aged modules, only a few methods are available. These include the peel test and torsional extraction method, both of which are destructive in nature [125, 126, 177, 178]. These methods are generally referred to as qualitative, due to the occurrence of viscoelastic deformation that occurs during the measurement, and can only provide a relative value of engineering adhesion strength. These techniques can provide valuable insight during accelerated aging studies; however, comparative studies between dissimilar materials are often convoluted due to variations in the amount of work done to cause plastic deformation.

Although measurements on actual modules are often preferred, several measurement techniques are available for specially prepared samples that can provide very accurate adhesion results. These techniques include the wedge test, double cantilever beam method, single cantilever beam method, four point bend method, compressive shear tests, lap shear test, and blister tests [179, 180]. An exhaustive literature survey including the details and limitations of each technique is beyond the scope of this paper, however, recent work by Novoa *et al.* should be noted for its potential implication in lifetime predictions [181]. With the use of cantilever based methods and controlled displacement, fracture mechanics was applied in order to extract the debonding energy at interfaces within the backsheet. With the ability to accurately measure extremely low debond/crack growth rates down to 10^{-8} m/s, the results are much more representative of conditions and delamination mechanisms observed during PV module deployment. With additional studies that focus on the impact of environmental stresses on debonding kinetics, it may be possible to model and predict, based on the operating conditions, when delamination will occur within a module for a specific set of encapsulation materials.

4.5   Gap Analysis

The metrology techniques discussed in the previous section allow for qualitative or quantitative analysis of the various properties of the module or individual encapsulation materials. It is important to note that a single test or metrology technique is rarely sufficient to ensure a reliable product. Therefore, there is a need for a comprehensive set of metrology techniques for materials qualification/quality control, process qualification, and in-line process control in order to provide confidence in the durability of the final PV module. Fortunately, several groups are working toward this goal of identifying relevant quality assurance tests and protocols [182, 183].

There is a significant interest within the industry to improve light transmission into the cell in order to increase the short circuit current of the device. One approach to accomplish this is to provide an anti-reflective coating on the front surface of the glass [184]. There is, however, very little literature on the reliability of this coating and how it might impact module performance in the long-term. Additional studies, beyond the initial performance of anti-reflective coated glass, are required to better quantify and predict the long-term reliability of these coating.

Although there are several techniques discussed in Section 4.4.3 used to evaluate interfacial adhesion, there is no consensus on which methodology may provide the most valuable results. The critical parameter required to quantify interfacial delamination is the fracture energy in units of J/m^2. Due to inaccuracies introduced from elastic deformation and geometrical considerations, several methods provide only qualitative results. Additional complications arise when considering the variety of methods used for surface preparation and the need to prepare specialized samples. There is a need for test methodologies that can identify the fracture, or debonding, energy at a particular interface, which could ideally be applied to actual modules. Furthermore, an understanding of the minimum amount of adhesion require for reliable operation is also required.

5.   Integration of Junction Box and Bypass Diode(s)

Crystalline silicon PV modules consist of several cells serially connected within a module. Following the stringing, tabbing, and lamination of these cells into a module configuration, a junction box is attached. The junction box is where string interconnects are converted to module leads and bypass diodes are usually incorporated in the electrical configuration of the module circuitry. Some module designs have incorporated bypass diode within the encapsulation, however this is generally not the standard configuration. General requirements for the junction box are that it must adhere well to the module, provide sufficient electrical insulation from internal components, and prevent the penetration of moisture. Requirements of internal components and materials of the junction box are that they provide sufficient electrical insulation to prevent arcing between leads, withstand relatively high operating temperatures, provide adequate heat dissipation, and remain mechanically secured.

5.1   Junction Box

5.1.1   Background

PV module junction boxes perform the critical functions of connecting the internal cell circuitry to an external cable connector and enclosing the protective bypass diodes. PV module junction boxes are

typically made from Noryl, a polymer blend of ployphenylene oxide and polystyrene, or Xyron, a copolymer of modified polyphenylene ether and polystyrene [185] . The junction box is adhered to the module backsheet using an adhesive foam tape, adhesive polymer, or a hot-melt polymer. The junction box must provide sufficient protection from moisture to avoid corrosion of internal components. A pottant could be used within the junction box, after all electrical connection have been made, to further protect the internal components. For protection of the internal electrical connections from external mechanical stress, UL requires the use of a strain relief for the exiting cables. Breakdown of the basic functions of a PV module junction box will lead to catastrophic failure of the PV module through excessive heating and/or arcing [186] . Due to economic constraints and the ever growing need to reduce manufacturing costs, it is important that the quality and functionality of the junction box is not compromised. Therefore, extensive qualification testing of new junction box designs and internal components is recommended in order to avoid premature failure of PV modules in the field.

5.1.2 Failure Modes

5.1.2.1 Junction box delamination

If the adhesion between the junction box and the backsheet degrades over time, the potential for detachment of the junction box increases. Once the junction box detaches, problems such as electrical shorting, ground faults, or corrosion may occur. It is essential that the junction box remains in place over the service lifetime of the module, which may include extreme weather conditions such as high temperatures, high humidity, rain and snow. Miller *et al.* proposed a potential qualification test, in which weight was applied to the junction box during extended damp heat conditions [185]. It was determined that the materials systems used, including the junction box, adhesive and substrate, must be compatible in order to provide sufficient adhesive strength over time.

5.1.2.2 Arc Fault

Within a PV system, parallel or series type of arc faults are possible. A parallel arc can occur between a point in the PV module array and ground, or between two current carrying components with opposite polarities. A series arc occurs when there is an open circuit in the PV module string. Both situations pose serious safety concerns and create potential fire hazards [187]. Within a junction box, potential for series and parallel type arcing exists. Poor solder joints between busbars and module connector leads, failed bypass diodes, corroded electrical contacts or degraded electrical insulation are all potential mechanisms that may result in open circuit conditions and lead to the occurrence of arcing within the junction box. In order to avoid open circuit conditions, Wohlgemuth recommended designing modules so that multiple failures were required in order for open circuit condition to occur[188]. This includes the use of redundant electrical connections involving multiple solder points or the use of a mechanical support along with the solder joint. Mechanical press fit contacts are known to be less robust than soldered connections and can lead to infant mortality caused by arcing and melting within the junction box [189]. The thermal design of the junction box should also be considered to prevent overheating of electrical insulation, as well as to limit the maximum operating temperature of the bypass diode. This is because both degraded electrical insulation and failed bypass diodes are potential sources of arc faults.

Because bypass diodes also provide protection against series arcing, it is recommended that all bypass diodes be verified as operational prior to leaving the manufacturing facility.

5.2   Bypass Diode

5.2.1   Background

Ideally, a PV module in the field would consist of solar cells generating identical current throughout the entire working lifetime of the module. Practically, however, situations such as electrical mismatching of cells, partial shading, damage, or degradation can lead to conditions where certain cells generate less current than other cells within the module. Not only does this condition lead to a reduction in power output, it can result in the dissipation of power in the form of heat within the under-producing cells. This leads to safety and reliability concerns for the PV system. These local hot-spots, caused by reverse biasing of individual cells, can lead to further damage of the under-producing cells or may induce thermal degradation of other module components and materials. The heat produced from these hot spots can exceed 150 °C and may result in damaged cell interconnects, shunting of solar cell junction and/or degradation of module packaging materials [190]. This condition must be considered in the design of the module to avoid catastrophic failure. Bypass diodes are used to prevent the described scenarios from resulting in irreversible damage to the module. Additionally, bypass diodes provide a limited protection against series arcs by limiting the arcing voltages to 10–20 V [191].

5.2.2   Configuration of Bypass Diodes

During the module interconnection process several cells are connected in series to form individual strings. Each string is individually routed to the junction box to allow for the incorporation of bypass diodes. The module layout determines the number of cells in a string thereby determining the number of cells connected across a single bypass diode. Typically, one diode or two diodes in parallel are used for a single string of cells depending on the rated current of the diodes. In general, bypass diodes are used per every 12 – 24 cells [191]. For example, if a manufacturer included three bypass diodes per module, for a 60 cell module there would be one diode for each string of 20 solar cells and in a 72 cell module there would be one diode for every 24 cells [192, 193]. .

5.2.3   Ideal Diode Electrical Properties

The normal mode of operation for a bypass diode is in the reverse bias condition. In this case it is ideal that the diode has extremely low leakage current as to not affect the performance of the PV module or unnecessarily heat the diode itself. Therefore, the reverse breakdown voltage of the diode is required to be much higher than the voltage of the cell strings. For operating conditions when a module or cell is partially shaded, the diode will be in the forward bias condition. In this condition it is desirable for the power loss to be minimal [194].

Originally, P-N junction diodes were used as bypass diodes. These diodes had reverse breakdown voltages as high as 100 V with very low leakage currents and minimal power dissipation during normal operation. During forward bias conditions P-N junction diodes suffer from high turn on voltages of around 1 V. As the wafer size used for solar cells increased, the short circuit current of the module also

increased, resulting in excessive power dissipation and heating in the P-N junction diodes. Therefore, the PV industry adopted Schottky diodes that exhibit lower turn on voltages and lower power dissipation when forward biased. Schottky diodes, on the other hand, suffer from relatively high leakage currents when reverse biased.

In an event of sudden transition from shaded to unshaded, the diode goes from forward bias to reverse bias. In this case, it is required that the power consumption in the reverse bias be less than the power consumption in forward bias to prevent thermal runaway.

Bypass diodes must also be able to withstand extreme conditions such as overvoltage spikes. These spikes may occur during module assembly caused by electrostatic discharge (ESD), during system installation, or during field operation due to nearby lightning strikes [10].

Finally, if a bypass diode does fail in the field it is ideal that the diode fail in the short circuit rather than open circuit. This condition will reduce the power output from the PV system, but will prevent any further damage to the cells or to the PV system.

5.2.4   Failure Modes

5.2.4.3   Electrostatic Discharge (ESD)

Electrostatic Discharge (ESD) is a phenomenon that occurs when there is a sudden, intense amount of current exchanged between two objects. ESD incidents generally involve a spark that can be seen or heard, with lightning being the most extreme example. There is however, ESD that occurs below human perception, which can be detrimental to sensitive electron components [195]. The environment in which the object is handled determines the extent of ESD. Most ESD sensitive components, including most semiconductor-based electronic devices, are assembled in an environment that is designed to contain ESD within acceptable limits by employing standards such as ESD 20:20 or IEC 61340-5-1. Precautions include grounding of all conductive materials, installing equipment on conductive floor mats, requiring grounded wrist straps for employees, and maintaining higher humidity environments. These precautions are followed in almost all electronics manufacturing facilities.

Within a PV module there are no materials or components, with the exception of the bypass diode, which are sensitive to ESD. This may lead to the easing of well-known ESD precautions within module manufacturing facilities [196]. Individual diodes and complete junction boxes undergo testing, including IEC 61000-4-2 or JESD22-A114D-HBM, to determine susceptibility to ESD according to various models [12]. These qualification tests conclude whether the electronic properties of devices can withstand an ESD event up to a certain voltage. However, latent failures can be induced by ESD events with voltage spikes well below the maximum ESD tolerance limit of the device. These latent failures in bypass diodes could ultimately lead to premature failure of the PV module [197]. Therefore, ESD precautions are recommended within the manufacturing facility so as not to affect the long-term reliability of the diode.

5.2.4.4   Mechanical Damage

During junction box assembly, the electrical leads of the diode may require mechanical manipulation prior to being inserted within the electronic housing, depending on the geometry and configuration. The

method by which each lead is adjusted can have a significant impact on the integrity of the device. Improper bending can lead to mechanical stress on the die [14]. This mechanical stress, along with high temperatures or thermal cycling, can degrade electrical properties of the diodes and lead to field failures.

5.2.4.5   Thermal Runaway

In a semiconductor device, thermal runaway occurs when the current flowing through the device exceeds a certain critical point. At this point the temperature of the device increases excessively, resulting in more available charge carriers and higher currents. These higher currents in turn further heat the device until catastrophic failure occurs due to thermal damage. Within a diode this failure occurs when the rate of power generation exceeds the cooling capabilities of the system [198].

Bypass diodes may experience this behavior in the field when rapidly returning to reverse bias from a high temperature forward bias state. Figure 8 (a) depicts a diode in the reverse bias state within an unshaded module. In a typical bypass diode, the reverse leakage current is negligible and the diode operates at the ambient temperature within the junction box. When the sub-string of cells corresponding to the diode is shaded, the diode becomes forward biased and the current generated by the rest of the sub-strings begins to flow through the diode. This continuously increases the temperature of the diode until thermal equilibrium is reached as represented by Figure 8 (b). When the shading is quickly removed, the diode returns to the reverse bias state, while its temperature remains the elevated as represented in Figure 8 (c). This elevated temperature results in an increase in the reverse leakage current through the diode compared to the original state. If the power dissipation in the diode is greater than the heat dissipation allowed by the thermal design of the diode and junction box, the temperature of the diode increases further. As the temperature increases, the leakage current also increases resulting in thermal runaway behavior that ends in diode failure as represented in Figure 8 (d).
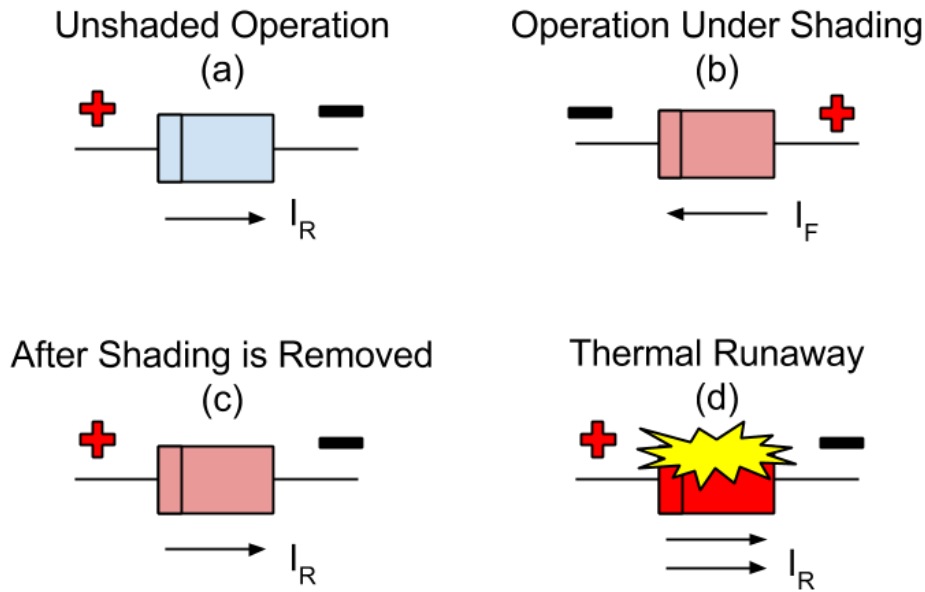
Figure 8. Diagram depicting a thermal runaway event within a bypass diode in sequence (a)-(d). Arrows below each figure represent the direction of current flow within the diode and the number of arrows represents the relative magnitude. The color of the diode represents the relative temperature; blue represents ambient temperature, light red represents elevated temperatures, and dark red represents excessive temperatures.

A test was carried out by Posbic *et al.* in which bypass diodes were forward biased between 12-15 A to heat up the diode to various temperatures up to 150°C [193]. At the given temperature, the devices were reversed biased and the leakage current characteristics were recorded. It was found that for various diode types, excessive leakage currents were observed and generally led to failures in the open circuit condition. A recommendation was provided to include a similar test in the qualification testing of PV module bypass diodes.

The junction box design, including the shape, layout and materials, has a significant effect on the operating temperature of the diodes. Uchida *et al.* determined that for a typical junction box in which three diodes are used, the center diode temperature was affected by the adjacent diodes, resulting in an increased operating temperature [199]. Experiments were carried out within an environmental chamber, in which after application of a forward current, a reverse voltage was applied to the diode. The test was carried out in steps of increased forward current, reverse voltage and environmental chamber temperature to identify at which point thermal runaway and diode failure occurs for various junction box designs. It was determined that the junction box shape and use of potting affected when the failure occurred. Additionally, in all cases the center diode failed earlier than the outer diodes. Recently, a theoretical framework to predict the vulnerability of bypass diodes to thermal runaway based on the parameters derived from the manufacturers datasheet has been proposed [143].

5.2.4.6 Thermal Fatigue

For a module experiencing extended hot-spot conditions in the field, the bypass diode will be continuously in the forward bias condition. This condition may lead to excessive heating beyond the rated junction temperature of the diode. The IEC 61215 bypass diode test requires the diode junction

temperature to be less than the rated maximum junction temperature in controlled operating conditions. TamizhMani *et al.* reported on the temperatures commonly observed during this test, as well as the alarming rate of failures due to excessively high diode junction temperatures [200]. Even for modules that passed this test, the actual diode junction temperature was very close to the rated maximum junction temperature, commonly reaching temperatures between 150 to 200°C. This raises concerns for the long-term reliability of these silicon-based diodes as they experience similar conditions repeatedly in the field, even after passing IEC qualification.

Studies to evaluate the effect of junction box designs on the performance of diodes under extended forward bias conditions were carried out at NREL [201]. Several junction box designs and diodes were used in this testing. Two thermal conditions were applied including long-term high temperatures, and thermal cycling. When these conditions were supplemented with forward biasing of the diode, representing a hot-spot condition, degradation of the diodes was observed for junction boxes with poor heat dissipation. For the high temperature endurance testing no diodes failed, however some diodes experienced increased forward turn-on voltages. Thermal cycling, with an applied forward current, led to the failure of several diodes and increased reverse leakage currents in other diodes. It was seen that the junction box design had a tremendous effect on the results of this testing as at least one junction box type resulted in no degradation of the diodes for each test.

The results of the tests for thermal fatigue and thermal runaway confirm the requirement of a junction box designed to allow for adequate heat dissipation. The location, layout and size of the junction box along with thermal conductance of the materials, including the potting, should all be considered in the design of a PV module junction box.

5.3   Relevant Metrology Techniques

5.3.1   Thermal Characterization Techniques

Forward biased, or activated, bypass diodes operate at relatively high temperatures, and can be identified in fielded modules with the use of an infrared camera [70, 202]. Although it may be difficult to accurately determine the diode operating temperature through simple thermal imaging, this can be used as a tool to identify damaged or underperforming modules.

Identifying the operating temperature of a diode is critical to ensure reliable operation when in the field. The bypass diode test within the IEC 61215 qualification sequence is required to ensure that the maximum operating temperature, evaluated at an ambient of 75°C and a forward current of 1.25 Isc, is less than the rated junction temperature of the bypass diode. There are two methods available to determine the junction temperature of the diode.

The first method is the T_{lead} method. In this method the temperature at the leads of the diode (T_{lead}), the forward current passing through the diode (I_F) and the forward voltage drop across the diode (V_F) is experimentally measured and the junction temperature (T_J) is calculated from following formula:

$$T_J = T_{lead} + R_{th} \times I_F \times V_F$$

36

where $R_{th(J-L)}$ is thermal resistance of the diode from junction to lead, as provided by the manufacturer.

The second method involves extraction of the temperature data from the forward voltage versus junction temperature curve, generally provided on the diode datasheet. This technique requires a measurement of the forward voltage of the diode at a specific current. Typically the forward voltage of the Schottky diodes reduces linearly as the junction temperature is increased. The junction temperature can be extracted from data specifying the junction temperature as a function of forward voltage at a given current, which is often provided by the manufacturer.

It has been reported that the T_{lead} method is prone to errors introduced from variations in thermal resistance of the diode [199]. Some diode manufacturers provide the thermal resistance of diode junction to case, instead of diode junction to lead. Therefore, in this case it would be necessary to attach temperature sensors (e.g. thermocouples) on the diode case to estimate the junction temperature. However, the diode case is made of thermally insulating material, and attaching temperature sensors to case can introduce additional errors. Additionally, the measured junction temperature using T_{lead} method was shown to be less than the temperature measured by V_F-T_J method [199]. Therefore, the V_F-T_J method should be preferred whenever the forward voltage versus junction temperature data is available.

5.3.2   Electrical Characterization Techniques

The current-voltage characteristics of the diode are measured to calculate the important diode parameters such as forward voltage (V_F), forward current (I_F), reverse voltage (V_R) and reverse leakage current (I_R). The reverse breakdown voltage (V_{Br}) is defined as the minimum reverse voltage, V_R at which the diode breaks down. Although this data is often provided on the datasheet provided from the manufacturer, each specific diode will have some deviation from the specified characteristics. It may be beneficial to verify the performance of a representative sample of diodes when evaluating a new diode type or manufacturer.

In a given sample of diodes undergoing accelerated testing, the distribution of V_F, and I_R can be monitored before, during and after the testing in order to study the statistical changes in the diode parameters. These types of experiments can provide information about progression of degradation in diodes.

5.3.3   Techniques for Identification of Failed Bypass Diodes

Diode failure may occur during the diode manufacturing, module assembly, or during fielded operation. Several techniques are available to detect a failed bypass diode.

Prior to leaving the module manufacturing facility, a failed diode can be identified in several ways depending on whether the failure is in the short circuit or open circuit condition. During module quality control, a significant reduction in the power observed in the I-V characteristics, or a dark string of cells observed in electroluminescence imaging can be attributed to a short-circuited bypass diode. A failed diode can also be identified directly by passing a forward current through the diode and measuring the

voltage. A zero or near zero voltage would indicate a short circuit failure while an open circuit would identify an open circuit failure.

In the field, failed diodes can be identified by taking I-V curves of a PV module measured while sequentially shading each string of cells. Open circuit failures will be identified by no power output, while operational bypass diodes will only reduce the power output [18]. Short circuit failures or active diodes will be identified during an unshaded I-V measurement.

A non-contact voltage tester, known as a cell line checker, can also be used to detect open or short circuit failures in bypass diodes in field deployed modules. Short circuit failures in bypass diodes are easy to detect as they typically result in loss of one-third power in commercial 60-cell modules with three bypass diodes. This device can be specifically used for detecting open circuit failures in bypass diodes. The process involves attachment of a transmitter to the module leads and checking the response by scanning the receiver along the module interconnects under conditions of partial shading. When a string of cells inside the module is partially shaded and the diode is working properly, the current is bypassed through the diode. In this scenario the receiver will show no response as it is scanned along the module interconnects of that string. In case of a failed bypass diode in the open circuit condition, the current cannot be bypassed, and the receiver detects current flow through the shaded string.

X-ray imaging is a non-destructive technique that can be utilized to perform root-cause failure analysis on diodes. The transparency of elements to X-rays reduces with increase in atomic mass. Therefore, the silicon die appears transparent while the metallic components within a diode appear opaque in an X-ray image. Figure 9 shows an X-ray image of a diode failed by thermal runaway. In this case it appears, that the high temperature led to metal diffusion inside the silicon die as shown in the inset.
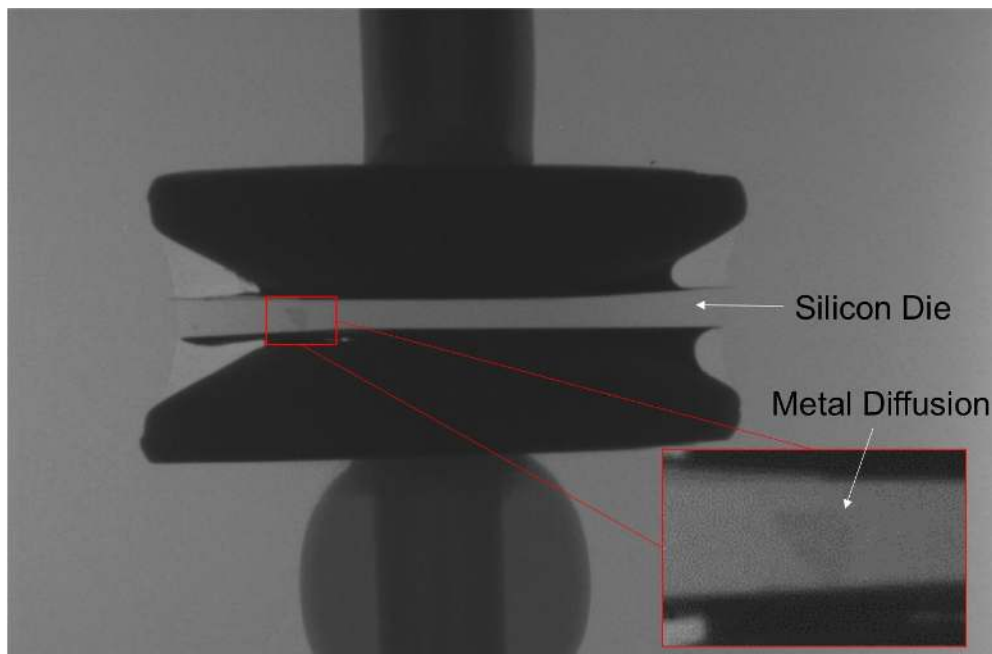
Figure 9. X-ray image of a failed bypass diode highlighting a region in which metal is present within the silicon die.

5.4 Emerging Technologies

When maximum power point tracking (MPPT) is performed at the string level using a string inverter, a single shaded module can significantly reduce the power output of the entire string. There is potential for significant improvement in system energy yield if MPPT is carried out at the module level. Module level power electronics (MLPE) refers to devices such as power optimizers and micro-inverters that carry out MPPT at module level [203]. MLPE devices are becoming more popular due to increased energy yield and system reliability as compared to string inverters. They also provide the added benefits of ease of installation and improved safety. "AC Modules" with integrated power electronics are also being proposed to further reduce the costs and time associated with installation [204]. Smart or active bypass diodes with significantly lower forward voltage drop than Schottky diodes are also being developed [205]. These devices may become more common due to their ability to reduce power loss during events of shading and ease of integration into the module laminate.

The success of MLPE or active bypass diode technologies will depend on their long-term reliability. Currently there is no internationally accepted test standard for reliability testing of MLPE devices and inverters due to large variation in their power rating, operating temperature and other performance specifications. Even if the modules with integrated active bypass diodes pass the IEC 61215 qualification test sequence, there is limited field data available about their long-term performance. Integration of complex power electronics comprising of several components inside the PV module may result in reduced overall reliability of the PV module itself. Wherever the MLPE device is externally attached to the module, in case of failure, the device can be replaced independently. However the replacement of a failed device could be difficult in case of integrated MLPE, and the whole PV module may need to be replaced.

There is a need for the development of test standards that evaluate the long-term reliability testing of MLPE devices. Even before a consensus on the test standard is reached, the reliability of MLPE devices can be improved by replacing the components with known higher failure rates, such as electrolytic capacitors, with components known to have lower failure rates such as ceramic capacitors, film capacitors and inductors, wherever applicable.

5.5 Gap Analysis

In general, characterization and detection of bypass diode failures is often difficult and rarely carried out. Currently, there are no methods to monitor the progress of degradation in the bypass diodes in field-deployed modules. Therefore, only catastrophic failures (e.g. degradation of module packaging materials due to excessive heating) are detected and reported. New techniques are needed to detect latent failures in bypass diodes as well as to efficiently detect problems with bypass diodes in field deployed modules. Qualification of diodes, based on avoiding failures such as thermal runaway, should be implemented to avoid premature failure in the field. Additionally, a test protocol is necessary to ensure the bypass diodes in the modules are working before modules are shipped from the manufacturing facility.

The bypass diode test and other qualification tests, such as ESD test, are designed for reliability testing of the systems, and not individual components. This means, a good diode can fail if enclosed in a

junction box with poor thermal design. It would be useful to have a quantitative measure for the thermal resistance of the junction box so as to rate the junction boxes according to their heat dissipation capabilities. Similarly, a good diode can be rendered useless due to poor electrical connection within a junction box. Testing and qualification is needed for both individual components and integrated systems to ensure adequate reliability.

6. Summary

The operational lifetime of a PV system is a key factor when evaluating the economics of solar energy production. The longer a system operates, the cheaper the overall cost of energy produced. Performance of PV modules reduces over time due to one or more degradation modes. Along with loss of energy generation, certain degradation modes can also pose a significant safety hazard [206]. Operational hazards in photovoltaic system are typically a result of electrical faults due to exposed circuitry, or degradation of materials responsible for electrical isolation. In extreme cases, fires can result from failure of the particular components [187]. The failure modes and degradation mechanisms discussed in this paper can be classified by their impact on the system as either a loss of performance, an operational safety hazard or both.

By understanding the underlying physical and chemical mechanism driving degradation, manufacturers can produce PV modules that last longer and perform better. Each process step has an impact on the long-term reliability and durability of the PV module. Metrology can play a crucial role in validating and maintaining high quality production in regards to both performance and reliability. A summary highlighting the key takeaways from each section is provided below.

6.1 Stringing and Tabbing

Several different failure modes can develop during or as a result of the cell interconnection processes. The failure modes identified are microcrack formation and cell fracture, solder bond failure, ribbon or interconnect failure, and corrosion. Microcracks, which may lead to cell fracture and increased module series resistance, can develop due to stresses caused by differences in coefficient of thermal expansion or applied pressure from soldering. Methods to avoid cell damage during soldering include using a low yield strength ribbon to allow for expansion during cooling and simultaneous stringing and tabbing reducing the thermal stress induced from the two soldering processes. Increased resistance also results from solder bond failure, which can be a result of poor solderability of the cell metallization, incompatible solder metal alloys, inappropriately sized solder joints, or metal diffusion from the solder. Ribbons can fail as a result of thermally-driven stresses, resulting in increased resistance and current crowding. Corrosion, although driven generally by moisture and other contaminants within the laminate, has also been linked to the laminate conductivity and both negative and positive biases during operation.

A number of metrology techniques including methods for individual component as well entire modules have been used to characterize and predict durability issues during the stringing and tabbing process step. Interconnect degradation can be determined through measurements of module series resistance, which can be measured using illuminated or dark I-V curves, a cell line checker tool in the field, or qualitatively through electroluminescence imaging. Electroluminescence imaging has also been used to

identify grid-finger failures, cell fracture, and interconnect failure. Infrared thermography, both steady sate and lock-in, can be used to evaluate hot spots that form due to weak or failed solder bonds resulting in Joule heating of the solder ribbon. Additionally, thermal cycling can be used as a method to stress solder bonds and interconnects, to screen modules for issues related to thermal expansion.

There are also several component level tests that can be used to quantify properties of materials used and determine the quality of solder bonds or interconnects. The peel test can be used to determine the adhesion between the cell interconnect and the silicon substrate. The pull test can be used to determine the maximum stress level before failure. Dynamic mechanical analysis is useful in determining ribbon cycle lifetime. Information about solder bond morphology and microstructure can be obtained through electron microscopy techniques.

6.2   Lamination

Lamination is the process of encapsulating interconnected cells to provide mechanical support, offer protection from environmental stresses, and ensure safe and reliable operation. A typical packaging scheme, or laminate, utilizes a glass front cover, multilayer polymer backsheet, and internal encapsulant such as EVA. Failure of the fundamental functions of the module packaging can lead to safety hazards, degradation of internal components or complete failure of the module. The failure modes identified for the module packaging itself were discoloration, delamination, mechanical failure, and backsheet degradation. The laminate also has a significant influence on degradation mechanisms of the active internal components including potential induced degradation within the cell and corrosion of the cell interconnects, metallic front or rear contacts, and cell antireflection coatings.

Metrology techniques were discussed which focused on methods for extracting properties of raw materials, for understanding materials interactions after lamination, and for failure analysis or aging studies. Methods for extraction of various properties of the encapsulation materials have been identified that include: chemical analysis for determination of critical glass transition temperatures, curing temperatures, level of cross-linking or curing, chemical structure, morphology, impurity content (e.g. moisture, acetic acid), and moisture/oxygen transmission and diffusion rates; mechanical analysis for determination of hardness, storage modulus, elastic modulus, viscosity, tensile strength, fracture strength, glass surface stress, and laminate stress state; electrical analysis for volume resistivity, dielectric strength, and module insulation resistance; and finally interfacial adhesion analysis through various adhesive strength measurement techniques. There is a wide range of techniques available, however a comprehensive series of tests or thorough quality assurance protocol is required to ensure materials and lamination processes being used will provide adequate performance over the operational life-time of the module. There are several groups working to identify the key metrics required to evaluate potential materials or processing conditions prior to incorporation into the lamination step of the module manufacturing line.

6.3   Junction Box and Bypass Diode

Breakdown of the basic functionality of the module junction box and protective bypass diodes can have a significant impact on the reliability and durability of the PV module. Junction box delamination can result in electrical shorting, ground faults, or corrosion. Series arcing within the junction box is also a

potential result when there is an open circuit condition between two nearby points. This can be caused by poor solder joints between string interconnects or module connector leads, failure of bypass diodes, corrosion of electrical contacts, or degradation of electrical insulation. There are a number of mechanisms that result in bypass diode failure, which include electrostatic discharge (ESD), thermal runaway, and thermal fatigue. Bypass diodes are sensitive to ESD, which can occur within a module manufacturing facility and lead to premature failure of a PV module if proper ESD precautions are not taken. The properties of the diode must also be considered, including the current-voltage characteristics and junction operating temperature, to avoid thermal runaway when the diode rapidly returns to reverse bias from a high temperature forward bias state and to avoid thermal fatigue if extended hot-spot conditions occur in the field. In the field, the operating condition of bypass diodes can be identified (including identification of failed diodes), through the use of infrared thermography, module current-voltage measurements, or with a non-contact voltage tester (i.e. diode checker).

Until only recently, reports on the field performance and reliability of bypass diodes have been missing from the literature. Several techniques have been discussed that allow one to monitor the functionality of bypass diodes in order to prevent catastrophic failure of the module through overheating or arcing. Additionally, new techniques to monitor the performance of bypass diodes in the field, prior to failure, need to be developed. There is also a need to qualify the use of diodes based on their resistance to failure as well as their compatibility with the junction box system and module electrical characteristics. In general, testing of individual components and materials along with evaluation of the entire system is essential to ensure reliable performance of c-Si PV modules.

7.   Conclusion

This article provided an overview of the processing steps involved in manufacturing c-Si PV modules, which included stringing and tabbing, lamination, and junction box and bypass diode(s) integration. The key aspects of processing were discussed with a focus on identifying the issues impacting module reliability and durability. Fundamental failure modes and mechanisms resulting from each step in the module fabrication process were discussed and relevant metrology techniques were identified. A comprehensive summary of metrology techniques is provided in Table 1 to help guide the reader to relevant literature for a particular application.

The goal of module manufacturing is to incorporate finished c-Si solar cells into a functional package that allows for rapid deployment and reliable operation. Each processing step and material used during this process can impact the reliability and durability of the final product. Adequate quality assurance programs must be implemented by manufacturers to qualify incoming materials, qualify process equipment and procedures, and provide feedback for process control. This will involve the use of metrology for characterization of individual materials or components and evaluating their interactions. This article identifies a variety of relevant metrology techniques that can be utilized for these purposes with the ultimate goal of improving confidence in module reliability and durability.

The literature contains a wide range of in-depth studies and investigations regarding module manufacturing and reliability and is a valuable resource for module manufacturers. The need to condense this vast array of literature into a readily accessible and functional form was identified and

fulfilled with this article. In addition to the literature survey of c-Si module manufacturing process steps, failure modes, and metrology techniques, new and emerging technologies were discussed and areas of further research were identified.

8. Acknowledgments

Table 1. Relevant Metrology Techniques for Module Manufacturing

Application	Parameter	Technique(s)
Solder-bond resistance	Series Resistance	I-V measurements[61, 62]
	Hot-spot detection	Infrared imaging[69, 71]
	Spatially resolved current distribution within a cell	Electroluminescence Imaging[72, 74-76, 207]
Solder-bond contact adhesion/stress-state	Displacement due to thermal expansion	Digital image correlation[35]
	Interfacial adhesion	Pull test[78]
	Interface morphology	Scanning electron microscopy[66, 67]
	Interconnect failure	Non-contact voltage testing[64, 65]
		Electroluminescence Imaging[72, 74-76, 207]
Mechanical properties of encapsulation materials	Hardness	Nanoindenter
		Durometer[122, 156, 158]
	Storage modulus	Dynamic mechanical analysis[12, 147, 149, 161, 170, 171]
	Viscosity	
	Tensile strength	Stress-strain measurements[112, 149, 158, 172, 173]
	Elastic modulus	
	Fracture strength (glass only)	Four-point bending method
	Surface stress (glass or laminate only)	Grazing angle surface polarimetry
Module/laminate stress state	Laminate thickness	Micrometer measurements[174, 175]

	Laminate bow or bending	Depth measurements[129]
		Surface geometry scan[175]
	Component/materials displacement	Digital image correlation[176]
		Electroluminescence or photoluminescence Imaging
Chemical properties of encapsulation materials	Thermal analysis	DSC, DMA, TGA[147-149, 152, 156]
	Cross-linking/curing	Differentiation scanning calorimetry [149]
		Rheological measurements/ dynamic mechanical analysis [147, 149]
		Gel content test using solvent extraction method[147, 149, 153, 154, 156]
		Size exclusion chromatography with multi angle laser light scattering[129]
		Viscometric detection[129]
		Ultrasonic/Acoustic methods[149, 157]
		Optical transmission spectroscopy[154]
	Chemical structure	Fourier transform infrared spectroscopy[122, 158, 160, 166]
		Raman Spectroscopy[162, 164]
	Encapsulant crystallinity	X-ray diffraction[122]
	Moisture permeability	Water vapor transmission rate measurements[94, 133-135, 138]
		Moisture diffusion coefficient measurements [94, 133-135, 138]
Chemical degradation analysis of encapsulants	Moisture ingress	Raman spectroscopy[163, 165]
		Optical transmission/reflectance measurements[166]
	Acetic acid content	Ion chromotography[140, 160]
		Fluorescence spectroscopy of pH-sensitive dye additives[167]
	Discoloration/chemical breakdown of encapsulant	Fluorescent spectroscopy[101, 105, 168]
		Determination of color (yellowing/browning) index[108]
Encapsulation adhesion	Adhesion strength	Peel test[126, 178]
		Torsional extraction method[125, 177]
		Wedge test

		Cantilever methods[179, 181]
		Four point bend method
		Compressive shear test[179, 180]
		Lap-shear tests[179]
		Blister tests
Electrical properties of encapsulation materials	Volume resistivity	Current-Voltage measurements
	Dielectric strength	Partial discharge test
		Capacitance measurements
	Insulation resistance/leakage current	High potential testing (multiple variations)[169]
		Wet high potential testing
		Long-term high voltage biasing[141, 143]
Operational Properties of Bypass Diodes	Performance characteristics	Current-Voltage Measurements
	Thermal characteristics	Diode operating temperature measurements
		Junction box thermal resistance measurements
		Infrared Imaging

9. References

[1] Mirhassani S, Ong HC, Chong WT, Leong KY. Advances and challenges in grid tied photovoltaic systems. Renewable and Sustainable Energy Reviews. 2015;49:121-31.

[2] Manganiello P, Balato M, Vitelli M. A Survey on Mismatching and Aging of PV Modules: The Closed Loop. Industrial Electronics, IEEE Transactions on. 2015;62:7276-86.

[3] Shrestha SM, Mallineni JK, Yedidi KR, Knisely B, Tatapudi S, Kuitche J, et al. Determination of Dominant Failure Modes Using FMECA on the Field Deployed c-Si Modules Under Hot-Dry Desert Climate. Photovoltaics, IEEE Journal of. 2015;5:174-82.

[4] Cristaldi L, Faifer M, Lazzaroni M, Khalil MMAF, Catelani M, Ciani L. Diagnostic architecture: A procedure based on the analysis of the failure causes applied to photovoltaic plants. Measurement. 2015;67:99-107.

[5] Jordan DC, Kurtz SR. Photovoltaic Degradation Rates—an Analytical Review. Prog Photovolt. 2013;21:12-29.

[6] Luque A, Hegedus S, Editors. Handbook of Photovoltaic Science and Engineering, Second Edition: John Wiley & Sons Ltd.; 2011.

[7] Gabor AMR, M.; Montminy, S.; Alegria, L.; Bordonaro, C.; Woods, J.; Felton, L. Soldering Induced Damage to Thin Solar Cells and Detection of Cracked Cells in Modules. 21st European Photovoltaic Solar Energy Conference and Exhibition; Year.21st European Photovoltaic Solar Energy Conference, September 4-8, 2006, Dresden, Germany.

[8] Wohlgemuth JH, Cunningham DW, Placer NV, Kelly GJ, Nguyen AM. The effect of cell thickness on module reliability. 33rd IEEE Photovoltaic Specialists Conference (PVSC); Year:1-4.

[9] Micciche B, Dingle B, Sidelinger S. Understanding the causes for cell breakage during the cell interconnecting process -- Part II. 22nd European Photovoltaic Solar Energy Conference and Exhibition; Year:2531-5.

[10] Cuddalorepatta G, Dasgupta A, Sealing S, Moyer J, Tolliver T, Loman J. Durability of Pb-Free solder connection between copper interconect wire and crystalline silicon solar cells. 10th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronics Systems; Year:1232-9.

[11] Jeong JS, Park N, Han C. Field failure mechanism study of solder interconnection for crystalline silicon photovoltaic module. Microelectron Reliab. 2012;52:2326-30.

[12] Dietrich S, Sander M, Pander M, Ebert M. Interdependency of mechanical failure rate of encapsulated solar cells and module design parameters. SPIE 8472; Year:84720P-P.

[13] Wohlgemuth JH. Reliability of PV Systems. SPIE 7048; Year:704802--13.

[14] Doi T. New Acceleration Test for PV Modules such as Burns or Interconnector Failures. NREL Photovoltaic Module Reliability Workshop; Year.

[15] Wohlgemuth J, Cunningham DW, Nguyen A, Kelly G, Amin D. Failure Modes of Crystalline Si Modules. NREL Photovoltaic Module Reliability Workshop; Year.

[16] Rogelj I, Ziger P, Eiselt P. Production of PV Ribbon for Photovoltaic Solar Panels: Overview of Product Specifications and Comparison of Production Processes. CabWire World Conference; Year.

[17] Pingel S, Zemen Y, Frank O, Geipel T, Berghold J. Mechanical Stability of Solar Cells within Solar Panels. 24th European Photovoltaic Solar Energy Conference and Exhibition; Year:3459-63.

[18] Pavani L, Turner A, Schultz-Whittmann O. Silicon Cracking in Plated c-Si Solar Cells. NREL Photovoltaic Module Reliability Workshop; Year.

[19] Davis KO, Kurtz SR, Jordan DC, Wohlgemuth JH, Sorloaica-Hickman N. Multi-pronged analysis of degradation rates of photovoltaic modules and arrays deployed in Florida. Prog Photovolt. 2013;21:702-12.

[20] DeGraaff D, Lacerda R, Campeau Z. Degradation Mechanisms in Si Module Technologies Observed in the Field; Their Analysis and Statistics. NREL Photovoltaic Module Reliability Workshop; Year.

[21] Quintana MA, King DL, McMahon TJ, Osterwald CR. Commonly observed degradation in field-aged photovoltaic modules. 29th IEEE Photovoltaic Specialists Conference (PVSC); Year:1436-9.

[22] Quintana MA, King DL, Hosking FM, Kratochvil JA, Johnson RW, Hansen BR, et al. Diagnostic analysis of silicon photovoltaic modules after 20-year field exposure. 28th IEEE Photovoltaic Specialists Conference (PVSC); Year:1420-3.

[23] Moyer J, Zhang W, Kurtz E, Tavares R, Buzby D, Kleinbach S. The Role of Silver Contact Paste on Reliable Connectivity Systems. 25th European Photovoltaic Solar Energy Converence and Exhibition/ 5th World Conference on Photovolatic Energy Conversion; Year:2624-30.

[24] King DL, Quintana MA, Kratochvil JA, Ellibee DE, Hansen BR. Photovoltaic module performance and durability following long-term field exposure. Prog Photovolt. 2000;8:241-56.

[25] Jahn U. PV Module Reliability Issues Including Testing and Certification. IEA PVPS Workshop at 27th EUPVSEC: Characterizing and Classifying Failures of PV Modules; Year.

[26] Vasilis Fthenakis RG. Lead-free Solder Technology Transfer from ASE Americas. Vali: PV Performance, Reliability and Standards Workshop; 1999.

[27] University W. Soldering Tips & Lifetime Issues "Coping with lead free". 2007.

[28] Gayatri Cuddalorepatta AD, Scott Sealing, Jerome Moyer, Todd Tolliver,James Loman. Durability of Pb-Free Solder Connection between Copper Interconnect Wire and Crystalline Silicon Solar Cells-Experimental Approach. 11th International Symposium on Advanced Packaging Materials: Processes, Properties and Interface; Year:16-21.

[29] Hongtao M, Suhling JC, Lall P, Bozack MJ. Reliability of the Aging Lead Free Solder Joint. 56th IEEE Electronic Components and Technology Conference; Year:16.

[30] Hsin-Hsin Hsieh F-ML, Fang-Yao Yeh,Mei-Hsiu Lin. The effects of temperature and solders on the wettability between ribbon and solar cell. Sol Energy Mater Sol Cells. 2009;93:864–8.

[31] Hsin-Hsin Hsieh F-M, Shan-PuYu. Performance of low series-resistance interconnections on the polycrystalline solar cells. Sol Energy Mater Sol Cells. 2011;95:39–44.

[32] Cuddalorepatta G, Dasgupta A, Sealing S, Moyer J, Tolliver T, Loman J. Durability of Pb-free solder between copper interconnect and silicon in photovoltaic cells. Prog Photovolt. 2010;18:168-82.

[33] Meier R, Kraemer F, Wiese S, Wolter K, Bagdahn J. Reliability of copper-ribbons in photovoltaic modules under thermo-mechanical loading. 35th IEEE Photovoltaic Specialists Conference (PVSC); Year:001283-8.

[34] Bosco N. Modeling Metal Fatigue as a Key Step in PV Module Life Time Prediction. NREL Photovoltaic Module Reliability Workshop; Year.

[35] Meier R, Kraemer F, Schindler S, Wiese S, Bagdahn J. Thermal and Mechanical Induced Loading on Cell Interconnectors in Crystalline Photovoltaic Modules. 25th European Photovoltaic Solar Energy Conference and Exhibition/ 5th World Conference on Photovoltaic Conversion; Year:3740-4.

[36] Tamizh-Mani G, Kuitche JM. Failure and Degradation modes of PV modules in a hot dry climate: results after 12-26 years of field exposure. NREL Photovolatic Module Reliability Workshop; Year.

[37] Shimizu S, Arai T, Sagawa T, Aoki Y, Hirakawa T, Hiraike H, et al. Failure Assessments for Outside-Exposed Photovoltaic Modules. Jpn J Appl Phys. 2012;51:10NF04.

[38] Hacke P, Kempe M, Terwilliger K, Glick S, Call N, Johnston S, et al. Characterization of Multicrystalline Silicon Modules with System Bias Voltage Applied in Damp Heat. 25th Eurpoean Photovoltaic Solar Energy Conference and Exhibition; Year:3760-5.

[39] Hacke P, Terwilliger K, Glick S, Trudell D, Bosco N, Johnston S, et al. Test-to-Failure of crystalline silicon modules. 35th IEEE Photovoltaic Specialists Conference (PVSC); Year:000244-50.

[40] Kuitche JM, Tamizh-Mani G, Pan R. Failure modes effects and criticality analysis (FMECA) approach to the crystalline silicon photovoltaic module reliability assessment. SPIE 8112; Year:81120L.

[41] Zarmai MT, Ekere NN, Oduoza CF, Amalu EH. A review of interconnection technologies for improved crystalline silicon solar cell photovoltaic module assembly. Appl Energy. 2015;154:173-82.

[42] Schulte-Huxel H, Blankemeyer S, Steckenreiter V, Kajari-Schroeder S, Brendel R. Laser-welded Interconnection of Screen-printed Si Solar Cells. Energy Procedia. 2014;55:356-60.

[43] Schulte-Huxel H, Blankemeyer S, Bock R, Merkle A, Kajari-Schroder S, Brendel R. Aging behaviour of laser welded Al-interconnections in crystalline silicon modules. Sol Energy Mater Sol Cells. 2012;106:22-6.

[44] De Wolf S, Descoeudres A, Holman Z, Ballif C. High-efficiency Silicon Heterojunction Solar Cells: A Review. Green. 2012;2:7-24.

[45] Xu T, Valentin O, Luechinger C. Reliable Tabbing Process for Si Thin-Film Solar Cells Using Ultrasonic Bonding. 25th European Photovoltaic Solar Energy Conference and Exhibition/ 5th World Conference on Photovoltaic Energy Conversion; Year:3292-8.

[46] Zemen Y, Schulz SC, Trommler H, Buschhorn ST, Bauhofer W, Schulte K. Comparison of new conductive adhesives based on silver and carbon nanotubes for solar cells interconnection. Sol Energy Mater Sol Cells. 2013;109:155-9.

[47] Halm A, Loescher M, Theobald J, Lemp E, Hering P, Popescu L, et al. Eco-friendly minimodules made of n-type aluminum rear emitter solar cells. Energy Procedia. 2011;8:409-14.

[48] Schwertheim S, Scherff M, Mueller T, Fahrner WR, Neitzert HC. Lead-free electrical conductive adhesives for solar cell interconnectors. 33rd IEEE Photovoltaic Specialists Conference (PVSC); Year:1-6.

[49] Dziedzic A, Graczyk I. Lead-free solders and isotropically conductive adhesives in assembling of silicon solar cells - preliminary results. 26th International Spring Seminar on Electronics Technology: Integrated Management of Electronic Materials Production Year:127-32.

[50] Sameshima T, Takenezawa J, Hasumi M, Koida T, Kaneko T, Karasawa M, et al. Multi junction solar cells stacked with transparent and conductive adhesive. Jpn J Appl Phys. 2011;50:052301-4.

[51] Beaucarne G, Kuzma-Filipek I, Campeol F, Young X, Wei J, Yu Y, et al. Innovative Cell Interconnection Based on Ribbon Bonding of Busbar-less Cells Using Silicone-based Electrically Conductive Adhesives. Energy Procedia. 2015;67:185-93.

[52] Eitner U, Geipel T, Holtschke SN, Tranitz M. Characterization of electrically conductive adhesives. Energy Procedia. 2012;27:676-9.

[53] Beaucarne G, Schubert G, Hoornstra J. Summary of the 5th Workshop on Metallization for Crystalline Silicon Solar Cells. Energy Procedia. 2015;67:2-12.

[54] Beaucarne G, Schubert G, Hoornstra J, Horzel J, Glunz SW. Summary of the Third Workshop on Metallization for Crystalline Silicon Solar Cells. Energy Procedia. 2012;21:2-13.

[55] Wood D, Kuzma-Filipek I, Russell R, Duerinckx F, Powell N, Zambova A, et al. Passivated Busbars from Screen-printed Low-temperature Copper Paste. Energy Procedia. 2014;55:724-32.

[56] Letize A, Cullen D, Lee B, Crouse K, Bay N, Horzel J, et al. Pilot Scale Production and Reliability Testing of Solar Cell Modules Based on a Low Cost Copper Electroplating Process. 29th European Photovoltaic Solar Energy Conference and Exhibition; Year:1359 - 62.

[57] Kraft A, Wolf C, Lorenz A, Bartsch J, Glatthaar M, Glunz SW. Long Term Stability Analysis of Copper Front Side Metallization for Silicon Solar Cells. Energy Procedia. 2014;55:478-85.

[58] Walter J, Tranitz M, Volk M, Ebert C, Eitner U. Multi-wire Interconnection of Busbar-free Solar Cells. Energy Procedia. 2014;55:380-8.

[59] Papet P, Andreetta L, Lachenal D, Wahli G, Meixenberger J, Legradic B, et al. New Cell Metallization Patterns for Heterojunction Solar Cells Interconnected by the Smart Wire Connection Technology. Energy Procedia. 2015;67:203-9.

[60] Schubert G, Beaucarne G, Hoornstra J. The Future of Metallization – Forecast of the Experts of the 5th Metallization Workshop. Energy Procedia. 2015;67:13-9.

[61] Pysch D, Mette A, Glunz SW. A review and comparison of different methods to determine the series resistance of solar cells. Sol Energy Mater Sol Cells. 2007;91:1698-706.

[62] Bowden S, Rohatgi A. Rapid and accurate determination of series resistance and fill factor losses in industrial silicon solar cells. 17th European Photovoltaic Solar Energy Conference and Exhibition; Year.

[63] Crozier JL, van Dyk EE, Vorster FJ. Characterization of cell mismatch in a multi-crystalline silicon photovoltaic module. Phys B: Condens Matter. 2012;407:1578-81.

[64] Kato K. PV Module Failures Observed in the Field - solder bond and bipass diode failures. IEA PVPS Workshop at 27th EUPVSEC: Characterizing and Classifying Failures of PV Modules; Year.

[65] Dhere NG, Shiradkar NS, Schneller E. Cell Line Checker Correlated to Infrared Thermography. Infrared Thermography Workshop at Intersolar North America; Year.

[66] Schmitt P, Eberlein D, Voos P, Tranitz M, Wirth H. Metallographic Preparation of Solar Cell Samples for Quality Assurance and Material Evaluation. Energy Procedia. 2011;8:402-8.

[67] Schmitt P, Kaiser P, Savio C, Tranitz M, Eitner U. Intermetallic Phase Growth and Reliability of Sn-Ag-Soldered Solar Cell Joints. Energy Procedia. 2012;27:664-9.

[68] Kaplani E. Detection of Degradation Effects in Field-Aged c-Si Solar Cells through IR Thermography and Digital Image Processing. Int J Photoenergy. 2012;2012:1-11.

[69] Cunningham DW. Analysis of Hot Spots in Crystalline Silicon Modules and their Impact on Roof Structures. NREL Photovoltaic Module Reliability Worshop; Year.

[70] King DL, Kratochvil JA, Quintana MA, McMahon TJ. Applications for infrared imaging equipment in photovoltaic cell, module, and system testing. 28th IEEE Photovoltaic Specialists Conference (PVSC); Year:1487-90.

[71] García M, Marroyo L, Lorenzo E, Marcos J, Pérez M. Observed degradation in photovoltaic plants affected by hot-spots. Prog Photovolt. 2014;22:1292-301.

[72] Gazuz V, Buerhop C. Electroluminescence Imaging for Detection of Power Losses in Solder Contacts between Busbar and Interconnect in Solar Cells. 25th European Photovoltaic Solar Energy Conference and Exhibition / 5th World Conference on Photovoltaic Energy Conversion; Year:4219-22.

[73] Chaturvedi P, Hoex B, Walsh TM. Broken metal fingers in silicon wafer solar cells and PV modules. Sol Energy Mater Sol Cells. 2013;108:78-81.

[74] Gazuz V, Buerhop C. Detection of power losses in busbar solder contacts by electroluminescence imaging of solar cells. Meas Sci Tech. 2011;22:115702.

[75] Walter J, Eberlein D, Haunschild J, Tranitz M, Eitner U. A Method to Detect Defective Solder Joints by RS-Electroluminescence Imaging. Energy Procedia. 2012;27:652-7.

[76] Kajari-Schröder S, Kunze I, Eitner U, Köntges M. Spatial and orientational distribution of cracks in crystalline photovoltaic modules generated by mechanical load tests. Sol Energy Mater Sol Cells. 2011;95:3054-9.

[77] Wendt J, Traeger M, Klengel R, Petzold M, Schade D, Sykes R. Improved quality test method for solder ribbon interconnects on silicon solar cells. 12th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems; Year:1023-6.

[78] Lathrop R, Pfluke K. Novel approaches to benchmarking solar cell tabbing solderability. 26th European Photovoltaic Solar Energy Conference and Exposition; Year:1403-8.

[79] Wohlgemuth JH, Conway M, Meakin DH. Reliability and performance testing of photovoltaic modules. 28th IEEE Photovoltaic Specialists Conference (PVSC); Year:1483-6.

[80] Aoki Y, Okamoto M, Masuda A, Doi T, Tanahashi T. Early Failure Detection of Interconnection with Rapid Thermal Cycling in Photovoltaic Modules. Jpn J Appl Phys. 2012;51:10NF3.

[81] Tanahashi T. Accelerated TC Test. NREL Photovoltaic Module Reliability Workshop; Year.

[82] Paggi M, Berardone I, Infuso A, Corrado M. Fatigue degradation and electric recovery in Silicon solar cells embedded in photovoltaic modules. Scientific Reports. 2014;4:1-7.

[83] Park N, Jeong J, Han C. Estimation of the degradation rate of multi-crystalline silicon photovoltaic module under thermal cycling stress. Microelectron Reliab. 2014;54:1562-6.

[84] Heimann M, Bakowskie R, Köhler M, Hirsch J, Junghänel M, Hussack A, et al. Investigations of Different Soldering Failure Modes and their Impact on Module Reliability. Energy Procedia. 2014;55:456-63.

[85] Itoh U, Yoshida M, Tokuhisa H, Takeuchi K, Takemura Y. Solder Joint Failure Modes in the Conventional Crystalline Si Module. Energy Procedia. 2014;55:464-8.

[86] Coyle DJ, Blaydes HA, Northey RS, Pickett JE, Nagarkar KR, Zhao R-A, et al. Life prediction for CIGS solar modules part 2: degradation kinetics, accelerated testing, and encapsulant effects. Prog Photovolt. 2013;21:173-86.

[87] Barber GD, Jorgensen GJ, Terwilliger K, Glick SH, Pern J, McMahon TJ. New barrier coating materials for PV module backsheets. 29th IEEE Photovoltaic Specialists Conference (PVSC); Year:1541-4.

[88] Oreski G, Wallner GM. Delamination behaviour of multi-layer films for PV encapsulation. Sol Energy Mater Sol Cells. 2005;89:139-51.

[89] Jorgensen GJ, Terwilliger KM, DelCueto JA, Glick SH, Kempe MD, Pankow JW, et al. Moisture transport, adhesion, and corrosion protection of PV module packaging materials. Sol Energy Mater Sol Cells. 2006;90:2739-75.

[90] Skoczek A, Sample T, Dunlop ED. The results of performance measurements of field-aged crystalline silicon photovoltaic modules. Prog Photovolt. 2009;17:227-40.

[91] Ross RG. PV Reliability Development Lessons From JPL's Flat Plate Solar Array Project. Photovoltaics, IEEE Journal of. 2014;4:291-8.

[92] DeBergalis M. Fluoropolymer films in the photovoltaic industry. J Flourine Chem. 2004;125:1255-7.

[93] Geretschläger KJ, Wallner GM, Fischer J. Raman and Infrared Microscopical Analysis of Multilayer Backsheets. 27th European Photovoltaic Solar Energy Conference and Exhibition; Year:3499-502.

[94] Hülsmann P, Weiß K-A, Köhl M. Temperature-dependent water vapour and oxygen permeation through different polymeric materials used in photovoltaic-modules. Prog Photovolt. 2014;22:415-21.

[95] Rongbin Y, Guixiong L, Li X, Haikun H, Na W. Failure analysis and permeation modelling of photovoltaic module sealing material in Hot and humid conditions. Materials Research Innovations. 2015;19:S5-1004-S5-8.

[96] Zhang Y, Xu J, Mao J, Tao J, Shen H, Chen Y, et al. Long-term reliability of silicon wafer-based traditional backsheet modules and double glass modules. RSC Advances. 2015;5:65768-74.

[97] Yang J, Lee D, Baek D, Kim D, Nam J, Huh P. Effect of various encapsulants for frameless glass to glass Cu(In,Ga)(Se,S)2 photovoltaic module. RSC Advances. 2015;5:51258-62.

[98] Kraemer F, Wiese S. Assessment of long term reliability of photovoltaic glass–glass modules vs. glass-back sheet modules subjected to temperature cycles by FE-analysis. Microelectron Reliab. 2015;55:716-21.

[99] Cuddihy E, Coulbert C, Gupta A, Liang R. Electricity from photovoltaic solar cells, Flat-Plate Solar Array Project, Final Report.

. JPL Publication 86-31: Jet Propulsion Laboratory, Pasadena, CA; 1986.

[100] Czanderna AW, Pern FJ. Encapsulation of PV modules using ethylene vinyl acetate copolymer as a pottant: A critical review. Sol Energy Mater Sol Cells. 1996;43:101-81.

[101] Pern FJ. Ethylene-vinyl acetate (EVA) encapsulants for photovoltaic modules: Degradation and discoloration mechanisms and formulation modifications for improved photostability. Die Angew Makromol Chem. 1997;252:195-216.

[102] Pern FJ, Glick SH. Photothermal stability of encapsulated Si solar cells and encapsulation materials upon accelerated exposures. Sol Energy Mater Sol Cells. 2000;61:153-88.

[103] Peike C, Purschke L, Weiss KA, Kohl M, Kempe M. Towards the origin of photochemical EVA discoloration. 39th IEEE Photovoltaic Specialists Conference (PVSC); Year:1579-84.

[104] Parretta A, Bombace M, Graditi G, Schioppo R. Optical degradation of long-term, field-aged c-Si photovoltaic modules. Sol Energy Mater Sol Cells. 2005;86:349-64.

[105] Schlothauer J, Jungwirth S, Köhl M, Röder B. Degradation of the encapsulant polymer in outdoor weathered photovoltaic modules: Spatially resolved inspection of EVA ageing by fluorescence and correlation to electroluminescence. Sol Energy Mater Sol Cells. 2012;102:75-85.

[106] Yang S, Whitfiel K, Rhee E. UV degradation study of encapsulate backsheet system for PV module using metal halide lamp. NREL Photovoltaic Module Reliability Workshop; Year.

[107] Knausz M, Oreski G, Eder GC, Voronko Y, Duscher B, Koch T, et al. Degradation of photovoltaic backsheets: Comparison of the aging induced changes on module and component level. J Appl Polym Sci. 2015;132:n/a-n/a.

[108] Gambogi W, Heta Y, Hashimoto K, Kopchick J, Felder T, MacMaster S, et al. A Comparison of Key PV Backsheet and Module Performance from Fielded Module Exposures and Accelerated Tests. IEEE J Photovolt. 2014;4:935-41.

[109] Dechthummarong C, Wiengmoon B, Chenvidhya D, Jivacate C, Kirtikara K. Physical deterioration of encapsulation and electrical insulation properties of PV modules after long-term operation in Thailand. Sol Energy Mater Sol Cells. 2010;94:1437-40.

[110] McMahon W, Birdsall HA, Johnson GR, Camilli CT. Degradation Studies of Polyethylene Terephthalate. J Chem Eng Data. 1959;4:57 - 79.

[111] Steiner AJ, Krumlacher W, Muckenhuber H, Kraxner M. PV Backsheet Materials under Accelerated Aging Conditions: A Performance Study. 27th European Photovoltaic Solar Energy Conference and Exhibition; Year:3526-9.

[112] Kim N, Kang H, Hwang K-J, Han C, Hong WS, Kim D, et al. Study on the degradation of different types of backsheets used in PV module under accelerated conditions. Sol Energy Mater Sol Cells. 2014;120, Part B:543-8.

[113] Li H, Kikuchi R, Kumagai M, Amano T, Tang H, Lin J-M, et al. Nondestructive estimation of strength deterioration in photovoltaic backsheets using a portable near infrared spectrometer. Sol Energy Mater Sol Cells. 2012;101:166-9.

[114] Stollwerck G, Schoeppel W, Graichen A, Jaeger C. Polyolefin Backsheet and New Encapsulant Supress Cell Degradation in the Module. 28th European Photovoltaic Solar Energy Conference and Exhibition; Year:3318-20.

[115] Kempe MD, Wohlgemuth JH. Evaluation of temperature and humidity on PV module component degradation. 39th IEEE Photovoltaic Specialists Conference (PVSC); Year:0120-5.

[116] Lefebvre A, O'Brien G, Fang L, Moeller G. The Effect of Florida and Accelerated Weathering Exposures on Photovoltaic Backsheets. NREL Photovoltaic Module Reliability Workshop; Year.

[117] Lorenzo E, Zilles R, Moretón R, Gómez T, Martínez de Olcoz A. Performance analysis of a 7-kW crystalline silicon generator after 17 years of operation in Madrid. Prog Photovolt. 2014;22:1273-9.

[118] Sánchez-Friera P, Piliougine M, Peláez J, Carretero J, Sidrach de Cardona M. Analysis of degradation mechanisms of crystalline silicon PV modules after 12 years of operation in Southern Europe. Prog Photovolt. 2011;19:658-66.

[119] Voronko Y, Eder GC, Chernev BS, Knausz M, Oreski G, Koch T, et al. Analytical Evaluation of the Ageing Induced Changes of the Adhesive within Photovoltaic Backsheets. 28th European Photovoltaic Solar Energy Conference and Exhibition; Year:3037-42.

[120] Krommenhoek PJ, Lin C-C, Gu X. Cross-Sectional Chemical and Mechanical Characterization of a Multilayer Polymeric Backsheet During UV Exposure. NREL Photovoltaic Module Reliability Workshop; Year.

[121] Munoz MA, Alonso-García MC, Vela N, Chenlo F. Early degradation of silicon PV modules and guaranty conditions. Sol Energy. 2011;85:2264-74.

[122] Matsuda K, Watanabe T, Sakaguchi K, Yoshikawa M, Doi T, Masuda A. Microscopic Degradation Mechanisms in Silicon Photovoltaic Module under Long-Term Environmental Exposure. Jpn J Appl Phys. 2012;51:10NF07.

[123] Park NC, Jeong JS, Kang BJ, Kim DH. The effect of encapsulant discoloration and delamination on the electrical characteristics of photovoltaic module. Microelectron Reliab. 2013;53:1818-22.

[124] van Dyk EE, Chamel JB, Gxasheka AR. Investigation of delamination in an edge-defined film-fed growth photovoltaic module. Sol Energy Mater Sol Cells. 2005;88:403-11.

[125] Dhere NG, Raravikar NR. Adhesional shear strength and surface analysis of a PV module deployed in harsh coastal climate. Sol Energy Mater Sol Cells. 2001;67:363-7.

[126] Wu D, Zhu J, Betts TR, Gottschalg R. Degradation of interfacial adhesion strength within photovoltaic mini-modules during damp-heat exposure. Prog Photovolt. 2014;22:796-809.

[127] Pern FJ, Jorgensen GJ. Enhanced adhesion of EVA laminates to primed glass substrates subjected to damp heat exposure. 31st IEEE Photovoltaic Specialists Conference (PVSC); Year:495-8.

[128] Li H-Y, Perret-Aebi L-E, Chapuis V, Ballif C, Luo Y. The effect of cooling press on the encapsulation properties of crystalline photovoltaic modules: residual stress and adhesion. Prog Photovolt. 2015;23:160-9.

[129] Kempe MD, Miller DC, Wohlgemuth JH, Kurtz SR, Moseley JM, Shah Q, et al. A field evaluation of the potential for creep in thermoplastic encapsulant materials. 38th IEEE Photovoltaic Specialists Conference (PVSC); Year:001871-6.

[130] Mickiewicz R, Li B, Doble DMJ, Christian T, Lloyd J, Stokes A, et al. Effect of Encapsulation Modulus on the Response of PV Modules to Mechanical Stress. 26th European Photovoltaic Solar Energy Conference and Exhibition; Year:3157 - 61.

[131] Kempe MD, Jorgensen GJ, Terwilliger KM, McMahon TJ, Kennedy CE, Borek TT. Ethylene-Vinyl Acetate Potential Problems for Photovoltaic Packaging. 4th IEEE World Conference on Photovoltaic Energy Conversion Year.2:2160-3.

[132] Peike C, Hülsmann P, Blüml M, Schmid P, Weiß K-A, Köhl M. Impact of Permeation Properties and Backsheet-Encapsulant Interactions on the Reliability of PV Modules. ISRN Renew Energy. 2012;2012:1-5.

[133] Kapur J, Norwood JL, Cwalina CD. Determination of moisture ingress rate through photovoltaic encapsulants. 39th IEEE Photovoltaic Specialists Conference (PVSC); Year:3020-3.

[134] Kim N, Han C. Experimental characterization and simulation of water vapor diffusion through various encapsulants used in PV modules. Sol Energy Mater Sol Cells. 2013;116:68-75.

[135] Kempe MD. Modeling of rates of moisture ingress into photovoltaic modules. Sol Energy Mater Sol Cells. 2006;90:2720-38.

[136] Hülsmann P, Heck M, Köhl M. Simulation of Water Vapor Ingress into PV-Modules under Different Climatic Conditions. J Mat. 2013;2013:7.

[137] Wohlgemuth JH, Kempe MD. Equating damp heat testing with field failures of PV modules. 39th IEEE Photovoltaic Specialists Conference (PVSC); Year:0126-31.

[138] Kempe MD, Reese MO, Dameron AA. Evaluation of the sensitivity limits of water vapor transmission rate measurements using electrical calcium test. Rev Sci Instrum. 2013;84:025109.

[139] Kempe MD, Jorgensen GJ, Terwilliger KM, McMahon TJ, Kennedy CE, Borek TT. Acetic acid production and glass transition concerns with ethylene-vinyl acetate used in photovoltaic devices. Sol Energy Mater Sol Cells. 2007;91:315-29.

[140] Weber U, Eiden R, Strubel C, Sögding T, Heiss M, Zachmann P, et al. Acetic Acid Production, Migration and Corrosion Effects in Ethylene-Vinyl-Acetate- (EVA-) Based PV Modules. 27th European Photovoltaic Solar Energy Conference and Exhibition; Year:2992-5.

[141] Hacke P, Smith R, Terwilliger K, Glick S, Jordan D, Johnston S, et al. Testing and Analysis for Lifetime Prediction of Crystalline Silicon PV Modules Undergoing Degradation by System Voltage Stress. IEEE J Photovolt. 2013;3:246-53.

[142] Hoffmann S, Koehl M. Effect of humidity and temperature on the potential-induced degradation. Prog Photovolt. 2014;22:173-9.

[143] Dhere NG, Shiradkar NS, Schneller E. Evolution of Leakage Current Paths in MC-Si PV Modules From Leading Manufacturers Undergoing High-Voltage Bias Testing. IEEE J Photovolt. 2014;4:654-8.

[144] Shiradkar N, Schneller E, Dhere NG. Finite element analysis based model to study the electric field distribution and leakage current in PV modules under high voltage bias. SPIE 8825; Year.8825:88250G-G-9.

[145] Naumann V, Lausch D, Hähnel A, Bauer J, Breitenstein O, Graff A, et al. Explanation of potential-induced degradation of the shunting type by Na decoration of stacking faults in Si solar cells. Sol Energy Mater Sol Cells. 2014;120, Part A:383-9.

[146] Kapur J, Norwood J, Bennett A, Hamzavytehrany B, Stika K, Westphal C, et al. Prevention of Potential Induced Degradation with Ionomer Film. NREL Photovoltaic Module Reliability Workshop; Year.

[147] Stark W, Jaunich M. Investigation of Ethylene/Vinyl Acetate Copolymer (EVA) by thermal analysis DSC and DMA. Polym Test. 2011;30:236-42.

[148] Agroui K, Maallemi A, Boumaour M, Collins G, Salama M. Thermal stability of slow and fast cure EVA encapsulant material for photovoltaic module manufacturing process. Sol Energy Mater Sol Cells. 2006;90:2509-14.

[149] Hirschl C, Biebl–Rydlo M, DeBiasio M, Mühleisen W, Neumaier L, Scherf W, et al. Determining the degree of crosslinking of ethylene vinyl acetate photovoltaic module encapsulants—A comparative study. Sol Energy Mater Sol Cells. 2013;116:203-18.

[150] Polansky R, Pinkerova M, Bartunkova M, Prosr P. Mechanical behavior and thermal stability of EVA encapsulant material used in photovoltaic modules. J Electr Eng. 2013;64:361-5.

[151] Rimez B, Rahier H, Van Assche G, Artoos T, Biesemans M, Van Mele B. The thermal degradation of poly(vinyl acetate) and poly(ethylene-co-vinyl acetate), Part I: Experimental study of the degradation mechanism. Polym Degrad Stab. 2008;93:800-10.

[152] Agroui K, Collins G. Determination of thermal properties of crosslinked EVA encapsulant material in outdoor exposure by TSC and DSC methods. Renew Energy. 2014;63:741-6.

[153] Drabczyk K, Panek P. A comparative study of EVA with and without thermal history for different lamination process parameters. Mat Sci Eng: B. 2012;177:1378-83.

[154] Li H-Y, Perret-Aebi L-E, Théron R, Ballif C, Luo Y, Lange RFM. Optical transmission as a fast and non-destructive tool for determination of ethylene-co-vinyl acetate curing state in photovoltaic modules. Prog Photovolt. 2013;21:187-94.

[155] Rodríguez-Vázquez M, Liauw CM, Allen NS, Edge M, Fontan E. Degradation and stabilisation of poly(ethylene-stat-vinyl acetate): 1 – Spectroscopic and rheological examination of thermal and thermo-oxidative degradation mechanisms. Polym Degrad Stab. 2006;91:154-64.

[156] Khonakdar HA, Jafari SH, Haghighi-Asl A, Wagenknecht U, Häussler L, Reuter U. Thermal and mechanical properties of uncrosslinked and chemically crosslinked polyethylene/ethylene vinyl acetate copolymer blends. J Appl Polym Sci. 2007;103:3261-70.

[157] Stark W, Jaunich M, Bohmeyer W, Lange K. Investigation of the crosslinking behaviour of ethylene vinyl acetate (EVA) for solar cell encapsulation by rheology and ultrasound. Polym Test. 2012;31:904-8.

[158] Shi X-M, Zhang J, Li D-R, Chen S-J. Effect of damp-heat aging on the structures and properties of ethylene-vinyl acetate copolymers with different vinyl acetate contents. J Appl Polym Sci. 2009;112:2358-65.

[159] Allen NS, Edge M, Rodriguez M, Liauw CM, Fontan E. Aspects of the thermal oxidation of ethylene vinyl acetate copolymer. Polym Degrad Stab. 2000;68:363-71.

[160] Wang E, Yang HE, Yen J, Chi S, Wang C. Failure Modes Evaluation of PV Module via Materials Degradation Approach. Energy Procedia. 2013;33:256-64.

[161] Geretschläger KJ, Wallner GM, Fischer J. Spectroscopic, Thermal and (Thermo)Mechanical Analysis of Multilayer Backsheets. 28th European Photovoltaic Solar Energy Conference and Exhibition; Year:3046-9.

[162] Peike C, Kaltenbach T, Weiß KA, Koehl M. Non-destructive degradation analysis of encapsulants in PV modules by Raman Spectroscopy. Sol Energy Mater Sol Cells. 2011;95:1686-93.

[163] Rashtchi S, Ruiz PD, Wildman R, Ashcroft I. Measurement of moisture content in photovoltaic panel encapsulants using spectroscopic optical coherence tomography: a feasibility study. SPIE 8472; Year.8472:84720O-O-9.

[164] Voronko Y, Eder G, Weiss M, Knausz M, Oreski G, Koch T, et al. Long Term Performance of PV Modules: System Optimization through the Application of Innovative Non-Destructive Characterization Methods. 27th European Photovoltaic Solar Energy Conference and Exhibition; Year:3530-5.

[165] Peike C, Hoffmann S, Heck M, Kaltenbach T, Weiß KA, Köhl M. Nondestructive Determination of Climate-Specific Degradation Patterns for Photovoltaic-Module Encapsulation. Energy Technol. 2014;2:121-9.

[166] Kapur J, Proost K, Smith CA. Determination of moisture ingress through various encapsulants in glass/glass laminates. 34th IEEE Photovoltaic Specialists Conference (PVSC); Year:001210-4.

[167] Asaka T, Iwami K, Taguchi A, Umeda N, Masuda A. Detection of acid moisture in photovoltaic modules using a dual wavelength pH-sensitive fluorescent dye. Jpn J Appl Phys. 2014;53:04ER18.

[168] Röder B, Ermilov EA, Philipp D, Köhl M. Observation of polymer degradation processes in photovoltaic modules via luminescence detection. SPIE 7048; Year.7048:70480F-F-6.

[169] Schneller E, Shiradkar NS, Dhere NG. Baseline testing procedures for PV modules beyond the qualification testing. SPIE 8825; Year.8825:882506--7.

[170] Miller DC, Kempe MD, Glick SH, Kurtz SR. Creep in photovoltaic modules: Examining the stability of polymeric materials and components. 35th IEEE Photovoltaic Specialists Conference (PVSC); Year:000262-8.

[171] Oreski G, Wallner GM. Damp heat induced physical aging of PV encapsulation materials. 12th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems; Year:1-6.

[172] Oreski G, Wallner GM. Aging mechanisms of polymeric films for PV encapsulation. Sol Energy. 2005;79:612-7.

[173] Oreski G, Wallner GM. Evaluation of the aging behavior of ethylene copolymer films for solar applications under accelerated weathering conditions. Sol Energy. 2009;83:1040-7.

[174] Cording CR. Optimizing photovoltaic module glass reliability. SPIE 7048; Year.7048:70480J-J-9.

[175] Sander M, Henke B, Schweizer S, Ebert M, Bagdahn J. PV module defect detection by combination of mechanical and electrical analysis methods. 35th IEEE Photovoltaic Specialists Conference (PVSC); Year:001765-9.

[176] Eitner U, Kontges M, Brendel R. Measuring thermomechanical displacements of solar cells in laminates using digital image correlation. 34th IEEE Photovoltaic Specialists Conference (PVSC); Year:001280-4.

[177] Jorgensen GJ, McMahon TJ. Accelerated and outdoor aging effects on photovoltaic module interfacial adhesion properties. Prog Photovolt. 2008;16:519-27.

[178] Yang H. EVA Adhesion Test Method: 180-peel vs. T-peel in PV applications. NREL Photovoltaic Module Reliability Workshop; Year.

[179] Balzani C, Wagner W, Wilckens D, Degenhardt R, Büsing S, Reimerdes HG. Adhesive joints in composite laminates—A combined numerical/experimental estimate of critical energy release rates. Int J Adhes Adhes. 2012;32:23-38.

[180] Chapuis V, Pélisset S, Raeis-Barnéoud M, Li H-Y, Ballif C, Perret-Aebi L-E. Compressive-shear adhesion characterization of polyvinyl-butyral and ethylene-vinyl acetate at different curing times before and after exposure to damp-heat conditions. Prog Photovolt. 2014;22:405-14.

[181] Novoa FD, Miller DC, Dauskardt RH. Environmental mechanisms of debonding in photovoltaic backsheets. Sol Energy Mater Sol Cells. 2014;120, Part A:87-93.

[182] Kurtz S, Wohlgemuth J, Sample T, Yamamichi M, Amano J, Hacke P, et al. Ensuring quality of PV modules. 37th IEEE Photovoltaic Specialists Conference (PVSC); Year:000842-7.

[183] Wohlgemuth J, Kempe M, Miller D, Kurtz S. Developing standards for PV packaging materials. SPIE 8112; Year.8112:81120A-A-8.

[184] Schneider J, Turek M, Dyrba M, Baumann I, Koll B, Booz T. Combined effect of light harvesting strings, anti-reflective coating, thin glass, and high ultraviolet transmission encapsulant to reduce optical losses in solar modules. Prog Photovolt. 2014;22:830-7.

[185] Miller DC, Wohlgemuth JH. Examination of a junction-box adhesion test for use in photovoltaic module qualification. SPIE 8472; Year.8472:84720M-M-13.

[186] Oldervoll F, Bjomeklett B, Tan TC. Junction box qualification at REC Solar. NREL Photovoltaic Module Reliability Workshop; Year.

[187] Dhere NG, Shiradkar NS. Fire hazard and other safety concerns of photovoltaic systems. J Photonics Energy. 2012;2:022006.

[188] Wohlgemuth J. Module Safety Issues. NREL Photovoltaic Module Reliability Workshop; Year.

[189] Kalejs J. Junction Box and Wiring Issues in Reliability. NREL Photovoltaic Module Reliability Workshop; Year.

[190] Danner M, Bucher K. Reverse characteristics of commercial silicon solar cells-impact on hot spot temperatures and module integrity. 26th IEEE Photovoltaic Specialists Conference (PVSC); Year:1137-40.

[191] Fahrenbruch SA. Solar Bypass Diodes: Then and Now. Sol: PV Management Mag. 2010;VI:21-6.

[192] Silvestre S, Boronat A, Chouder A. Study of bypass diodes configuration on PV modules. Appl Energy. 2009;86:1632-40.

[193] Posbic J, Rhee E, Amin D. High temperature reverse by-pass diodes bias and failures. NREL Photovoltaic Module Reliability Workshop; Year.

[194] Dhere NG, Shiradkar NS, Schneller E, Gade V. The reliability of bypass diodes in PV modules. SPIE 8825; Year.8825:88250I-I-8.

[195] Wunsch DC, Bell RR. Determination of Threshold Failure Levels of Semiconductor Diodes and Transistors Due to Pulse Voltages. IEEE Transactions on Nuclear Science. 1968;15:244-59.

[196] Whitfield K. Diode ESD Characterization. NREL Photovoltaic Module Reliability Workshop; Year.

[197] Loo Jv. Bypass Diodes for PV Modules: 10 years of field experience. Intersolar Europe Conference; Year.

[198] Buttay C, Raynaud C, Morel H, Civrac G, Locatelli M-L, Morel F. Thermal Stability of Silicon Carbide Power Diodes. IEEE Trans Electron Devices. 2012;59:761-9.

[199] Uchida Y, Konishi Y, Okura T. On the occurance of thermal runaway in diodes in the junction box. NREL Photovoltaic Module Reliability Workshop; Year.

[200] TamizhMani G, Li B, Arends T, Kuitche J, Raghuraman B, Shisler W, et al. Failure analysis of design qualification testing: 2007 VS. 2005. 33rd IEEE Photovoltaic Specialists Conference (PVSC); Year:1-4.

[201] Zhang Z, Wohlgemuth J, Kurtz S. Thermal reliability study of bypass diodes in photovoltaic modules. NREL Photovoltaic Module Reliability Workshop; Year.

[202] Kim KA, Krein PT. Reexamination of Photovoltaic Hot Spotting to Show Inadequacy of the Bypass Diode. Photovoltaics, IEEE Journal of. 2015;5:1435-41.

[203] Deline C, Meydbrey J, Donovan M, Forrest J. Photovoltaic Shading Testbed for Module-Level Power Electronics. National Renewable Energy Laboratory; 2012.

[204] Carbone R, Tomaselli A. A High-Efficiency AC PV-Module for High-Quality Connection to Modern Low-Voltage Distribution Grids. Int Rev Electr Eng. 2011;6:2796-805.

[205] Bauwens P, Doutreloigne J. Reducing partial shading power loss with an integrated Smart Bypass. Sol Energy. 2014;103:134-42.

[206] Falvo MC, Capparella S. Safety issues in PV systems: Design choices for a secure fault detection and for preventing fire risk. Case Studies in Fire Safety. 2015;3:1-16.

[207] Trupke T, Pink E, Bardos RA, Abbott MD. Spatially resolved series resistance of silicon solar cells obtained from luminescence imaging. Appl Phys Lett. 2007;90:093506-3.