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Manufacturing of 3D multifunctional microelectronic devices: challenges and opportunities

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Abstract

Sophisticated three-dimensional (3D) forms are expected to be one of the significant development trends in next-generation microelectronics because of their capabilities of rendering substantially enhanced performances, a high degree of integration, and novel functionalities. To date, a diversity of manufacturing methods has been developed for 3D microelectronic devices with different structural and functional features. Most of these methods fall into two categories, i.e., micromanufacturing technologies and mechanically guided 3D assembly approaches. From this perspective, we review the different manufacturing methods and their specific features as well as their limitations. At present, there is still no universal method that can deterministically form 3D microelectronic devices with very high geometric complexity and nanoscale precision. We offer an outlook on future developments in the manufacturing of 3D multifunctional microelectronics devices and provide some perspectives on the remaining challenges as well as possible solutions. Mechanically guided 3D assembly based on compressive buckling is proposed as a versatile platform that can be merged with micromanufacturing technologies and/or other assembly methods to provide access to microelectronic devices with more types of integrated functions and highly increased densities of functional components.

The formation of three-dimensional (3D) microdevices in advanced materials with feature sizes ranging from nanometers to millimeters has important implications in a diversity of areas, from energy storage/harvesting[1], photonic sensing[2,3], and micro/nanoelectromechanical systems (MEMS/NEMS)[4,5] to transistors[6], because of their advantages (e.g., smaller footprint, lower weight, higher functional performance, lower power consumption, high productivity, and potentially lower cost) over planar 2D counterparts. In the last couple of decades, many different approaches have been explored and/or developed to deterministically form 3D microelectronic components and devices. These approaches can be classified into two broad classes: modern micromanufacturing approaches and mechanically guided assembly approaches. Modern micromanufacturing technologies, including lithographic patterning, etching, and deposition, can fabricate 3D microelectronics consisting of simple constructions (e.g., suspended/stacked components) in a relatively direct manner. In contrast, mechanically guided 3D assembly leverages the mature planar processing techniques available in the semiconductor industries to fabricate 2D precursor structures, which are then transformed into well-controlled 3D forms with the aid of various mechanical forces (e.g., capillary forces[7–9], residual stresses[1,2,10], constraint forces in active materials[11–13]). Here, we summarize the advantages and limitations of the aforementioned approaches and provide some perspectives on the remaining challenges as well as possible solutions in the manufacturing of multifunctional 3D microelectronic devices.

Micromachining, which represents one of the first explored micromanufacturing approaches, was initially developed for building 3D MEMS. A diversity of micromachining technologies are now available,

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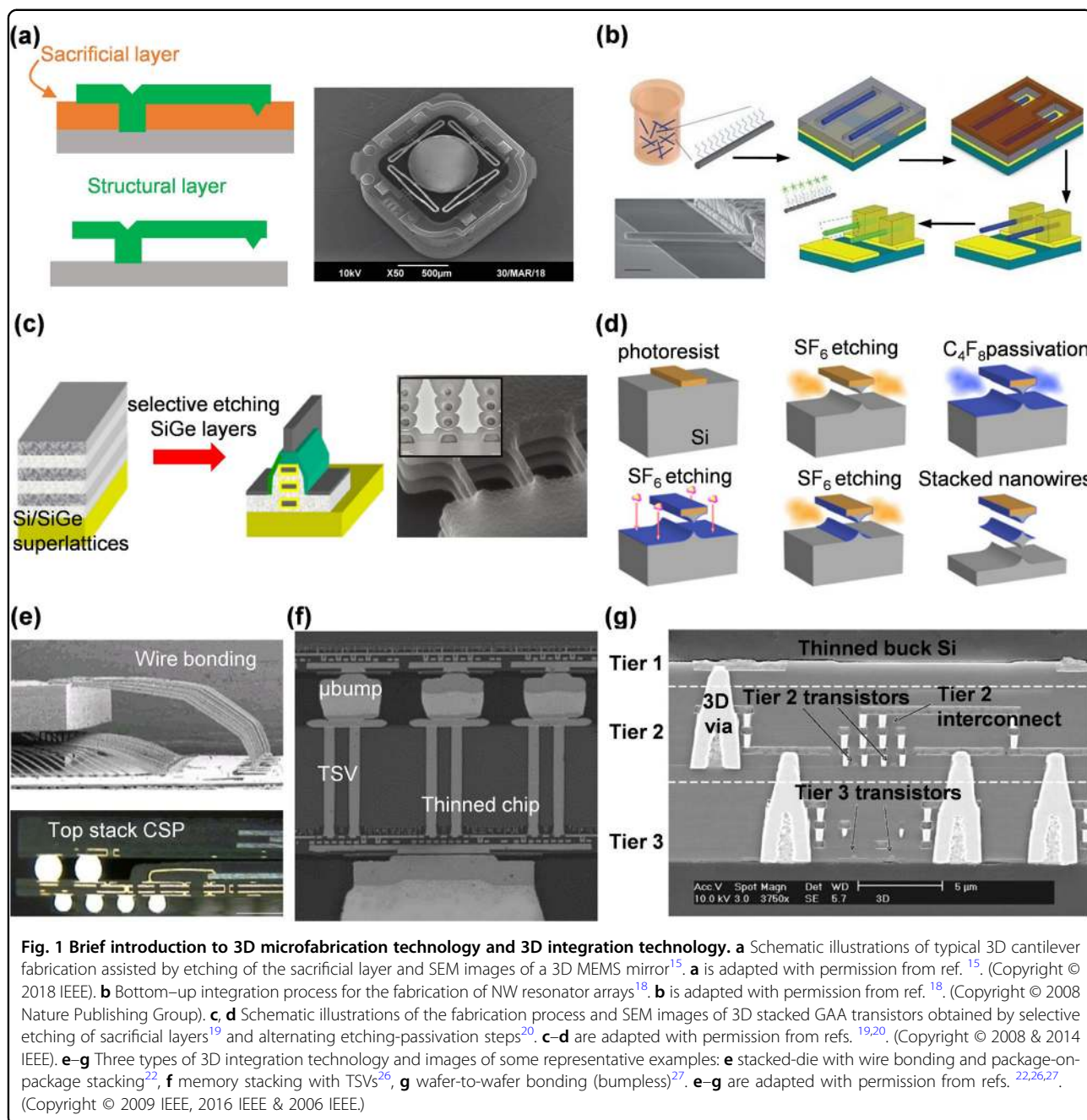
including bulk/surface micromachining, deep reactive ion etching (DRIE), hot embossing, laser and focused ion-beam machining. Among these technologies, the first two (bulk/surface micromachining and DRIE) have thus far been widely exploited in the electronics industries. Bulk micromachining involving the selective removal of the substrate material to obtain 3D components could be achieved by chemical or physical means. Here, chemical wet etching is more popularly used than physical means owing to its higher etch rates, selectivity, and modifiability. According to the directionality of etching, there are two general types—isotropic and anisotropic wet etching—masked with lithography patterning. Surface micromachining techniques offer more precise dimensional and structural control than bulk techniques. These techniques typically include step-by-step deposition and patterning of sacrificial and structural layers, followed by selective removal of the underlying sacrificial layer to release the 3D structural layer[14], as illustrated in Fig. 1a. For 3D MEMS with high aspect-ratio features, DRIE (also termed the 'Bosch process') was developed by alternately etching Si and depositing etch-resistant material on the sidewalls, which can avoid the etching of sidewalls. Recent studies extended this technology to a wider range of materials (e.g., silicon carbide, titanium, tungsten, glass, and polymers), which demonstrates it as a cost-effective method of deep etching with high selectivity and precision. Although the frequent switching of gases and etching parameters makes the equipment quite complicated and expensive, DRIE is still one of the most widely used techniques to accurately realize high aspect-ratio etching. According to the specific requirements of different applications, various micromachining technologies can be combined to manifest the feature of each technology, enabling the manufacture of 3D MEMS with diverse suspension geometries (e.g., the 3D MEMS mirror[15] in Fig. 1a). In addition, bottom–up approaches that build smaller units (usually atoms and molecules) into more-complex assemblies based on their chemical properties also represent an important class of manufacturing approaches to the self-assembly of a variety of morphological functional nanomaterials[16], ranging from quantum dots, nanowires (NWs), and nanotubes to two-dimensional materials. Integration strategies[17] that combine bottom–up nanomaterials with micromachining technologies can facilitate the fabrication of 3D nanodevices. An example shown in Fig. 1b illustrates the fabrication of NW resonator arrays using these bottom–up integration processes[18].

The persistent demand for higher functional density, higher performance, and lower power consumption has been driving the structure of transistors to gradually evolve from the traditional planar layout to the current widely used Fin-FETs (tri-gate) and to the next-generation 3D gate-all-around (GAA) structures. In 2008, T. Ernst et al.[19] demonstrated a 3D stacked GAA multichannel CMOS by selective removal of sacrificial SiGe layers from multilayer Si/SiGe superlattices epitaxially grown on top of silicon-on-Insulator (SOI) substrates and gate-stack deposition of Si multichannels all around, as shown in Fig. 1c. By introducing the etch-passivation cycle into DRIE technology, De Marchi et al.[20] and Lee et al.[21] developed techniques for etching suspended multi-NW GAA FETs on an SOI substrate and on a bulk silicon substrate, respectively, as illustrated in Fig. 1d. According to recent reports from IMEC and Samsung, the 3D GAA FET architecture is a very promising candidate to extend Moore's Law for future technology with <7 nm nodes. The innovation of 3D transistors through the introduction of new processing technologies will continue to drive the development of the microelectronics industry.

To achieve more diverse functions and a higher degree of integration, beyond those achievable through simple lithography scaling based on a single chip (system on chip), technologies of heterogeneous integrations in 3D architecture have been attracting increasing attention, such as 3D integrated circuit (IC) packaging, 3D IC integration, and 3D Si integration[22,23]. Invented in the 1980s, 3D IC packaging has now been widely used in industries as a type of mass production technology, a key component of which involves stacking several conventional components in the vertical direction with robust electrical connections (e.g., wire bonding and package-on-package stacking, as shown in Fig. 1e). With the assistance of through-silicon-via (TSV) technology[23–25] that enable a vertical interconnection completely through a silicon wafer, 3D IC/Si integration technologies were developed to achieve a higher level of integration than are possible with Moore technologies. Compared with 3D IC packaging, 3D IC integration can stack much thinner IC chips with TSVs and microbumps[26] (Fig. 1f), thereby offering higher integration, a smaller footprint, higher performance, and lower power consumption. With a bumpless and smaller TSV diameter, 3D Si integration (Fig. 1g) aims to achieve further enhanced integration through direct wafer-to-wafer bonding[27] and is considered the best means of competing with Moore's law. However, there are still many technical issues to be solved to enable batch manufacturing, such as thermal management, vias formation, and thin-wafer handling.

The development of the aforementioned micro-manufacturing technologies has offered the capabilities of achieving a variety of 3D suspended MEMS structures, stacked GAA transistors, and 3D ICs. Their relatively high cost and low efficiency, however, represent prevalent issues with these technologies, especially in the fabrication of relatively complex 3D constructions. Moreover, devices

Fig. 1 Brief introduction to 3D microfabrication technology and 3D integration technology. a Schematic illustrations of typical 3D cantilever fabrication assisted by etching of the sacrificial layer and SEM images of a 3D MEMS mirror[15]. **a** is adapted with permission from ref. [15]. (Copyright © 2018 IEEE). **b** Bottom–up integration process for the fabrication of NW resonator arrays[18]. **b** is adapted with permission from ref. [18]. (Copyright © 2008 Nature Publishing Group). **c, d** Schematic illustrations of the fabrication process and SEM images of 3D stacked GAA transistors obtained by selective etching of sacrificial layers[19] and alternating etching-passivation steps[20]. **c–d** are adapted with permission from refs. [19,20]. (Copyright © 2008 & 2014 IEEE). **e–g** Three types of 3D integration technology and images of some representative examples: **e** stacked-die with wire bonding and package-on-package stacking[22], **f** memory stacking with TSVs[26], **g** wafer-to-wafer bonding (bumpless)[27]. **e–g** are adapted with permission from refs. [22,26,27]. (Copyright © 2009 IEEE, 2016 IEEE & 2006 IEEE.)

with more complex 3D geometries (e.g., conical spirals and hemispherical and polyhedral shapes) are almost inaccessible to these technologies.

The approaches based on mechanically guided 3D assembly represent an alternative route to the formation of 3D microelectronic devices with the ability to build highly complex 3D geometries, including those with multilevel and even hierarchical constructions. As indirect routes that can make full use of the well-established planar technologies in the semiconductor and integrated photonic industries, this class of approaches offers a broad range

of applicability, either to most of the different types of materials available (e.g., semiconductors, metals, polymers, ceramics) or over different length scales (from tens of nanometers to centimeters)[28]. A key aspect of these approaches involves the application of different types of mechanical forces (residual stress[1,2], constraint forces in heat/light/solvent-responsive active materials[11,13,29], capillary forces[7,8], and the compressive forces associated with a soft substrate[3,30,31]) to deform strategically designed 2D precursor structures into 3D configurations through bending, twisting, or a mixed mode of deformations.
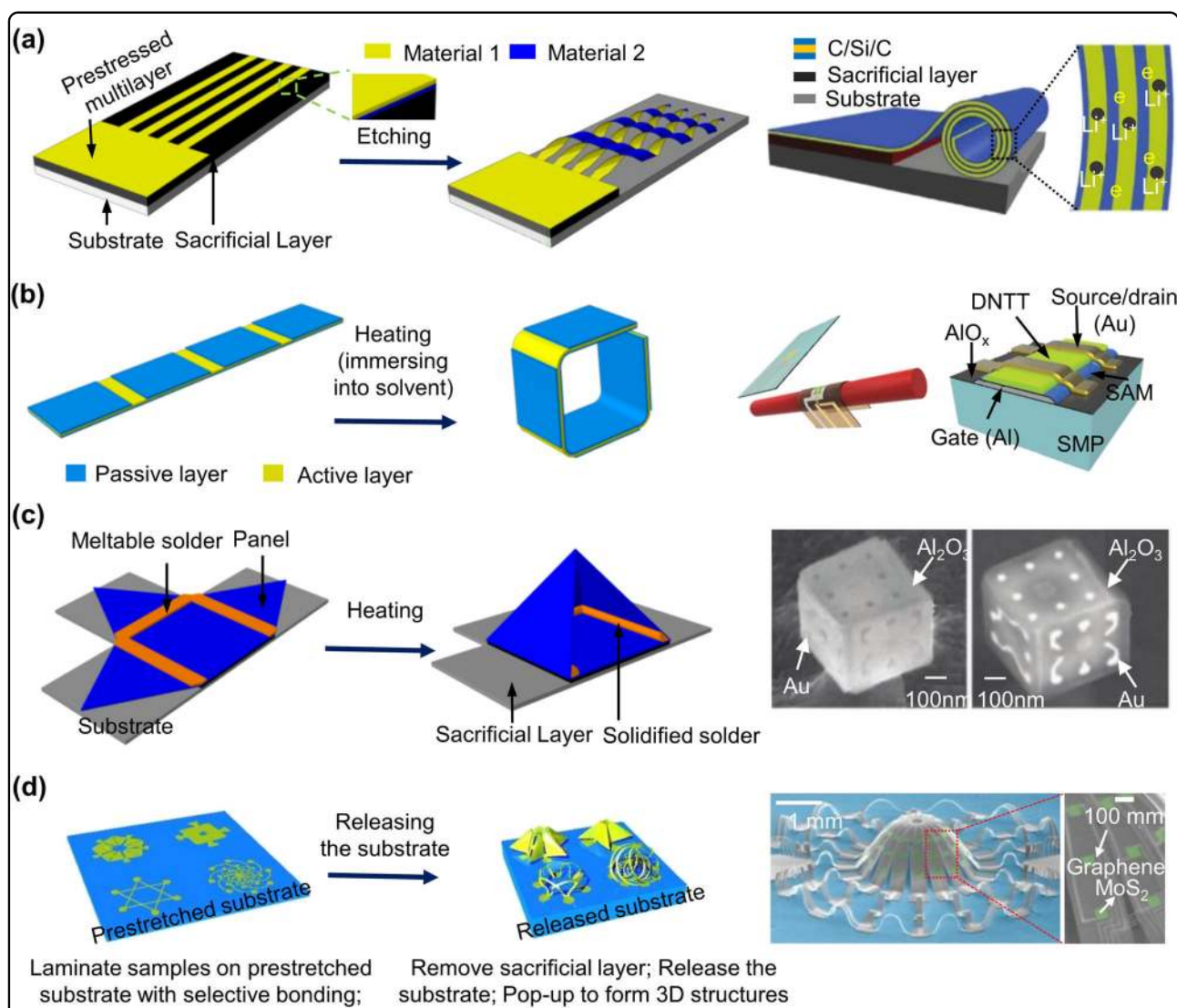
Fig. 2 Assembly of 3D mesostructures and microdevices through a variety of different mechanical forces. a Schematic illustration of residual stress-induced rolling and its application to lithium-ion batteries[1]. **a** is adapted with permission from ref. [1]. (Copyright © 2013 Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim). **b** Folding-dominated method that relies on the use of active materials and its application in 3D deployable organic thin-film transistors (OTFTs)[12]. **b** is adapted with permission from ref. [12]. (Copyright © 2014 Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim). **c** Folding-dominated method induced by capillary forces and a representative microelectronic device with optically active split-ring resonator (SRRs) patterns[7]. **c** is adapted with permission from ref. [7]. (Copyright © 2011 Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim). **d** Mechanically guided 3D assembly by compressive forces imparted by a prestrained substrate[28] and 3D photodetection systems capable of measuring incident light parameters[3]. **d** is adapted with permission from ref. [3]. (Copyright © 2018 Macmillan Publishers Limited, part of Springer Nature)

Figure 2a shows a schematic illustration of the residual stress method used to fabricate tubular or helical 3D electronic devices at the nanoscale[1]. By controlling the relevant fabrication parameters (e.g., deposition rate, temperature, or composition), the misfit strain between the top and bottom layers induces the self-rolling of 2D precursors into deterministic 3D structures after the selective etching of the sacrificial layer[32]. Using these methods, some impressive 3D electronic devices were fabricated, ranging from rolled-up field effect transistors

with higher (by five orders) on-ratios[33], 3D tubular infrared photodetectors with a widened visual field[2], and 3D radio frequency (RF)/microwave air-core transformers with highly enhanced performance compared with that of their other reported on-chip planar counterparts[34]. A representative example of a microelectronic device with remarkable cycling performance is shown in Fig. 2a. The heterogeneous integration of multiple electronic components at different in-plane locations (e.g., ICs) remains a challenge.

Figure [2]b illustrates a strategy that leverages the constraint forces arising from the strain mismatch of active materials (e.g., hydrogels[35], shape memory alloys/polymers[29], liquid crystal elastomers[36]) and passive materials to drive 2D-to-3D transformations. In the presence of external stimuli (e.g., high temperature, solvent, or light exposure), the recovery of a programmable SMP/SMA or the swelling of a hydrogel results in spatially nonuniform strains along the out-of-plane direction, thereby leading to bending or folding deformations that can be used as a basis of origami assembly. Some representative devices have been fabricated using this approach, such as 3D deployable organic thin-film transistors (OTFTs)[12] and 3D humidity sensors[13]. In response to a temperature increase, the planar OTFT demonstrated in Fig. [2]b can deploy into 3D complex shapes (e.g., helix) with the capability of actively conforming to target objects without any significant electrical degradation. In this approach, the active materials that operate in different particular environments impose certain limitations on the integration of microelectronic devices, and scalability sets practical constraints on industrial applications.

Capillary forces or surface tension serves as another type of mechanical trigger to drive the 3D assembly of microelectronic devices from 2D patterns. Figure [2]c schematically illustrates the folding assembly of a 3D structure guided by the capillary forces of the melted solder. These approaches have been exploited to achieve high-performance microelectronic devices, such as 3D photovoltaic devices with a higher conversion efficiency than their planar counterparts[8] and cubic plasmonic resonators with optically active split-ring resonator patterns[7]. However, the presence of water or meltable solder at the folding creases of 3D microelectronic devices places certain limitations on their practical applications. The accessible range of 3D geometries based on this method (Fig. [2]c) and those shown in Fig. [2]a and b is constrained by the simple mode of deformations, mainly in terms of bending.

Figure [2]d presents a strategy that relies on the compressive forces of a prestrained soft substrate to transform 2D microelectronic devices into a 3D configuration through controlled compressive buckling. Since this process involves coordinated bending/twisting deformations as well as translational/rotational motions, a rich diversity of 3D geometries (Fig. [2]d) can be formed, together with the kirigami/origami design concepts associated with strategic engineering of the 2D precursor patterns and the substrates. Recent advances have demonstrated the utility of this assembly approach in obtaining a variety of advanced multifunctional devices, such as 3D scaffolds for engineered dorsal root ganglion neural networks[37], wearable physiological status-monitoring platforms with 3D interconnected networks of helical microcoils[38], 3D photodetection systems

capable of measuring incident light parameters (i.e., direction, intensity)[3], high-performance hemispherical electrically small antennas with tunable working frequencies[39], 3D energy-harvesting devices with broadband operation and high efficiency[40], 3D interdigital supercapacitors with solid-state electrolytes[41], and 3D RFelectronic devices capable of concealing themselves from external detection[42]. Although this compressive buckling approach is applicable to a broad range of materials and 3D geometries, it is still very challenging to form freestanding 3D electronic devices without any accessories or those with lateral dimensions down to several hundreds of nanometers. The development of inverse design algorithms that can map targeted 3D configurations onto the initial 2D precursor structures also represents an unsolved problem that is central to this approach.

Although the aforementioned methods each offer specific 3D fabrication features and capabilities, none of them is without limitations, either in terms of material compatibility, accessible feature sizes and 3D layouts or the integrability of diverse functional components. Recent studies suggest that the effective combination of different technologies could provide possible solutions to overcome some of those limitations. For example, 3D IC integration technology enables the construction of an interposer (carrier) microdevice that incorporates fluidic microchannels fabricated through wet etching for thermal management[25], as shown in Fig. [3]a. Figure [3]b demonstrates a TSV-based 3D integration of the chip-scale package of MEMS and ICs, both of which are formed using micromachining technology[43]. This type of heterogeneous integration of multiple functional components (e.g., logic processors, RF devices, biochips, sensors, MEMS) into a single chip may provide cost-optimized and value-added system solutions, which are a popular research field in both industry and academia. By introducing thin patterned layers with well-defined residual stresses as 2D precursor structures, mechanically guided 3D assembly based on compressive buckling is able to form highly complex 3D geometries that are otherwise inaccessible to a separate approach[44]. Based on such a combination, 3D configurations that evolve from high-order buckling modes or those that are transformed through concurrent global buckling and local rolling can be achieved, with an example shown in Fig. [3]c. In addition, the residual stresses owing to the metal plasticity result in irrecoverable deformations at predefined locations with high strains, which can be utilized to yield freestanding 3D mesostructures assembled through compressive buckling (Fig. [3]d)[37]. Such untethered 3D metallic mesostructures bypass the engineering constraints set by the underlying elastomer substrates and hold promise for applications in flexible microrobotics and biological scaffolds.
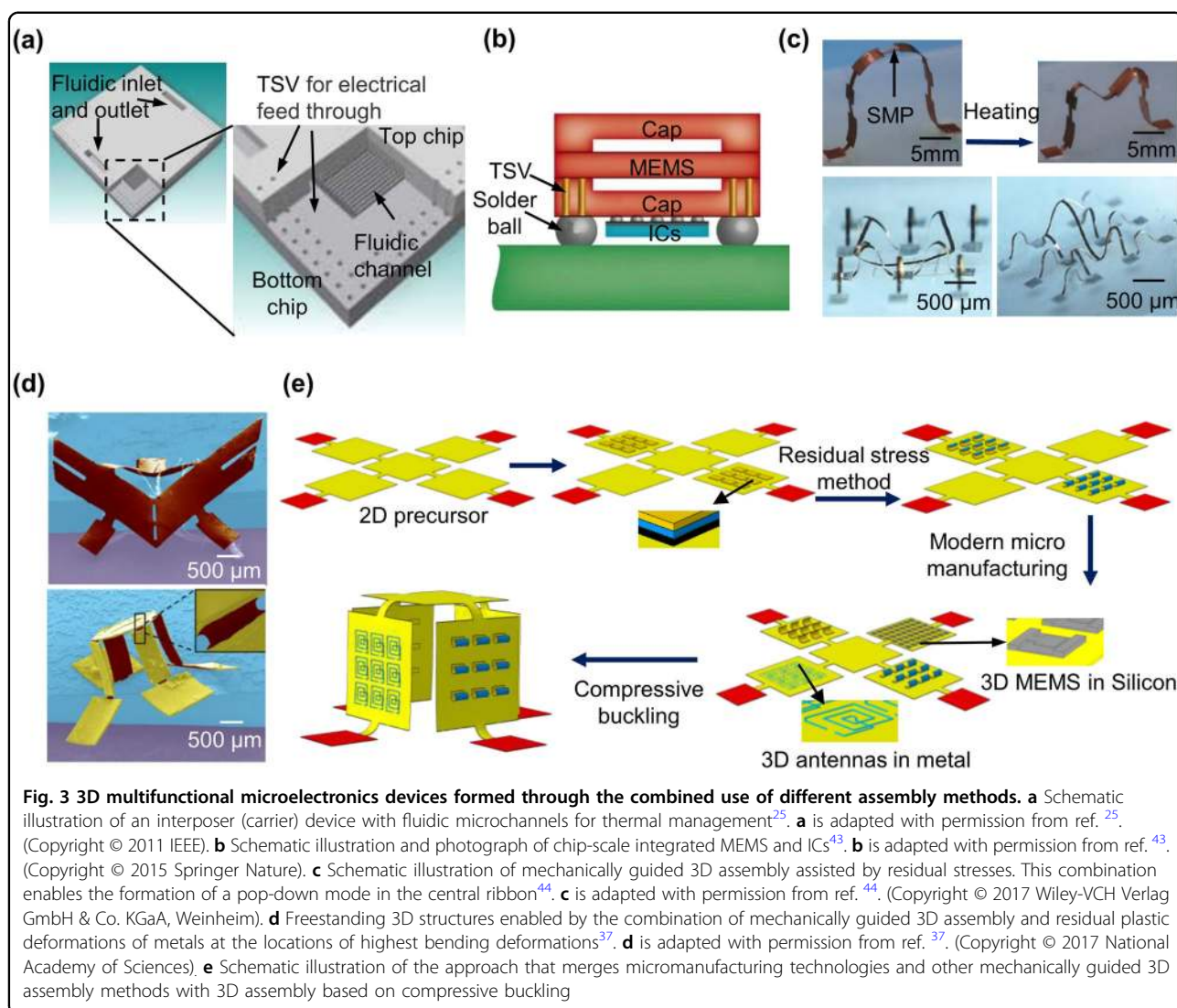
Fig. 3 3D multifunctional microelectronics devices formed through the combined use of different assembly methods. a Schematic illustration of an interposer (carrier) device with fluidic microchannels for thermal management[25]. **a** is adapted with permission from ref. [25]. (Copyright © 2011 IEEE). **b** Schematic illustration and photograph of chip-scale integrated MEMS and ICs[43]. **b** is adapted with permission from ref. [43]. (Copyright © 2015 Springer Nature). **c** Schematic illustration of mechanically guided 3D assembly assisted by residual stresses. This combination enables the formation of a pop-down mode in the central ribbon[44]. **c** is adapted with permission from ref. [44]. (Copyright © 2017 Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim). **d** Freestanding 3D structures enabled by the combination of mechanically guided 3D assembly and residual plastic deformations of metals at the locations of highest bending deformations[37]. **d** is adapted with permission from ref. [37]. (Copyright © 2017 National Academy of Sciences). **e** Schematic illustration of the approach that merges micromanufacturing technologies and other mechanically guided 3D assembly methods with 3D assembly based on compressive buckling

Because of the broad applicability to nearly any type of materials and the capability of integrating with diverse microelectronic devices, including commercial available platforms (e.g., a flexible printed circuit board), mechanically guided 3D assembly based on compressive buckling has the potential to serve as a fundamental platform for the 3D fabrication of microelectronic devices. Merging the other micromanufacturing technologies and/or assembly approaches with the above fundamental platform is anticipated to offer unprecedented capabilities and scalabilities (Fig. 3e). For example, nanoscale MEMS and GAA transistors with simple 3D configurations formed using micromachining and integration technologies could serve as a generalized, advanced form of 2D precursors in mechanically guided assembly to obtain hierarchical microelectronic devices with increased device densities and/or novel functionalities. The devices formed in this manner could encompass a diversity of 3D functional components over different length scales, targeted for the integration of multiple functionalities into a single system. Vast opportunities also exist in the development of viable technologies and experimental equipment that can precisely apply additional types of mechanical forces (e.g., residual stresses, constraint forces in heat/light/solvent-responsive active materials) based on the assembly platform of compressive buckling. Further research along this direction could follow by exploring the extended capabilities of 3D assembly and the reconfigurability of 3D microelectronic devices.

Author's contributions
X.G. and Z.X. contributed equally to this work. Y.Z., X.G., and Z.X. wrote the text and designed the figures. Y.Z. guided this work and designed the plan of the whole perspective. All authors commented on the paper.

Conflict of interest
The authors declare that they have no conflict of interest.

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