# Manufacturing Pathway and Associated Challenges for Nanoscale Computational Systems

Pritish Narayanan, Kyoung Won Park, Chi On Chui, and C. Andras Moritz

*Abstract* – **We propose one possible manufacturing pathway for realizing nanodevice based computational fabrics that combines self-assembly based techniques with conventional photolithography. This pathway focuses on realizing the fabric as a whole including assembly of nanostructures, functionalization of devices, contacts and interconnects. Furthermore, this pathway is scalable to large systems, as multiple devices are created simultaneously in a self-aligning process step. We discuss the key sequence of steps for achieving nanoscale computational systems using the example of a simple digital logic circuit, and review the associated challenges involved for each of these.**

**Keywords: NASIC, Nanoscale fabrics, self-assembly**

## INTRODUCTION

Reliable manufacturing of nanodevice based computational systems continues to be challenging. While individual nanodevices have been shown with desirable electrical characteristics (e.g. diodes/FETs) [1][2], key questions remain: how can many such devices be assembled into large scale functional systems, how will they be interfaced with the micro/macro-worlds, how to realize the interconnect between them, and what are the benefits at the system level (e.g. density, performance, power, and cost) over an equivalent conventional CMOS based system?

There have been several examples of logic devices and circuitry consisting of a few nanodevices such as a ring oscillator with carbon nanotubes [1], a decoder on nanowires (NWs) [2], and an XOR gate [3]. While these and other works are very important for the prototyping and/or device characterization purposes one key challenge is scalability: a manufacturing pathway by which orders of magnitude more nano-devices can be integrated together has never been shown. Furthermore, most work in the literature focuses on creating individual nanodevices or nanostructures followed by interfacing and contacting to build logic gates and circuits – an approach that is not scalable.

One nanoscale computational fabric is Nanoscale Application Specific Integrated Circuits (NASICs) [4]-[5]. NASICs implement logic on semiconductor NWs with field-effect transistors (FETs), and microwires that provide VDD, GND and control signals for data streaming. In NASICs, several manufacturing requirements have already been mitigated at various system levels including:

- NASIC designs use regular semiconductor NW crossbars without any requirement for arbitrary sizing, placement or doping. Regular nanostructures with limited customization are more easily realizable with unconventional nanofabrication approaches.
- NASIC circuits require only a one type of FET [4] in logic portions of the design.
- Local interconnection between individual devices as well as between adjacent crossbars is achieved entirely on NWs; interconnection of devices does not introduce new manufacturing requirements such as when individual devices need to be connected (e.g., in CMOS).
- NASICs tolerate high defect rates using built-in fault tolerance techniques [5], and do not need complex micro-to-nano interfacing as required by many reconfigurable fabrics.

In this paper we explore a manufacturing sequence for realization of the NASIC fabric as envisioned by its architects. While individual steps have been shown previously, this paper describes for the first time how a 2-D nanoscale computational fabric can be achieved through a sequence of self-assembly and photolithography process steps. The pathway focuses on realizing the fabric as a whole (with contacts, interconnects and devices all incorporated), as opposed to approaches that focus on interconnecting individual devices. Furthermore, it is scalable, i.e., a large number of individual devices can be simultaneously created as part of the fabric itself in a self-aligning process step. Key challenges are also discussed. The trend towards regular fabrics is also relevant to CMOS: as discussed in [6], optical lithography limitations might cause CMOS to forgo zig-zag and complex patterning.

## MANUFACTURING PATHWAY

Figure 1(A) shows a NASIC 1-bit full adder circuit. It consists of a NW crossbar (or tile) with crossed NWs FET (CNWFETs) at certain crosspoints. A limited number of control signals (*hpre, heva, vpre, veva*) from external CMOS circuitry are used to dynamically control data through NWs. The generated output signals act as the inputs to other tiles, and hence all interconnections are local (between neighboring tiles), and achieved on NWs themselves. VDD, GND supply rails at the extremities of the tile are also shown.

Key steps in manufacturing NASIC are shown in Figure 1. Horizontal NWs are grown and aligned on a substrate. In general, nanowire alignment can be *in-situ* or *ex-situ*. *In-situ* refers to techniques where nanowires are aligned in parallel arrays during the synthesis phase itself. On the other hand, *ex-*

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*situ* refers to techniques where nanowire synthesis and alignment are carried out separately.

Lithographic contacts for VDD and GND as well as some control signals are created (1.B). A photolithography step is used to protect regions where transistors will be formed while creating high conductivity regions - using ion implantation - elsewhere (1.C, D). Ion implantation creates $n^+/p/n^+$ regions along the nanowires which under suitable electrical fields act as inversion mode source/channel/drain regions.

Gate dielectric layer is then deposited (or oxide is grown) (1.E) followed by alignment of vertical NWs. The above steps are now repeated for the vertical NW layer (F-H). During ion implantation on vertical NWs (H), channels along horizontal NWs are self-aligned against the vertical gates.

Key individual steps and challenges are discussed in detail in the following subsections.

### A. *Nanowire Alignment*

The ideal technique to form aligned nanowire arrays should guarantee an intrinsic and concurrent control over three key parameters: (i) the number of nanowires, (ii) the inter-nanowire pitch, and (iii) the nanowire diameter within the array. The state-of-the-art semiconductor nanowire array formation with alignment techniques can be broadly classified into the following three categories:

a) ***In-situ* Aligned Growth**: *In-situ* aligned growth refers to techniques where nanowires are synthesized on a target substrate in an aligned fashion. Alignment during growth is typically achieved using some form of guiding. Representative techniques include substrate or template guiding [9][10], electric field guiding [11][12], and gas flow guiding [13]. While arrays containing more of less parallel nanowires have been demonstrated using these techniques, the desired control over the key parameters listed above could not be achieved. The control of pitch and diameter depends on the catalyst engineering since the nanowire synthesis often relies on catalytic processes. The alignment challenge thus hinges on to the ability to form a nanoscale periodic array of catalyst nanoparticles as a dotted straight line, whose diameter distribution should be narrow. In addition, the catalyst material compatibility with the substrate and the thermal budget involved in the nanowire synthesis are two other major technological limitations for *in-situ* techniques.

b) ***Ex-situ* Aligned Assembly**: The semiconductor nanowires are first synthesized elsewhere (through techniques such as Vapor-Liquid-Solid (VLS) growth) and then assembled onto the target substrate. The representative techniques include the Langmuir-Blodgett technique [14][15], fluidic-guided method [16], electric field guided assembly [17], organic self-assembly [18][19], and contact printing [20]. While almost parallel nanowire array prototypes have been fabricated, these methods however permit no control over the precise assembly locations as well as key parameters listed above. The critical challenge is therefore to attach each nanowire onto a precise position on the substrate surface and in the right orientation. This in turn rests on the feasibility to prepare a periodic line array with nanoscale pitch and linewidth on the substrate surface, a process which can obtain substantial leverage on the advances in lithography. Compared to *in-situ* approaches, *ex-situ* techniques offer a much wider variety of material choice and synthesis process owing to the ultra-low thermal budget involved. In addition, a tighter distribution of the nanowire diameter is allowed as the source nanowire materials could be purified prior to the assembly process.

c) **Nanolithography-based Patterning-and-Etching**: In these approaches, a semiconductor material layer pre-formed on the

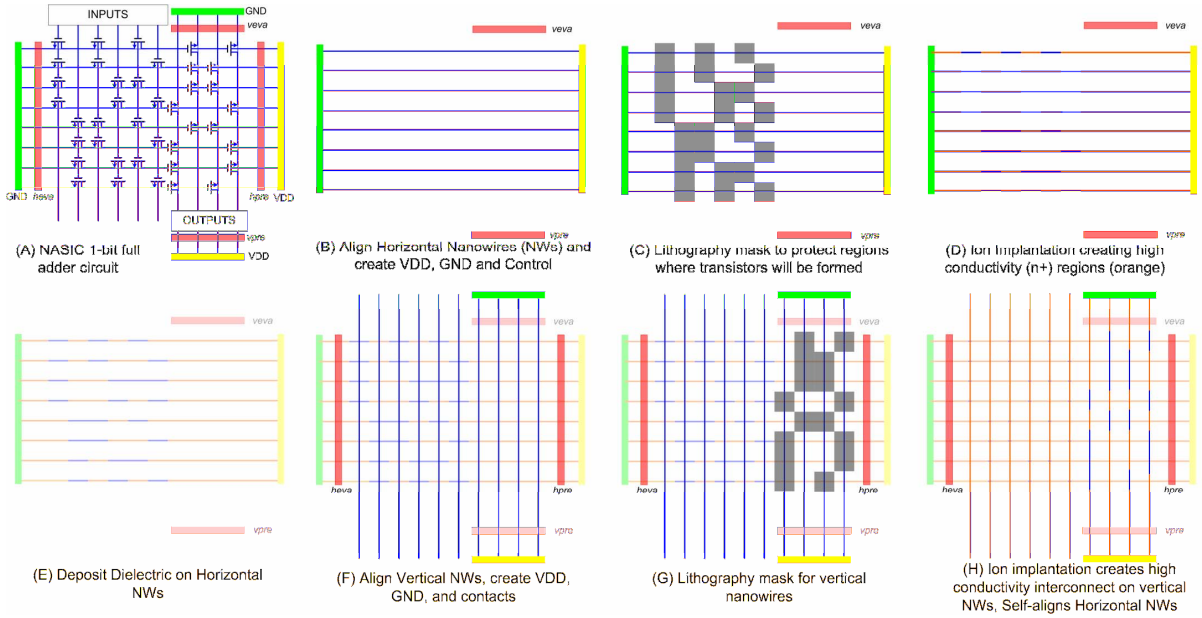


**Figure 1. NASIC Manufacturing Pathway**

target substrate surface is first patterned by nanolithography and then anisotropically etched to create a periodic nanowire array. While the etching process is rather standard, there are two very promising nanoscale patterning techniques including the nanoimprint lithography (NIL) [21] and superlattice nanowire pattern transfer (SNAP) [3][22]. These approaches in principle meet the aforementioned criteria yet they possess some subtle practicality concerns. Since the surfaces of these nanowires are usually damaged during the etching process, cautions should thus be exercised to prevent significant degradation in the resultant device performance. Also the choice of semiconductor nanowire material is more limited compared to either the *in-situ* or *ex-situ* approach.

The construction of the 2D nanowire fabric for NASIC circuit applications consists of two aligned nanowire array formation steps. The first (and bottom) semiconductor nanowire array can be formed by either the nanolithography-based patterning-and-etching technique or *ex-situ* aligned assembly method. The former selection is primarily driven by the material choice – silicon. Since silicon-on-insulator (SOI) substrates are readily available, the patterning-and-etching technique could be considered due to its outstanding alignment capability as long as nanowire surface damage is be minimized. Alternatively, the *ex-situ* method remains an attractive solution with the advantages and challenges discussed above.

The second (and top) array is preferentially formed by the transferring of a pre-aligned nanowire array assembled using either the *ex-situ* or *in-situ* approach. The choice of a particular technique would depend on its ability to accomplish the key specifications outlined above. Since the same material (silicon) with roughly the same nanowire diameter and pitch is required in both arrays, it is therefore beneficial to employ the same method (i.e., *ex-situ* aligned assembly) and repeat it twice.

### *B. Functionalization of Nanowires*

Figure 2 shows the structure of a crossed nanowire FET device used in the NASIC fabric. The gate, drain and source terminals are doped $n^+$, whereas the channel used *p*-type doping (shown in blue in Figure 2) for inversion mode operation. Similar to conventional FET devices, the potential applied at the gate controls the flow of electrons between the source and drain terminals. Functionalization of nanowire arrays is required to define the positions of transistors on the grid for achieving arbitrary logic functions, and create high conductivity interconnects elsewhere.

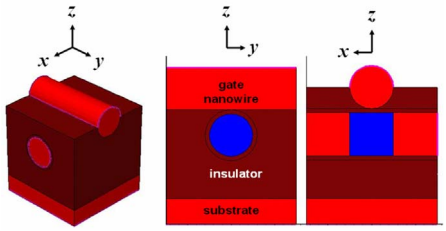


**Figure 2 Crossed Nanowire FET structure showing gate, drain, source and channel regions**

Nanowires assembled on the substrate are initially doped uniformly along their lengths. The doping type corresponds to the channel doping of the inversion mode FET devices (for example, if *n*-type FETs are needed, the nanowires transferred to the substrate will originally contain *p*-type dopants).

We propose to use ion implantation, a well controlled technique used in the semiconductor industry, to create: a) high conductivity regions on nanowires where transistors do not exist, b) gate material of NWs, and c) gate self-aligned FET channels. The minimum feature size assuming perfect registration and alignment is calculated to be (2×pitch – width) squares. Smaller squares can tolerate less precise registration. Given that there is a one nanowire per pitch alignment requirement, the smallest feature size in the worst case is then pitch × pitch squares (Figures 1.C and 1.G).

Ion implantation of horizontal nanowires is shown in Figures 1.C, 1.D. These steps create high conductivity regions along the assembled horizontal nanowires. $n^+/p/n^+$ regions are formed on the left side of figure 1.D; these act as source/channel/drain regions. The $n^+$ regions on the right of Figure 1.D are gates for vertical nanowires that will be assembled in subsequent steps. An additional silicidation step could be done to further improve the conductivity of the $n^+$ regions defined in this step.

Figures 1.G, 1.H show ion implantation steps applied to vertical nanowires. The six vertical nanowires on the left are doped $n^+$ and act as gates for underlying horizontal nanowire channels. The four vertical nanowires to the right contain $n^+/p/n^+$ source/channel/drain regions and are gated by underlying horizontal nanowires. Furthermore, this ion implantation step self-aligns the horizontal channels on the left side of the figure against the vertical nanowire gates.

It must be noted that lithography is used to protect regions where FETs will be formed, and not for complex patterning. In conjunction with self-alignment, this implies that precise shapes with sharp edges are not needed. NASIC built-in defect tolerance techniques [5] further ameliorate requirements on lithography. Fewer masks and NASIC's built-in fault tolerance imply that it may be possible to build NASICs at a much lower manufacturing cost and finer resolution than scaled CMOS.

The manufacturing pathway in Figure 1 needs nanowires to be transferred on to the substrate twice, once each for horizontal and vertical nanowires. This implies that vertical CNWFET channels are not on the substrate, but placed above layers of horizontal nanowires and oxide; this poses some challenges in terms of self-alignment of these channels against horizontal nanowire gates, as well as for achieving body biasing, which is used to tune device characteristics in NASICs (e.g., $V_{TH}$, ON-to-OFF current ratios).

These concerns may be overcome by using an approach that uses 3 separate nanowire transfers as shown in Figure 3– A) vertical NWs in the output plane are first transferred, and ion implantation with lithographic masks is carried out; B) horizontal NWs are transferred after gate dielectric deposition,

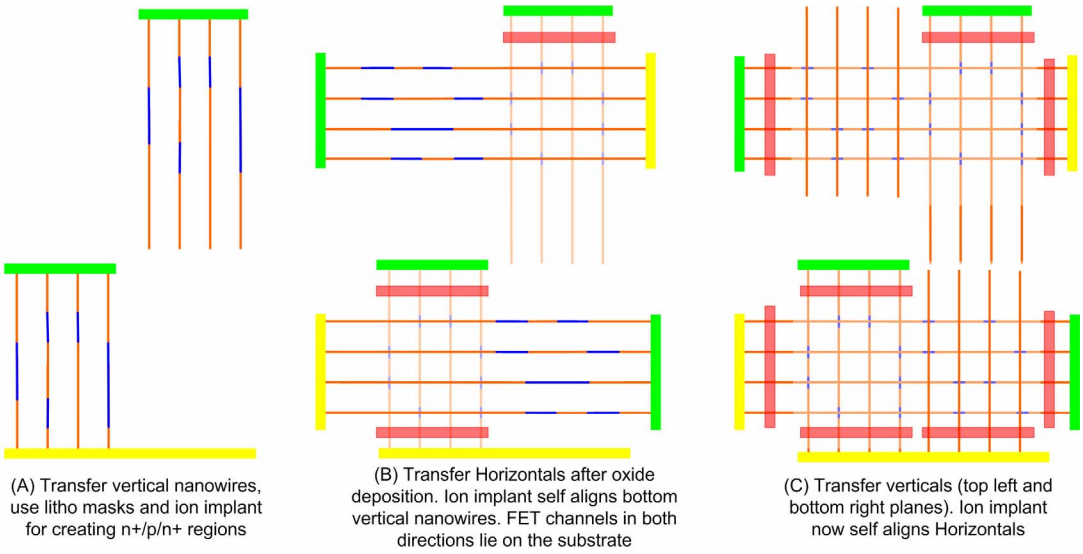


**Figure 3. NASIC Manufacturing using 3 nanowire transfers**

these NWs are self-aligned with the previously transferred verticals; and C) input plane verticals are transferred and ion implantation self-aligns these with the underlying horizontals. This approach, however, poses challenges in terms of alignment of input vertical nanowires in one NASIC tile against output nanowires of the previous tile, as well as achieving of physical interconnections between nanowires assembled in separate steps.

## CONCLUSIONS

One possible manufacturing pathway for the NASIC fabric was shown. Ultimately, realizing a nanodevice based computing system will need to bring together researchers from across a spectrum of expertise, including patterning, assembly, nano-devices, circuits, fault-tolerance, and architecture. We hope to stimulate this interdisciplinary discussion towards achieving nanodevice based computational fabrics.

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