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Mask Defect Verification Using Actinic Inspection and Defect Mitigation Technology

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ABSTRACT

The availability of defect-free masks remains one of the key challenges for inserting extreme ultraviolet lithography (EUVL) into high volume manufacturing. The successful production of defect-free masks will depend on the timely development of defect inspection tools, including both mask blank inspection tools and absorber pattern inspection tools to meet the 22 nm half-pitch node. EUV mask blanks with embedded phase defects were inspected with a reticle actinic inspection tool (AIT) and the Lasertec M7360. The Lasertec M7360 is operated at SEMATECH's Mask blank Development Center (MBDC) in Albany, with sensitivity to multilayer defects down to 40~45 nm, which is not likely sufficient for mask blank development below the 32 nm half-pitch node. Phase defect printability was simulated to calculate the required defect sensitivity for the next generation blank inspection tool to support reticle development for the sub-32 nm half-pitch technology node. This paper will also discuss the kind of infrastructure that will be required in the development and mass production stages.

Keywords: EUV, mask, phase defect, DUV inspection, actinic inspection

1. INTRODUCTION

Over the past year, the interest by leading edge chip manufacturers has tangibly shifted towards the insertion of extreme ultraviolet lithography (EUVL) into production. This emphasis is increasing the pressure to overcome the lack of defect-free blanks, which remains one of the key challenges impeding the insertion of EUVL into manufacturing. The success of the industry's mask blank defect reduction effort critically depends on the timely availability of inspection tools that can precisely and reliably find ever smaller defects. SEMATECH's Mask Blank Development Center (MBDC) facility has provided the world's best defect inspection capability starting in 2003 with the Lasertech M1350 tool, followed by the second generation defect inspection tool, the M7360, in 2006. Both tools use deep ultraviolet (DUV) light sources for defect detection: the 488 nm wavelength for the M1350 and 266 nm wavelength for the M7360. However, to meet high volume manufacturing (HVM) requirements for sub-32 nm half-pitch (HP) patterning, the industry needs a third generation of defect inspection tools capable of finding defects ≤ 20 nm on mask blanks with a high capture rate and high blank throughput. In addition, these tools will also need to support extendibility assessments of low defect deposition technologies and the associated infrastructure development towards meeting 22 nm HP defect specifications. SEMATECH operates the actinic inspection tool (AIT) at Lawrence Berkeley National Lab (LBNL) and a state of the art Lasertec M7360 to support the development of inspection tools and reticle blanks to eventually meet HVM requirements. In this paper, we simulated the required defect sensitivity for sub-32 nm HP [1-3] and have prepared an EUV mask blank, fabricated in SEMATECH's MBDC, to be inspected using the M7360 in the MBDC and the AIT at LBNL to compare the sensitivity of these tools. We prepared a mask blank with a real phase defect and then compared the detected image using the M7360 and AIT to explain why we need an actinic inspection tool for the mass production of EUV mask blanks. Most of the cost of ownership (COO) of EUV masks depends on the defect-free mask blank cost. Consequently, defect mitigation technology using mask blanks with some phase defects should be developed to reduce mask blankcosts during mass production. In this paper, we identify what is needed for defect mitigation technology and propose possible defect inspection scheme for EUV pilot line applications [4].

There are three ways to perform mask defect inspection after absorber patterning:

First: DUV pattern inspection → Repair → Aerial image inspection review → Wafer fab.

Second: DUV pattern inspection → Repair → Wafer fab. → Mask printing on the wafer

Third: Actinic pattern inspection → Repair → Aerial Image Inspection review → Wafer fab.

Commercial actinic pattern inspection tools should be developed. However, they will likely have a high COO. A DUV inspection tool would be applicable to both optical and EUV masks, but this tool cannot see phase defecs on EUV masks. We need additional defect verification tool using a small field EUV imaging microscope.

2. MASK BLANK INSPECTION TOOL IN SEMATECH

A defect inspection tool for EUV mask blanks is the key enabler for many technology developments, such as defect-free blank fabrication, cleaning, and masks handling. SEMATECH's MBDC has provided the world's best defect inspection capability with the Lasertech M1350 tool using a 488 nm wavelength in 2003, followed by a second generation inspection tool, yhe Lasertech M7360 using a 266 nm wavelength. The lower wavelength of the M7360 provides a great improvement in detection capability than the M1350. However, there is a large gap in supporting mask blanks for the 32 nm half-pitchHP. Improved sensitivity for smaller defects could be achieved with a higher laser power, shorter wavelength, and various technologies that can cover multilayer inspection for the 32 nm half-pitch node. However the photon energy absorbed on the multilayer can damage reflectivity in the EUV wavelength. Moreover, a DUV light source cannot provide information about phase defect inside of multilayer films. Substrate inspection can be supported with a DUV inspection tool based on the current mask blank inspection tool. Additionally, we need an at-wavelength inspection tool for multilayer inspection. SEMATECH has operated the AIT as a defect inspection tool and imaging tool at LBNL. Before 2008, only one zoneplate with a numerical aperture (NA) of 0.00625 on the mask was available for imaging. After an upgrade in 2008, five user-selectable zoneplates were implemented, with magnifications of 680, 907, and 1000X and NAs of 0.00625, 0.075, and 0.0875 on the mask. These NAs emulate a 4X EUV scanner with NAs of 0.25, 0.3, and 0.35. It is possible to study EUV mask technology down to the 22 nm half-pitch without wafer printing using the upgraded SEMATECH–LBNL AIT now. Figure 1 shows the improvements in contrast and minimum resolution after the upgrade. We can clearly see the programmed absorber defect between lines.

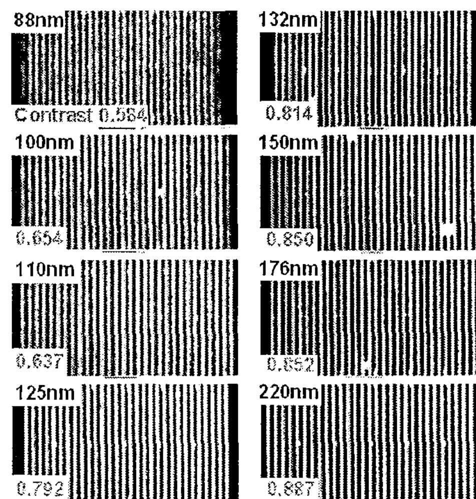


Figure 1. Minimum resolution after upgrade results in 2008

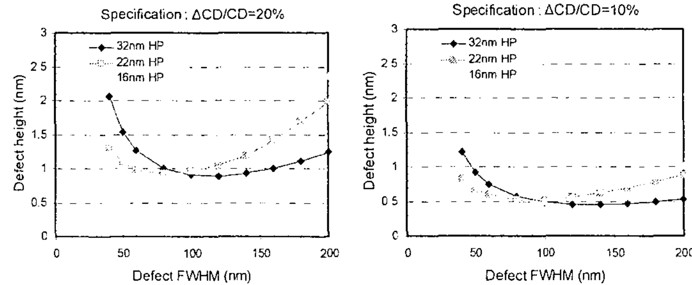
3. EXPERIMENTAL

3.1 Phase defect simulation

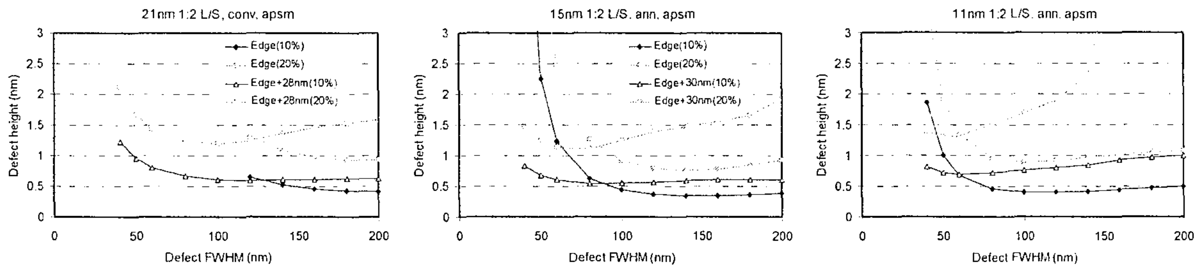
We simulated phase defect printability as a function of defect full width half maximum (FWHM) and height in a 1:1 L/S and 1:2 isolated line pattern in 32, 22, and 16 nm node devices [5]. Table 1 show the simulation condition used. The simulations cover different mask types (binary mask/phase shift mask) and illumination conditions (conventional and annular).The assumption of a multilayer profile is congruent as the phase defect profile. If there is smoothing or decorating during multilayer deposition, the simulation results can be different. We also used a constant threshold model; the resist effect is not considered in the simulation. Simulation results of phase defect printability for 1:1 dense L/S and 1:2 isolated line is shown in Figure 2. The criterion for defect printability is 10% CD variation in each line. The minimum defect FWHM is ~40 nm at a height of 0.5 ~ 1 nm. Defect height has a greater influence on CD variation than defect height. If the phase defect is away from the main pattern, it is also less printable than when it is adjacent to the pattern. This means that the phase defect specification should be much tighter in dense patterns than isolated patterns. The inspection capability to detect these types of substrate defects does not yet exist. Table 2 shows the required specifications for phase defect inspection.

Table 1. Simulation condition for defect printability

Node	32 nm	22 nm	16 nm
NA	0.25	0.35	0.45
Line: Space	32:32 / 21:42	22:22 / 15:30	16:16 / 11:22
Illumination condition	conventional (σ 0.5)	conventional (σ 0.5) Annular (σ 0.3/0.5)	conventional (σ 0.5) Annular (σ 0.3/0.5)



(a) Phase defect simulation in a 1:1 L/S



(b) Phase defect simulation in a 1:2 isolated line

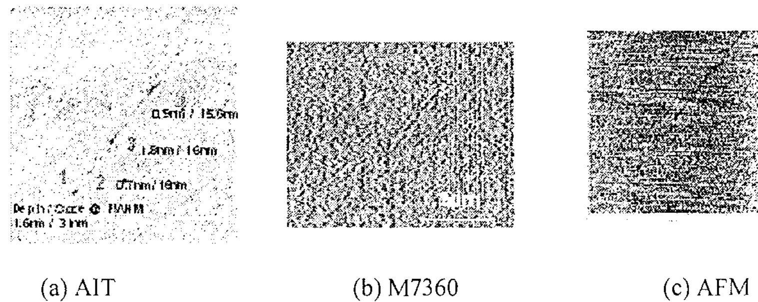
Figure 2. The simulation of phase defect printability

Table 2. Required sensitivity for phase defect inspection.

			3 ranges of defect widthw [FWHM]		
			40~50	50~70	>70
CD variation on wafer	32 nm half-pitch	10%	1.1	0.6	>0.5
		20%	1.7	1.2	>0.9
	22 nm half-pitch	10%	0.7	0.5	>0.5
		20%	1.2	0.9	>1
	16 nm half-pitch	10%	0.6	0.5	>0.5
		20%	0.9	0.8	>1

3.2 Comparison of M7360 and AIT

A test multilayer reticle blank was prepared in SEMATECH's MBDC and inspected using the M7360 at the most sensitive inspection condition to capture the smallest defect on the blank. This blank was then inspected with the AIT in LBNL using scanning and imaging modes. The images are shown in Figure 3 and demonstrate that the AIT can see details of the blank defect that are not detected by the M7360. The AIT shows that the scratch defect is composed of a series of pit defects and tails. It can also capture any phase defect less than 1 nm deep. This means that an actinic inspection tool will need to detect this kind of small and shallow defect during the pilot line phase.

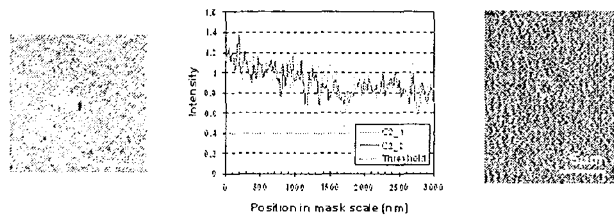


(a) AIT (b) M7360 (c) AFM

Figure 3. Image comparison using AIT and M7360

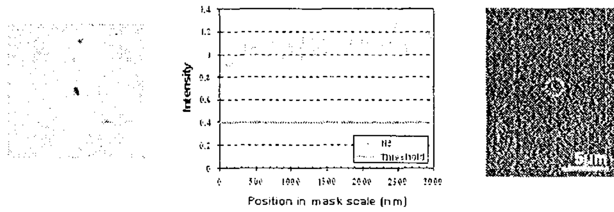
We inspected a total of 16 natural defects on an EUV mask blank using the M7360, AIT, and atomic force microscope (AFM) to study the printability of real defects. Five examples are shown in Figure 4. If the intensity of a phase defect captured by the AIT is higher than the threshold, it will be printed on the wafer. From the simulation results in section 2, we set a printable threshold value of 0.4. The shape of the real defect is arbitrary and very different from PDM and Gaussian profile in the simulations. The N3 defect in Figure 4(a) is 3.0 nm deep. However, the aerial image signal is higher than the threshold value, which means that this defect will not print if it is on the clear field, not between the lines. Even if the depth of the C2_1 defect in Figure 4(b) is shallower than N3, if its intensity is almost down to the threshold value, this kind of phase defect will be printed. The AIT detected the C2_2 defect, which is not detected by the M7360 and AFM. However, this defect will not print in the open field. The N1 defect looks like a scratch defect as imaged by the M7360 in Figure 4(c). However, the scratch defect is composed of four pits and tails and is very shallow and small as in the image from the AIT. The intensity of the scratch N1 defect is higher than 0.4. The defect in L2 is smaller and shallower than C2; however, its intensity drop is almost same. This means that real defect has a very different printability and profile than the programmed defect.

Figure 5 shows information about nine phase defects on the clear field using the AIT and AFM. If the phase defects are located between the lines, the minimum defect FWHM we need to be concerned about is ~40 nm at a height of 0.5 ~ 1 nm with 10% CD variation. On the contrary, clear field printability increases the printable defect size to between 0.7 and 3.5 nm if the defect is far away from the pattern. We need more real defect printability data to improve statistics and our understanding.

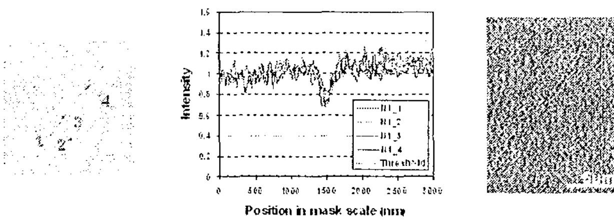


AIT Cross sectional image M7360

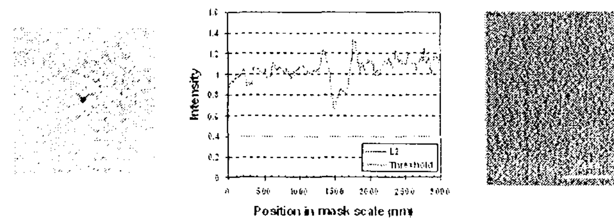
(a) N3 (FWHM 23.4 nm/depth 3.0 nm)



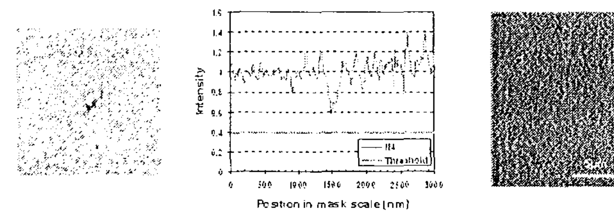
(b) C2 (FWHM 31.5 nm/depth 2.4 nm)



(c) N1_1 (FWHM 31.25 nm/depth 1.8 nm), N1_2 (FWHM 15.6 nm/depth 0.7 nm)
N1_3 (FWHM 21.2 nm/depth 1.8 nm), N1_4 (FWHM 29.2 nm/depth 0.9 nm)



(b) L2 (FWHM 15.7nm/depth 2.1nm)



(e) C2 (FWHM 33.4nm/depth 3.4nm)

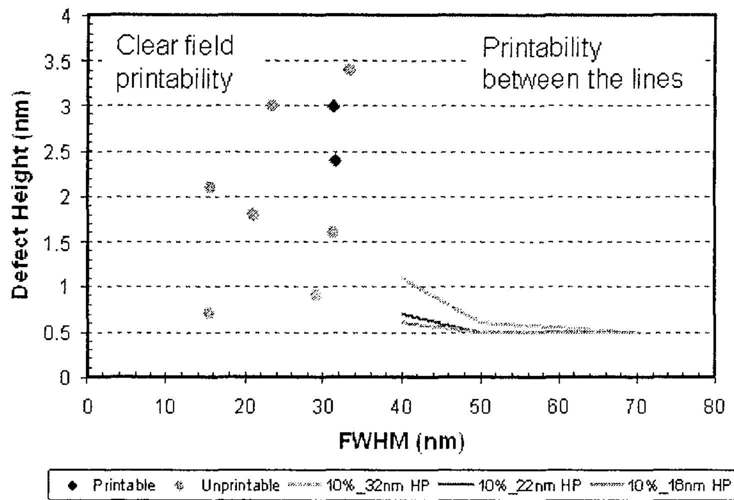


Figure 5. Summary of phase defect printability in the clear filed

4. DEFECT MITIGATION TECHNOLOGY

4.1 The species of various defects on EUV masks

There are various defects, such as substrate defects, multilayer defects, and absorber defects, on the EUV mask shown in Figure 6. As we discussed in phase defect simulation, defect printability is a function of not only defect profile, but also defect location. We need to categorize which kind of defect is printable using a database; we do not have to be concerned about unprintable defects. In the ITRS, the requirement for phase defects is 0.003/cm^2 for HVM production . However, maintaining a high yield with such a defect level will be difficult. It also will increase mask blank cost drastically. We must take advantage of mask blanks with some defects if we can make phase defects unprintable using defect mitigation technology. We can make a printable defect-free mask, not a defect-free mask with defect mitigation technology. Table 3 shows the requirements for fiducial marks for mask fabrication and application.

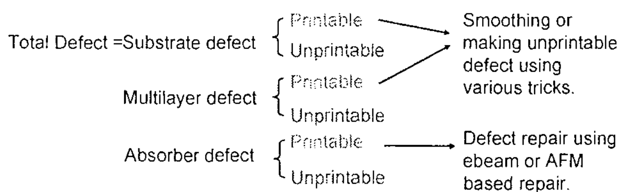


Figure 6. The species of defect in EUV mask

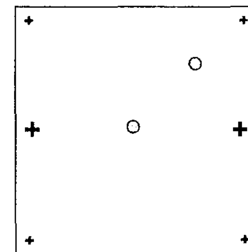


Figure 7. Fiducial mark on EUV mask blank

4.2 Fiducial marks on the multilayer

We need to get all defect information about size and exact coordination to create a defect mitigation technology. There should be a fiducial mark on the multilayer to extract the relative coordination of each defect (see Figure 7). After mask blank inspection, we need to get all necessary information about each phase defect so that we can define which kind of defect is printable or which is not. Because phase defects under the absorber or open field are less likely to print on the wafer, any shift and rotation of the blank with regard to the phase defect before e-beam writing can hide the phase defect on the blank if there are fiducial marks on the blank. Mask shops sort for layer use by

defect numbers (Figure 8). For example, a mask blank with some phase defects can be used for contact array patterns, moderated defects for metal layers, and a few defects for gate layers.

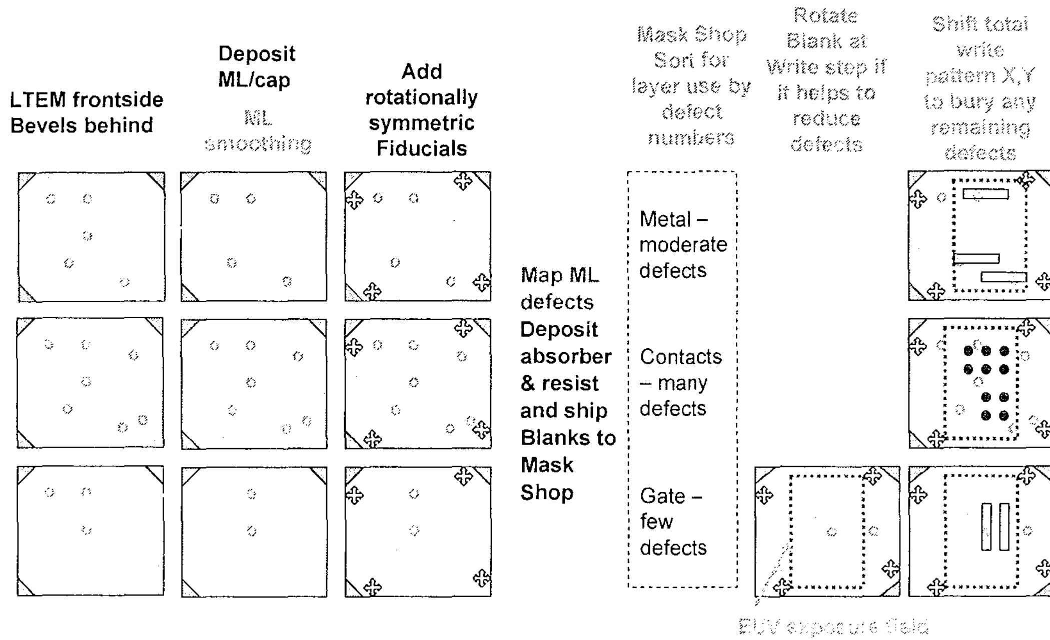


Figure 8. Summary of defect mitigation technology

Table 3. Requirements for fiducial marks

Defect location identification	Readable by blank defect inspection tool
For e-beam patterning defect mitigation	Readable by e-beam wiring tool for pattern alignment Blank rotation & shift as mask data
For mask proximity repair	Readable by repair tools
For final defect printability verification	Readable by EUV small field inspection tool, metrology or other inspection tool
EDA	Find best writing alignment from defect information & mask data

4.3 Mask fabrication process considering fiducial mark

A mask fabrication process considering fiducial marks and the required inspection tool is shown in Figure 9. We need to develop the next generation substrate inspection tool (2.5G), actinic blank inspection tool (3G), and small field aerial image microscope. SEMATECH is pursuing the following actions to attempt to meet defect metrology requirements. The tool is absolutely critical for the industry to stay on the mask blank defect reduction roadmap to meet 32 nm HP targets:

- Continued improvements to second generation visible light inspection tools. The Lasertec M7360 should get us to 30-35 nm sensitivity for pilot line applications.
- Drive a 2.5 generation tool – visible light inspection extension with 20 nm sensitivity.
- Drive a 3 generation tool - actinic inspection.

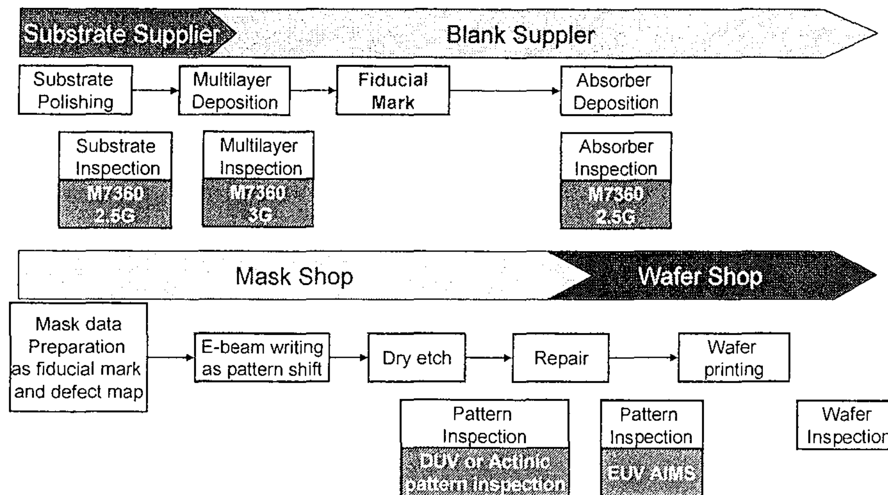


Figure 9. Mask fabrication process and required inspection tool

4.4 Possible defect verification method.

If a proper inspection tool cannot be developed for pilot line applications around 2010, we have no choice but to take advantage of our current inspection tool and print wafers on an EUV scanner to verify defect printability.

- First: DUV pattern inspection → Repair → Aerial image inspection review → Wafer fab
- Second: DUV pattern inspection → Repair → Wafer fab → Mask printing on the wafer
- Third: Actinic pattern inspection → Repair → Aerial Image Inspection review → Wafer fab

Phase defects present a significant challenge to mask inspection. In the first method, phase defects cannot be detected in a mask shop, but will be detected in the wafer fab. In contrast, phase defects can be detected in the wafer fab before device manufacturing using the second method. However, the third method is the best strategy for qualifying EUV masks. Using EUV wavelength inspection, both absorber and phase defects can be detected in the mask shop, and the qualified mask can be transferred to the wafer fab.

5. CONCLUSION AND FUTURE WORK

Reducing defects on EUV mask blanks is a key technology for EUV lithography used in mass production. In this paper, we studied phase defect printability for the 32/22/16 nm half-pitch. Because phase defects 0.5 nm high can print, we need an inspection tool to detect such shallow defects in EUV mask blanks. Because it will be difficult to obtain a high yield with a defect density of 0.003/cm^2 in the mass production stage, a defect mitigation technology using mask blanks with some phase defects should be developed to maintain a low cost of ownership for EUV masks. Fiducial marks need to have exact information about each defect on the mask blank. Actinic mask blank defect inspection and aerial imaging tools are key to enable yielding masks for the 32 nm hp. SEMATECH, in collaboration with industry, is making programmed phase defect masks to study the printability of phase defects using the microexposure tool (MET), AIT, and alph demo tool (ADT).

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