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Research Article

Master-Slave Topologies with Phase-Locked Loops

José Roberto C. Piqueira

Escola Politécnica da Universidade de São Paulo, Avenida Prof. Luciano Gualberto, Travessa 3, n. 158, 05508-900 São Paulo, SP, Brazil

Correspondence should be addressed to José Roberto C. Piqueira; piqueira@lac.usp.br

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Since phase-locked loops (PLLs) were conceived by Bellescize in 1932, their presence has become almost mandatory in any telecommunication device or network, being the essential element to recover frequency and phase information. As the technology developed, PLL appeared in several applications, such as, dense communication networks, smart grids, electronic instrumentation, computational clusters, and integrated circuits. In all of these practical cases, isolated or networked PLLs are responsible for recovering the correct time basis and synchronizing the processes. According to the application needs, different clock distribution strategies were developed, with the master-slave being the simplest and most used choice. Considering that the master clock is obtained from a stable periodic oscillator, two topologies are studied: one-way, not considering clock feedback; and two-way master-slave, with the slave nodes providing clock feedback to the master. Here, these two cases are studied by using simulation strategies, presenting results about the clock signal recovery process in the presence of disturbances, indicating that master-slave clock distribution networks can be useful for networks with few nodes and a stable master oscillator with the one-way topology presenting better results than the two-way arrangement.

1. Introduction

Phase and frequency synchronization problems have been present in electronic engineering since the first coherent modulation systems were developed, with the phase-locked loop implemented by using discrete components, performing the important function of detecting the time basis coming from a remote point [1].

When television systems were conceived, vertical and horizontal signals must have been synchronized by a periodic pulse, a function implemented by using the PLL architecture [2]. For the development of color television, PLL was essential for synchronizing color beams [3].

Essentially, all of these PLL systems were a closed loop composed of a phase detector (PD), a filter (F), and a voltage-controlled oscillator (VCO), as shown in Figure 1. The PD compares the phase of the input signal, $v_i(t)$, coming from a remote point, with the phase of the local (VCO) oscillation, $v_o(t)$, producing an error signal that is filtered and controls the phase of the VCO signal.

Around 1965, the first PLL-integrated circuits appeared, with all parts implemented with analogical components and with very low cost due to the wide range of their applications [4, 5]. The digitalization of the PLL functions started in 1970 with the PD implemented by an exclusive or (X-OR) or charge pump circuit, presenting good performance [6].

These developments were simultaneous to the digitalization of the telecommunication networks, in which all of the standard solutions are supposed to have synchronized time signals exchanged between the nodes [7–9].

With the development of the integrated services, the tendency towards the digitalization of all network devices became mandatory, and the PLL, in spite of following the same Bellescize architecture, improved the manner of processing signals, originating the digital PLL (DPLL) circuits and converting the VCO function into digital [6, 7, 10].

As a consequence of the strong development of integrated circuits and digital filtering [11], the entire PLL started to be implemented by using flexible architectures, with adequate signal processing functions digitally

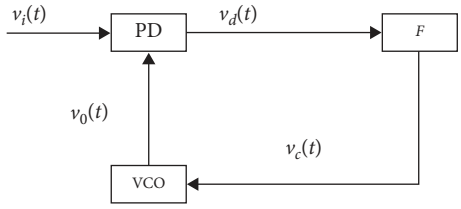


Figure 1: PLL block diagram.

implemented, generating the all-digital PLL (ADPLL) circuits, which is an important component of the new generation of wireless devices and dense communication networks [12, 13].

This evolution allowed software-implemented PLLs [4, 11], with connected PLL nodes starting to share the same electronic device. Consequently, to satisfy the rapid internal signal processing, fast synchronization is needed to guarantee precise time basis at the several electronic levels: chips, circuits, systems, and large distributed networks [14].

PLL networks currently play an important role in precision electronic instrumentation [15], power distribution smart grids [16], computational clusters [17], and integrated circuits [14, 17]. In all of these practical cases, isolated or networked PLLs are responsible for the correct recovering of time basis, synchronizing the processes.

Therefore, largely studied synchronization architectures [4, 5, 18], with implementations present in almost all telecommunication networks or devices [7, 19, 20], are demanded to be restudied to permit adequation analysis in each case, mainly due to the role played by nonlinearities and perturbations in the context of low-level signal propagation.

Here, master-slave synchronization architectures are studied with all PLL nodes following the model presented in Figure 1, i.e., considering that a phase detector compares the phases of two periodic signals, one coming from the outside, with θ_i being the phase of $v_i(t)$, and the other, from an internal oscillator, with θ_o being the phase of $v_o(t)$, with the output $v_d(t) = v_i(t) \cdot v_o(t)$.

As shown in [4, 6], if these inputs are in quadrature, the PD output $v_d(t)$ is proportional to the phase error $\phi = \theta_i - \theta_o$ with the addition of a double-frequency term. The filter is supposed to eliminate the double-frequency term, generating the signal $v_c(t)$that controls the VCO phase, according to $\dot{\theta}_o = K_0 \cdot v_c(t)$.

In this study, two definitions of synchronous state are presented: phase synchronization and frequency synchronization, considering the main case of interest for electrical circuit applications.

Definition 1. A phase-locked loop with an architecture shown in Figure 1 is in a phase synchronous state, for a time interval (t_1, t_2), if its phase error $\phi = \theta_i - \theta_o = 0$, $\forall t \in (t_1, t_2)$.

Definition 2. A phase-locked loop with an architecture shown in Figure 1 is in a frequency synchronous state, for a time interval (t_1, t_2), if its frequency error $\dot{\phi} = \dot{\theta}_i - \dot{\theta}_o = 0$, $\forall t \in (t_1, t_2)$.

In the Section 2, a single-node second-order PLL is adjusted, and the several cases of synchronization and nonsynchronization are described and simulated. Then, a one-way master-slave (OWMS) architecture [8, 21], with three slave nodes, is simulated, showing the several possible behaviors of the time basis propagation. To give some comparison ideas, a two-way master-slave (TWMS) architecture [8, 21] is studied.

It is shown that the use of master-slave architectures must be restricted to not too long networks, with OWMS presenting better performance than TWMS under perturbations.

2. Single-Node Simulations

2.1. Adjusting the Node. All the simulations conducted here use the PLL block from the "Communications Systems Toolbox," built in the MatLab-Simulink version R2015a [22] because it follows the mathematical model described in [23] and is compatible with the problem discussed here [24–26].

To work with normalized results, the PLL block was adjusted with the following parameters:

(i) PD gain = 1;

(ii) Filter transfer function = $1/(s + 2)$;

(iii) VCO central frequency = $2 \cdot \pi$ rad/s;

(iv) VCO initial phase = 0;

(v) VCO gain ($K_0 = 1$).

The PD input signal, $v_i(t)$, is periodical with unitary amplitude and was adjusted with frequency $2 \cdot \pi$ rad/s and initial phase equal to zero. The simulation result was mathematically expected [23], i.e., presenting phase synchronization between the PD input signal, $v_i(t)$, and the VCO output, $v_0(t)$.

The Lissajous figure shown in Figure 2 is generated by the combination of the PD input signal, $v_i(t)$, in the x-axis, and the VCO output, $v_0(t)$, in the y-axis. The circle, obtained after a transitory, indicates that the PD input ($v_i(t)$) and VCO output ($v_0(t)$) are periodic signals, with the same frequency and phases in quadrature, implying synchronization.

2.2. Phase Step. By using the formerly adjusted PLL block, the single-node behavior was studied, considering a phase step. The simulation procedure uses the same circuit formerly described, and a constant phase step was added to the phase of $v_i(t)$.

Two different simulations were conducted: for steps equal to $\pi/12$ (Figure 3(a)) and $\pi/2$ (Figure 3(b)).

As the second-order PLL is insensitive to phase steps [4, 6, 23], the Lissajous figures generated by the combination of the PD input signal, $v_i(t)$, in the x-axis, and the VCO output, $v_0(t)$, in the y-axis result in circles, i.e., PD input ($v_i(t)$) and VCO output ($v_0(t)$) in quadrature, indicating phase synchronization. An additional transitory interval appears caused by the step starting that occurred at $t = 5$ s.

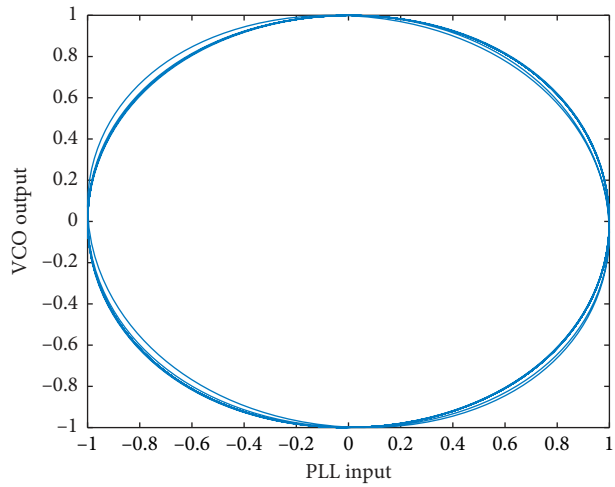


Figure 2: Adjusting the PLL single node.

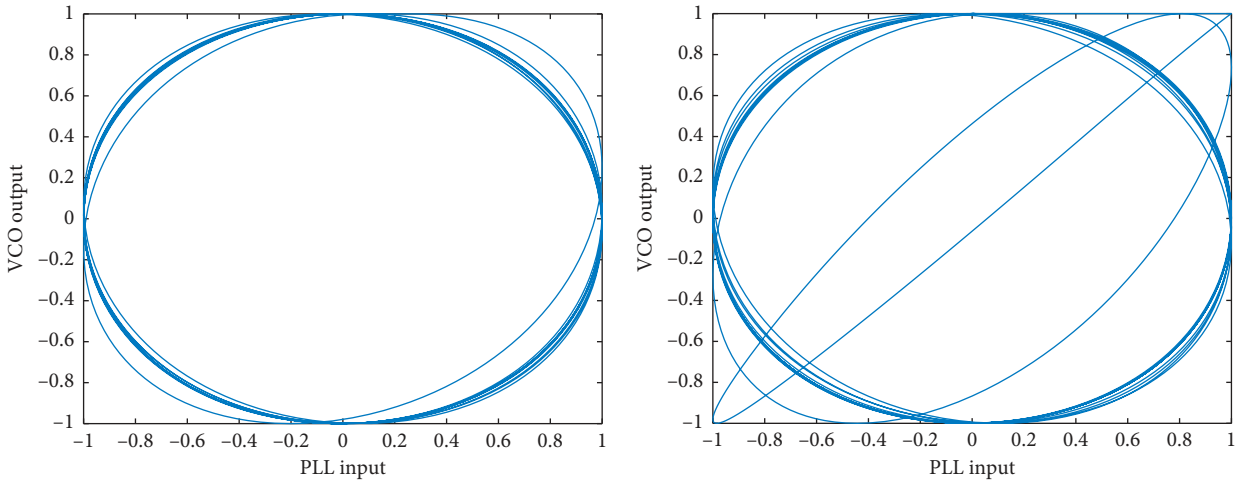


Figure 3: Phase step in a single-node PLL; (a) $\pi/12$ rad and (b) $\pi/2$ rad.

2.3. Phase Ramp. Considering that the time constant of the filter is $\mu_1 = 2$ s and applying a ramp perturbation with inclination $\Omega < 2$ to the PD input ($v_i(t)$), in spite of not having phase synchronization [23], the node captures the frequency synchronization with a constant phase error, as Figure 4(a) shows for $\Omega = 1$, with the Lissajous figure generated by the combination of the PD input signal, $v_i(t)$, in the x-axis, and the VCO output, $v_0(t)$, in the y-axis resulting, after a transitory, in an ellipse with inclined axis, indicating oscillations with the same frequency but different phases.

Increasing the ramp inclination ($\Omega = 1.5$), the transient interval increases, but the ellipse, in spite of being smaller, continues to be clearly the attractor (Figure 4(b)). For this point on, a small increase in the ramp inclination ($\Omega = 1.6$) almost destroys the attractor (Figure 4(c)).

For $\Omega \geq 2$, the frequency synchronization disappears. Consequently, when designing a network with the phase ramp input, the whole PLL gain ($K_0 \cdot \mu_1$) must be greater than the ramp derivative.

3. One-Way Master-Slave Network

Considering the adjusted components of the former section, a four-node single-chain master-slave architecture, with one master and three slave nodes, described in the Appendix, was implemented in the MatLab-Simulink version R2015a [22]. The periodic unitary amplitude input signal, adjusted with frequency $2 \cdot \pi$ rad/s with initial phase equal to zero, was considered to be the master signal that is sent to the PD input, $v_i(t)$, of the first slave.

The VCO output signal, $v_0(t)$, of the first slave is sent to the PD input of the second slave, whose VCO output signal is sent to the PD input of the third slave. As the PLL inputs and outputs must be in quadrature, 0.31 s transport delays must be considered between two adjacent nodes. As the master signal

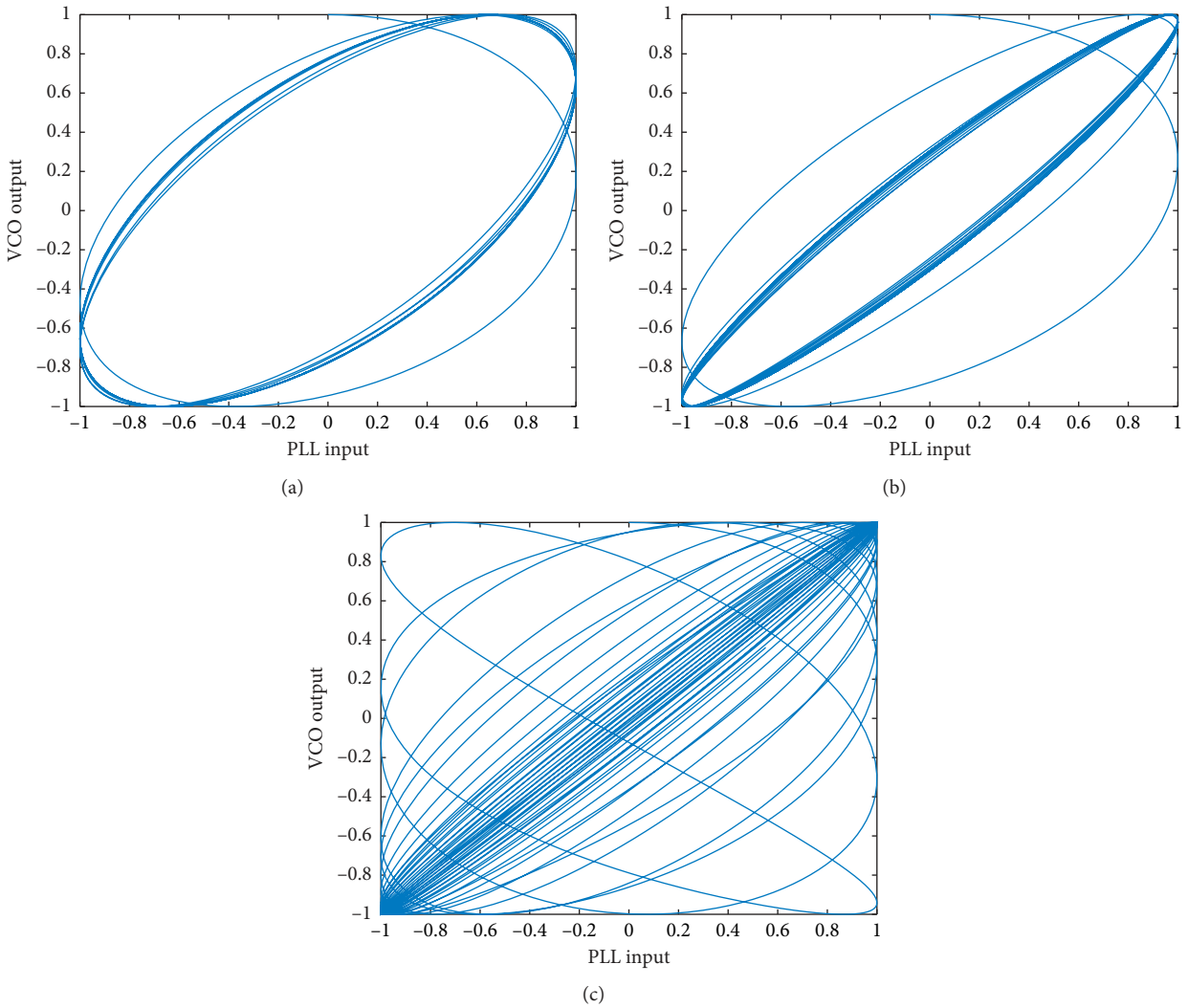


Figure 4: Phase ramp in a single-node PLL; (a) $\Omega = 1$, (b) $\Omega = 1.5$, and (c) $\Omega = 1.6$.

does not depend on the slave signals, this clock distribution strategy is called OWMS (one-way master-slave) [21].

3.1. Adjusting the Network. To test if the network was assembled in the correct way and the transport delays were well chosen, a simulation without perturbation was performed. The results comparing the node outputs with the master output are shown in Figure 5, for the three slaves. In the three cases, the Lissajous figures are generated, for each slave node, by the combination of the PD input signal, $v_i(t)$, in the x-axis, and the VCO output, $v_0(t)$, in the y-axis result, after a transitory, in circles. This fact indicates phase synchronization.

3.2. Phase Step Perturbation. Considering the OWMS network formerly implemented, a $\pi/2$ step perturbation was introduced into the master phase at $t = 5$ s, to study the effect of its propagation. The results are shown in Figure 6, with the Lissajous figures generated, for each slave node, by the combination of the PD input signal, $v_i(t)$, in the x-axis, and the VCO output, $v_0(t)$, indicating a transient desynchronization tending to a phase synchronization represented by a circle attractor.

However, observing Figure 6, it can be concluded that the farther the slave node is from the master, the longer is the transient desynchronization. This phenomenon is responsible for a strong limitation in the clock signal precision for long chains [8, 21, 24, 25].

3.3. Phase Ramp Perturbations. Considering that the time constants of all filters are equal to $\mu_1 = 2$ s, applying ramp perturbations with inclination $\Omega < 2$ to the master phase, in spite of not having phase synchronization [23] in the slave nodes, frequency synchronization occurs, as the Lissajous figures are generated, for each slave node, by the combination of the PD input signal, $v_i(t)$, in the x-axis, and the VCO output, $v_0(t)$, as shown in Figure 7 for $\Omega = 1.0$ ramp.

It can be observed that, before the frequency synchronization capture, a large nonsynchronized transient interval appears and, consequently, applications demanding short

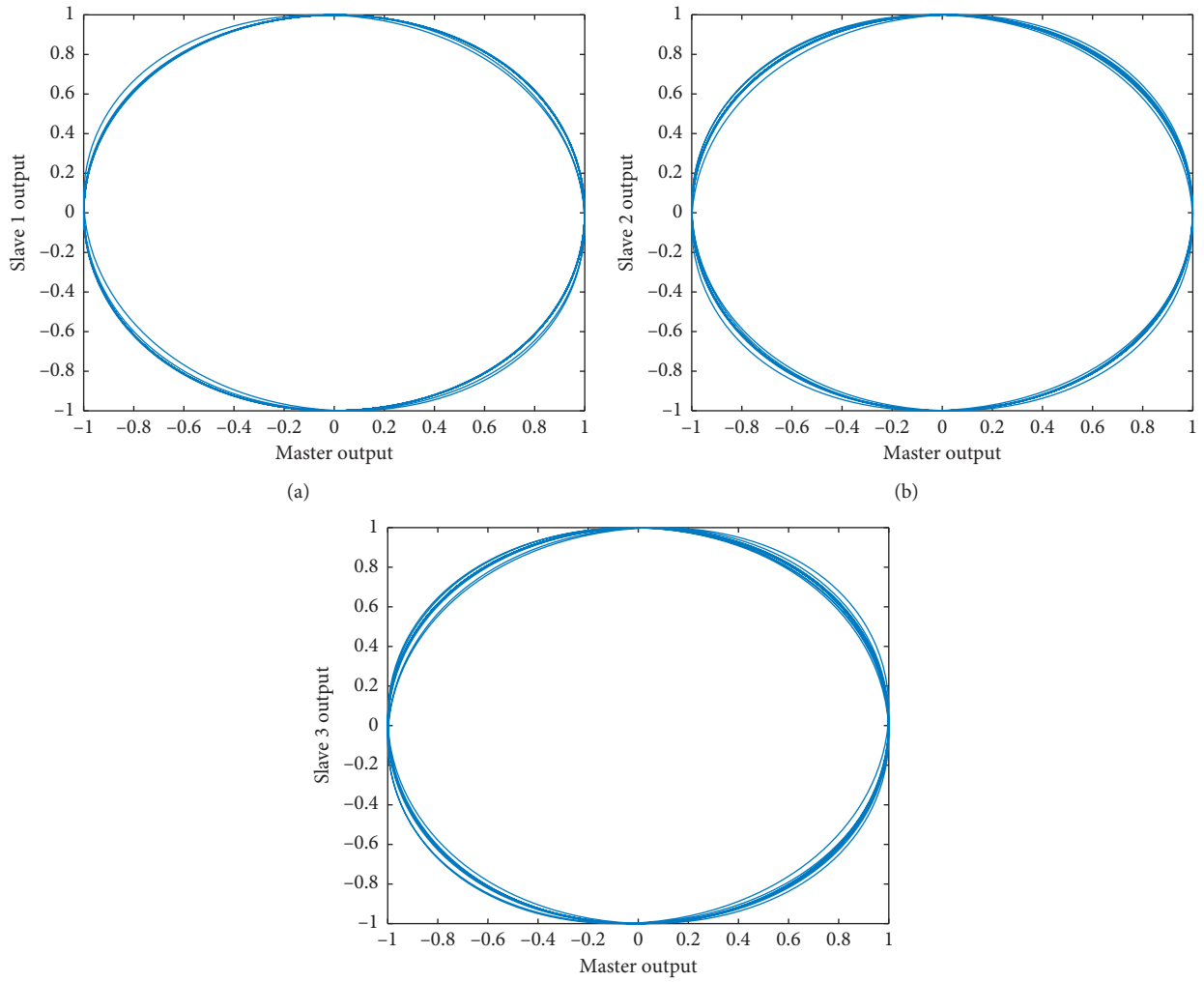


Figure 5: Unperturbed OWMS time basis comparisons; (a) Node 1, (b) Node 2, and (c) Node 3.

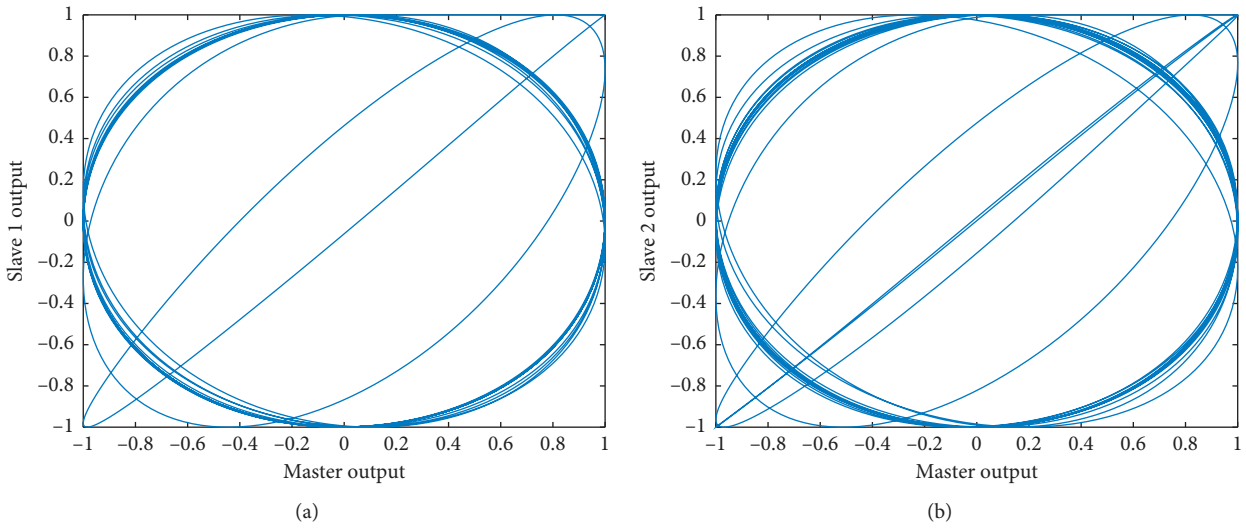
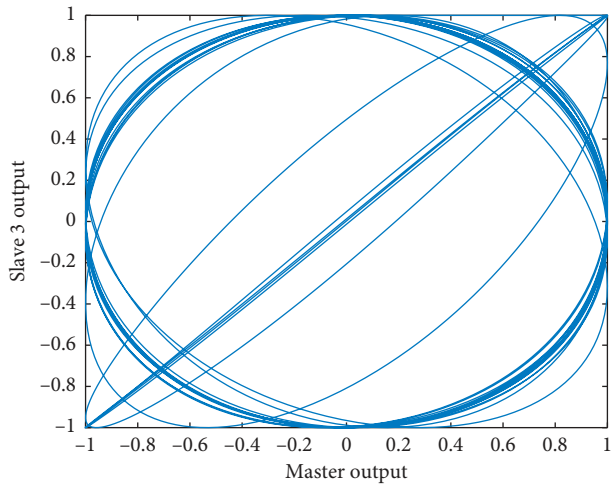
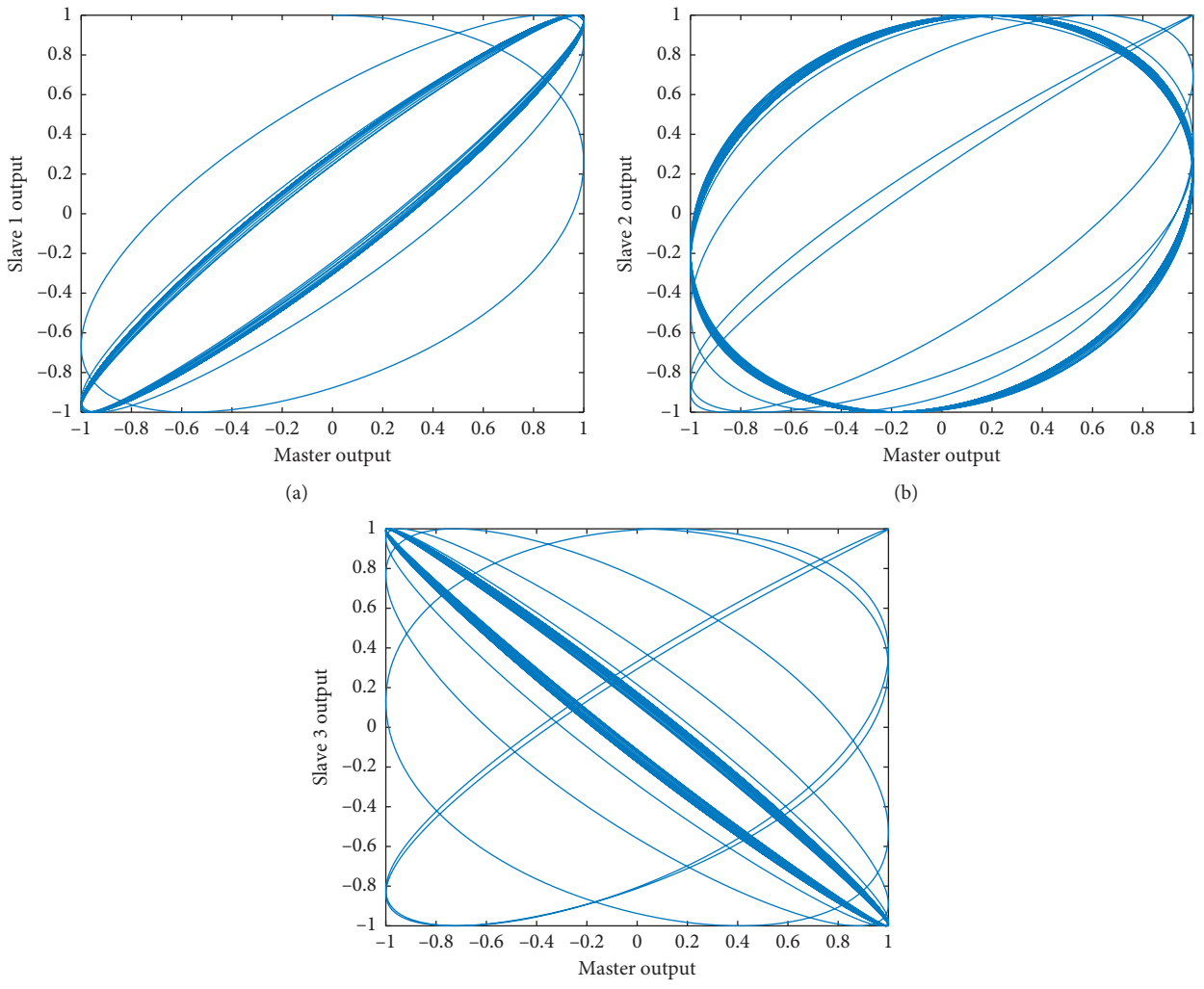


Figure 6: Continued.



(c)

Figure 6: OWMS time basis perturbed by a $\pi/2$ phase step; (a) Node 1, (b) Node 2, and (c) Node 3.



(a)

(b)

(c)

Figure 7: OWMS time basis perturbed by $\Omega = 1.0$ phase ramp; (a) Node 1, (b) Node 2, and (c) Node 3.

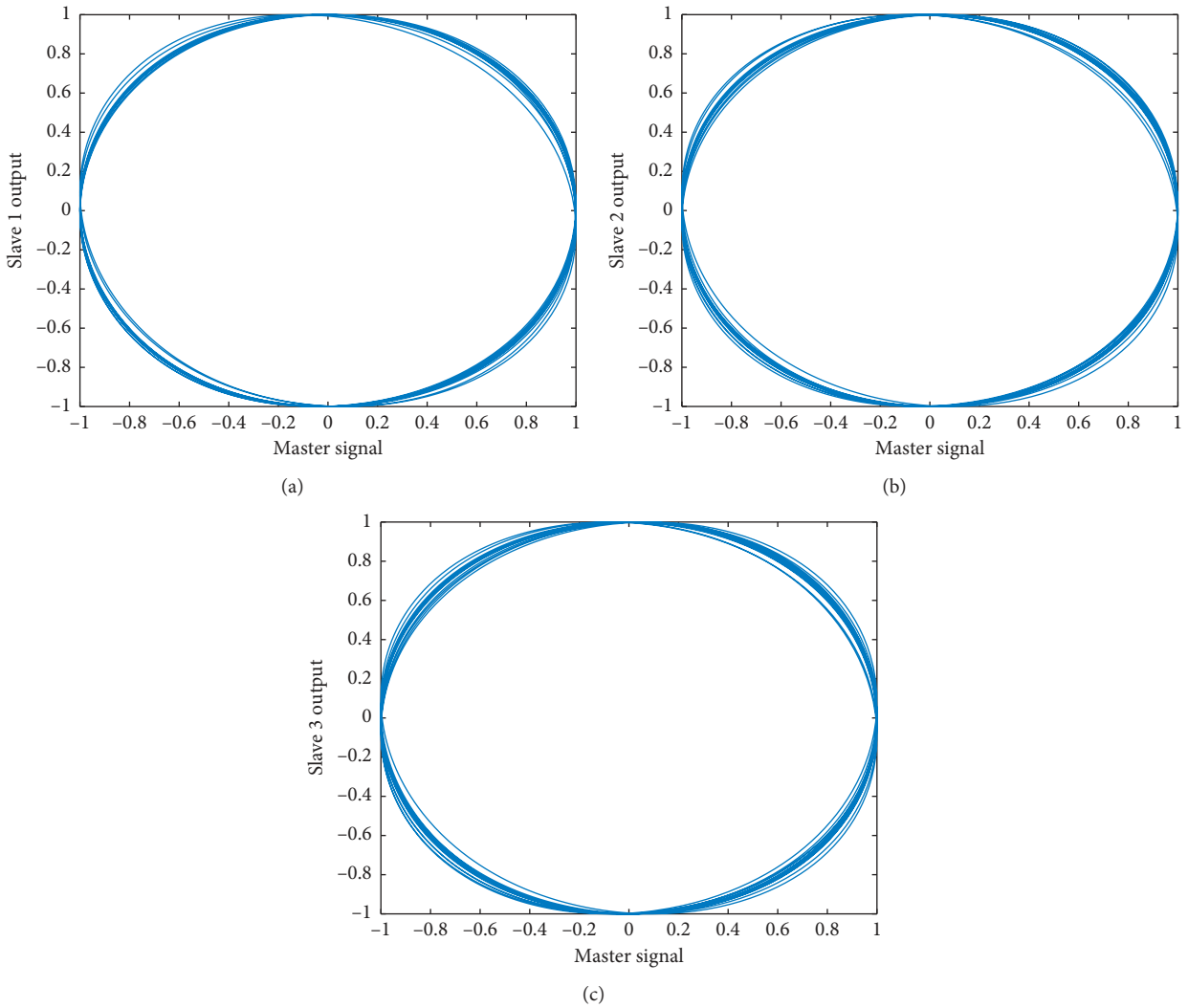


Figure 8: Unperturbed TWMS time basis comparisons; (a) Node 1, (b) Node 2, and (c) Node 3.

time responses and clock precision cannot use this type of architecture if a ramp perturbation is expected. Moreover, increasing the ramp inclination, even below the limit, this phenomenon occurs, being stronger for nodes more distant from the master, as it was shown in [24].

4. Two-Way Master-Slave Network

Considering the same components of the former sections, a four-node two-way master-slave architecture (TWMS), with one master and three slave nodes, described in the Appendix, was implemented. The periodic input signal, adjusted with frequency $2 \cdot \pi$ rad/s and initial phase equal to zero, was considered to be the master time basis. However, in this architecture, the signal sent by the master to the first slave considers the phases of the slave nodes as per the following equation:

$$\Phi_0 = 2 \cdot \Phi_M - \sum_{i=1}^{n} a_i \cdot \Phi_i, \quad (1)$$

with Φ_0 being the phase of the signal sent to the first node; Φ_M, the master natural phase; and Φ_i, the phase of the slave node i. Note that equation (1) results from a feedback term taking the slave phases into account, with $\sum_{i=1}^{n} a_i = 1$ [21].

The VCO output signal of the first slave is sent to the second slave node, whose VCO output signal is sent to the third slave. As the PLL inputs and outputs must be in quadrature, 0.31 s transport delays must be considered between two adjacent nodes. As the master signal depends on the slave signals, this clock distribution strategy is called TWMS (two-way master-slave) [21].

4.1. Adjusting the Network. To test if the network was assembled in the correct way and the transport delays well chosen, a simulation without perturbation was performed, considering $a_1 = a_2 = a_3 = 1/3$. The results comparing the node outputs with the master output are shown in Figure 8, for the three slaves. In the three cases, the Lissajous figures, built for each node combining PD input, $v_i(t)$, and VCO

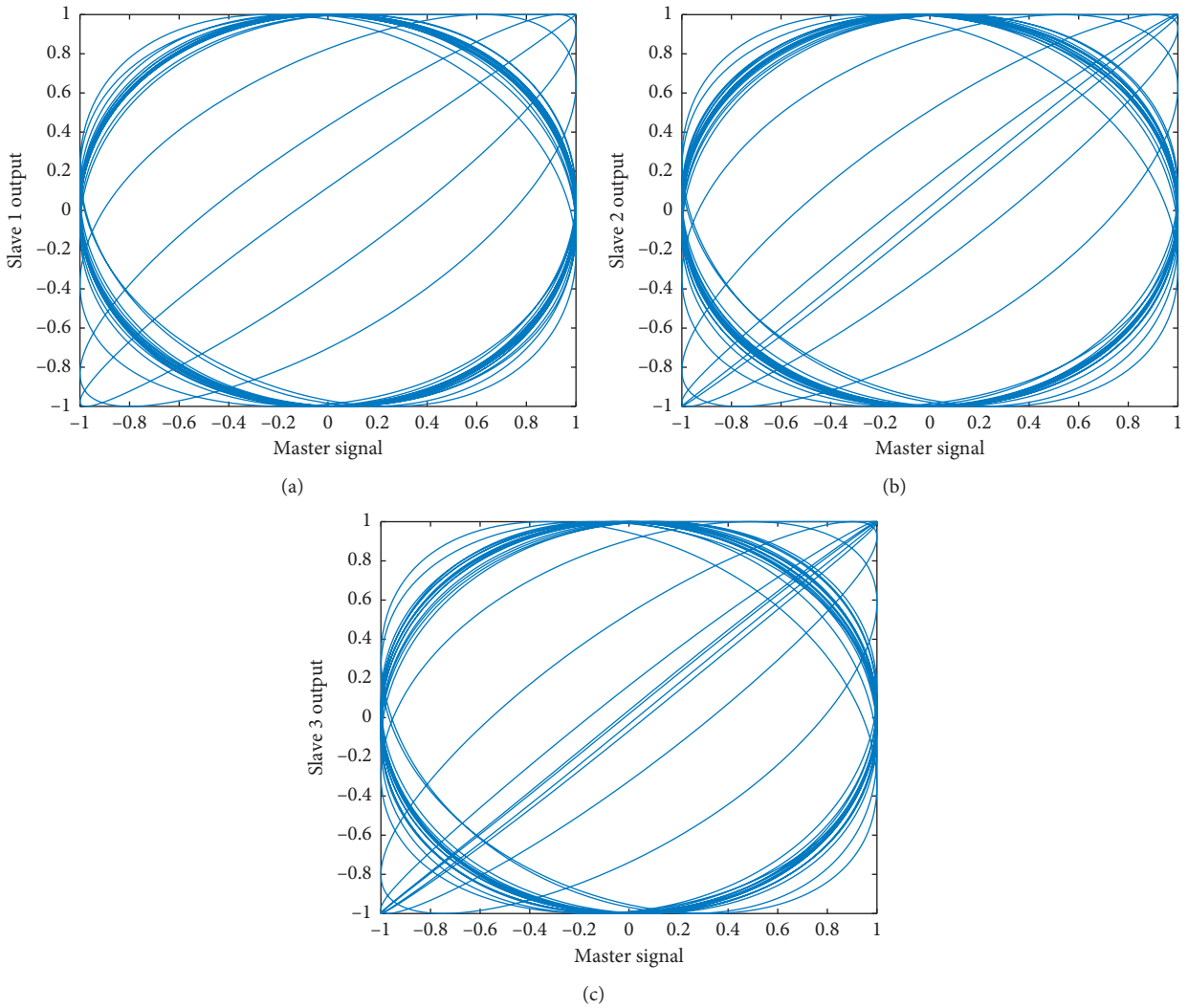


Figure 9: TWMS time basis perturbed by a $\pi/2$ phase step; (a) Node 1, (b) Node 2, and (c) Node 3.

output, $v_0(t)$, after a transitory time, are circles, indicating phase synchronization resulting similar to Figure 5 results.

4.2. Phase Step Perturbation. Considering the TWMS master-slave network formerly implemented, a $\pi/2$ step perturbation was introduced into the master phase at $t = 5$ s, to study the effect of its propagation. The results are shown in Figure 9 showing Lissajous figures, built for each node combining PD input, $v_i(t)$, and VCO output, $v_0(t)$, after a transitory time, which are circles indicating a transient desynchronization, worse than the OWMS case. After this transitory, phase synchronization is reached, as shown by the circle attractor.

Observing Figure 9, it can be concluded that the farther the slave node is from the master, the longer is the transient desynchronization. This phenomenon is responsible for a strong limitation in the clock signal precision for long chains, similarly to the same situation in the OWMS architecture [8, 21].

4.3. Phase Ramp Perturbations. Considering that the time constants of all filters are equal to $\mu_1 = 2$ s, applying ramp perturbations with inclination $\Omega < 2$ to the master phase, in spite of not having phase synchronization [23] in the slave nodes, frequency synchronization occurs, as the Lissajous figures are generated, for each slave node, by the combination of the PD input signal, $v_i(t)$, in the x-axis, and the VCO output, $v_0(t)$, shown in Figure 10 for $\Omega = 0.5$ ramp.

As in the OWMS case, it can be observed that, before the frequency synchronization capture, a nonsynchronized transient interval appears in the TWMS, slightly shorter than that observed in the OWMS. Consequently, even for the TWMS strategy, applications demanding short time responses and clock precision cannot use this type of architecture if a ramp perturbation is expected.

Increasing the ramp inclination, even below the limit, this phenomenon is too strong for the TWMS strategy, as Figure 11 shows for $\Omega = 1.0$ with the lost of frequency synchronization.

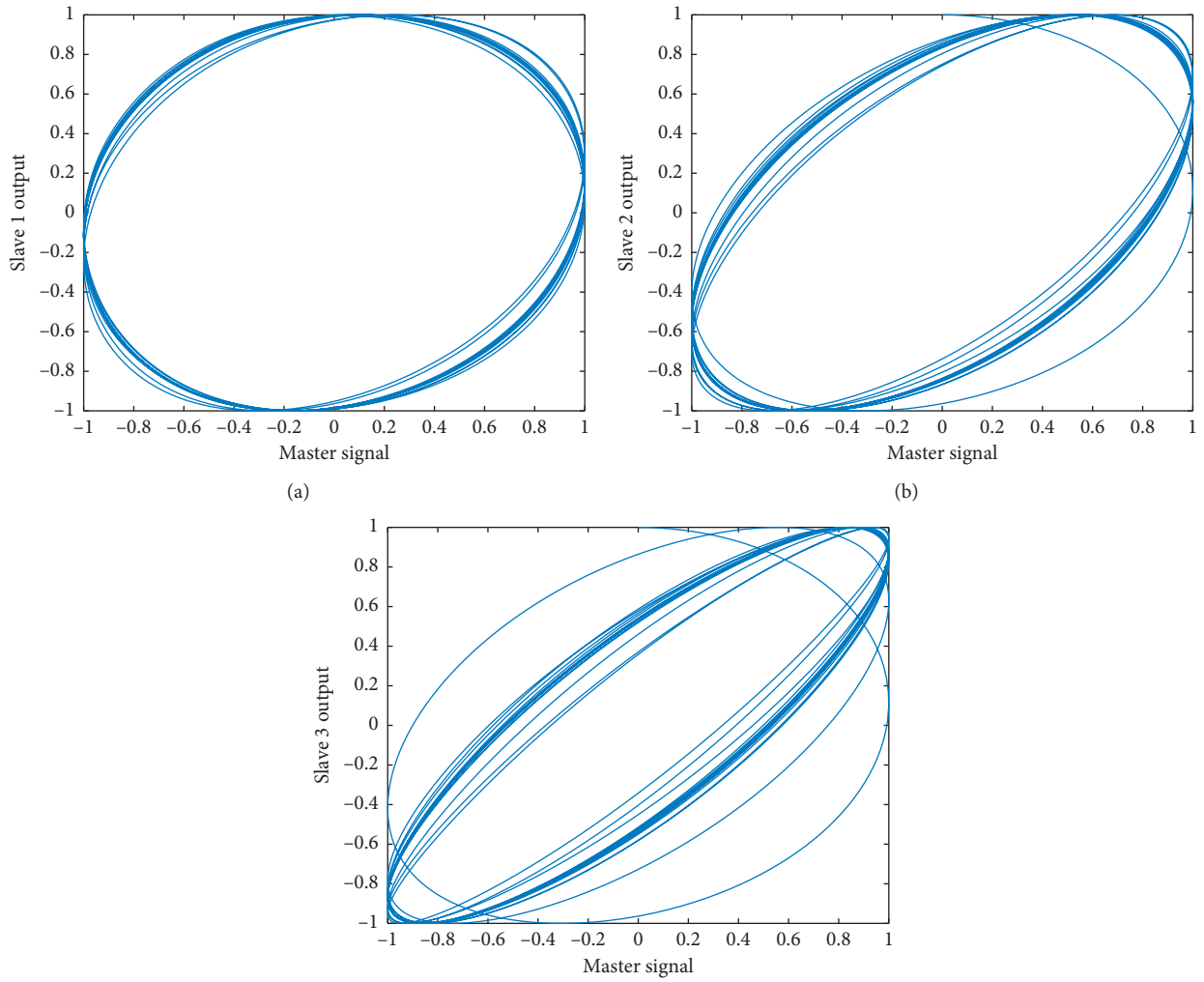


Figure 10: TWMS time basis perturbed by $\Omega = 0.5$ phase ramp; (a) Node 1, (b) Node 2, and (c) Node 3.

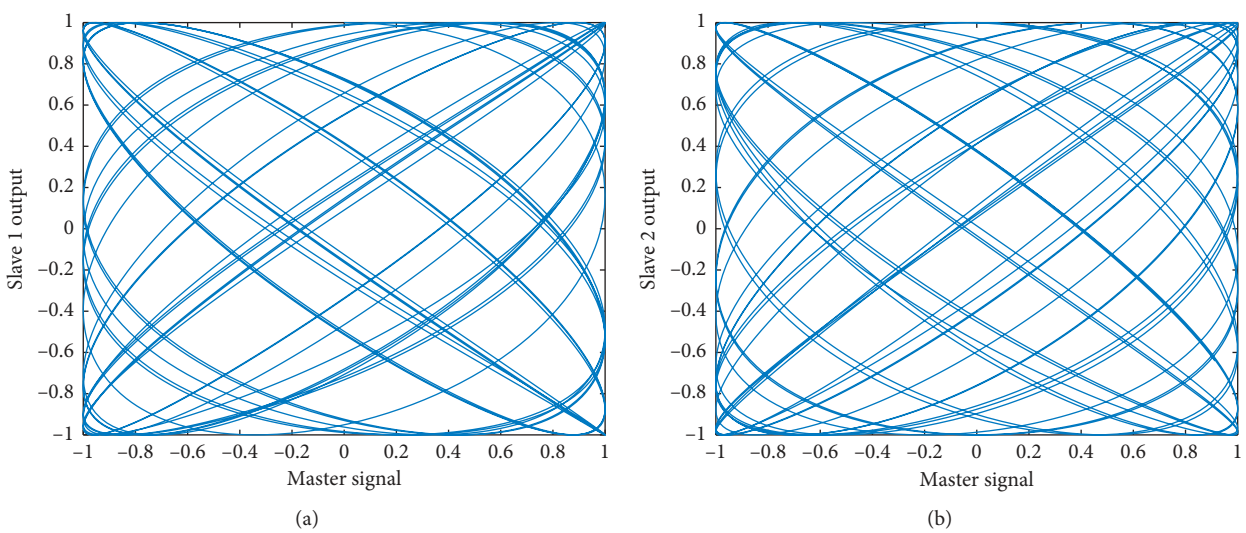
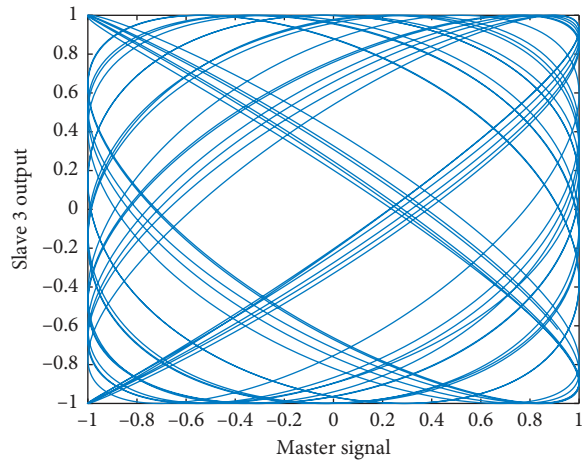


Figure 11: Continued.



(c)

Figure 11: TWMS time basis perturbed by $\Omega = 1.0$ phase ramp; (a) Node 1, (b) Node 2, and (c) Node 3.

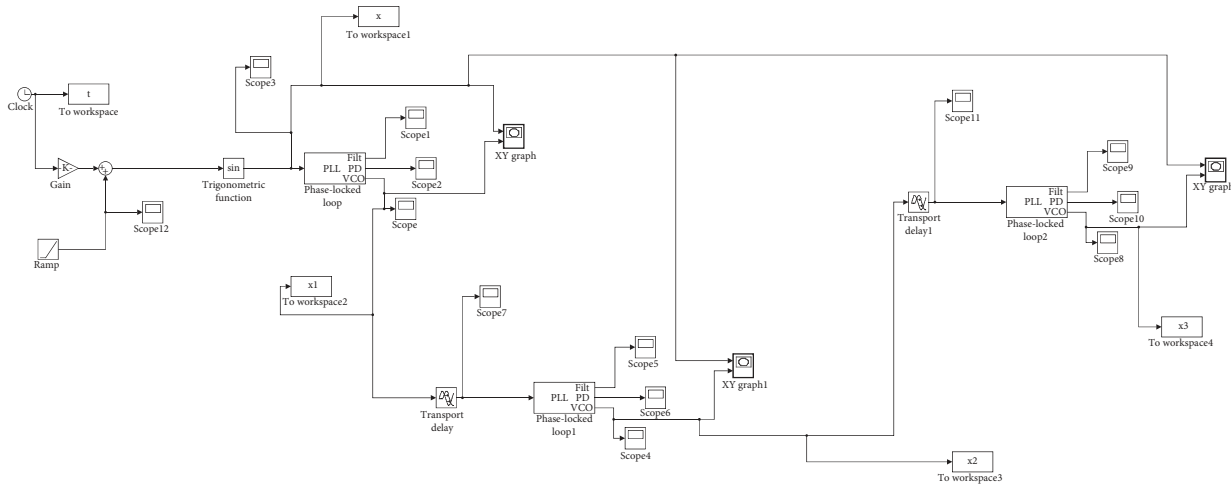


Figure 12: OWMS Simulink model.

5. Conclusions

Considering the problem of the recovering phase and frequency to provide clock signals in networks, isolated phase-locked loops provide good performance when excited by the stable periodic signal, as is widely known [3, 4, 6, 12, 19, 23], even perturbed by step perturbations. For ramp perturbations, inclinations shorter than the whole loop gain are tracked in frequency, with a constant phase error [4, 6, 19].

These simulation results are compatible with the recent development [27] about PLL analysis and can be used as rules of thumb to the time distribution systems design.

When OWMS PLL networks are built, even in non-perturbed situations, the number of nodes is limited by the acquisition time [19, 26]. Besides, if the master suffers high-step perturbations, bad transitory performance spoils the clock recovery performance. Ramp perturbations with inclinations shorter than the whole loop gain are tracked in frequency, with a constant phase error. If accuracy and short time tracking are necessary, the whole loop gain must be much larger than the ramp inclination [8, 21].

TWMS PLL networks are supposed to improve the precision of the clock distribution process. However, considering stable master clocks and deterministic perturbations, their performance is always worse than OWMS architectures.

Appendix

Figure 12 presents the Simulink diagram used to simulate the OWMS network, composed of a master node generating a periodical signal that can be locally perturbed. This signal is propagated through the three slave nodes where the synchronization process is measured considering the PD input and VCO output of each node.

Figure 13 presents the Simulink diagram used to simulate the TWMS network, composed of a master node generating a periodical signal that can be locally perturbed.

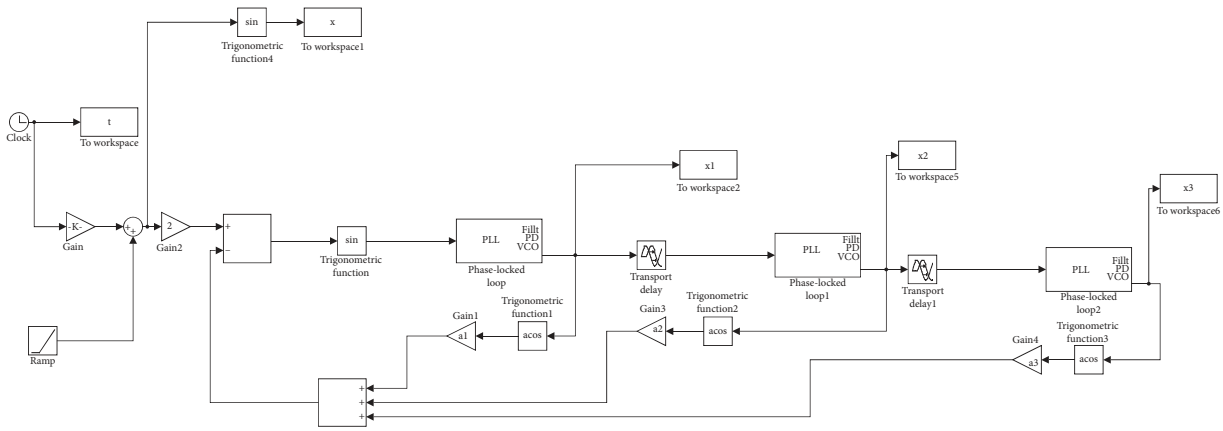


Figure 13: TWMS Simulink model.

Besides, the signal sent from the master to the first slave node has the phase adjusted by a linear combination of the phases of the slave nodes.

This signal is propagated through the three slave nodes where the synchronization process is measured considering the PD input and VCO output of each node.

Data Availability

All the data are described in the manuscript and can be obtained from the Internet by following the links cited at relevant places as references.

Conflicts of Interest

The author declares that there are no conflicts of interest regarding the publication of this article.

Acknowledgments

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