MATCHING PROPERTIES OF DEEP SUB-MICRON MOS TRANSISTORS

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MATCHING PROPERTIES OF DEEP SUB-MICRON MOS TRANSISTORS

by

Jeroen A. Croon

IMEC, Leuven, Belgium

Willy Sansen

Katholieke Universiteit Leuven,
Leuven, Belgium

and

Herman E. Maes

IMEC and Katholieke Universiteit Leuven,
Leuven, Belgium

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Preface

This book examines the matching properties of deep sub-micron MOS transistors. Microscopic fluctuations cause stochastic parameter fluctuations that affect the accuracy of the MOSFET. For analog circuits this determines the trade-off between speed, power, accuracy and yield. Furthermore, due to the down-scaling of device dimensions, transistor mismatch has an increasing impact on digital circuits. Good insight in the magnitude of the fluctuations and their physical origins is therefore required.
This work studies the matching properties of MOSFETs at several levels of abstraction. Firstly, a simple and physics-based model is presented that accurately describes the mismatch in de drain current for the full bias range above the threshold voltage. This facilitates accurate circuit design for deep sub-micron technologies. Secondly, the most commonly used methods to extract the matching properties of a technology are bench-marked with respect to model accuracy, measurement accuracy and speed, and physical contents of the parameters. This creates insight in which method to use in which situation and in how to treat data presented in literature. As third topic the physical origins of microscopic fluctuations and how they affect MOSFET operation are investigated. This leads to a refinement of the generally applied $\sigma_{\Delta P} \propto 1/\sqrt{area}$ law in both weak and strong inversion. In addition, the analysis of simple transistor models highlights the physical mechanisms that dominate the fluctuations in the drain current and transconductance. The fourth topic considers the impact of process parameters on the matching properties. In accordance with literature, it is found that the granular structure of the poly-silicon gate material can play an important role. Furthermore, it is identified that the gate does not act as an ideal mask for the halo implantation, which worsens the matching properties of a technology. Also, scaling issues are briefly addressed. Finally, the impact of gate

line-edge roughness is investigated, which is considered to be one of the roadblocks to the further down-scaling of the MOS transistor. The impact of line-edge roughness on parameter fluctuations, off-state current and yield has been modeled. The effect has also been experimentally studied by intentionally increasing the roughness and by studying transistors with sinusoidally shaped gate edges. A prediction is made about the technology node at which line-edge roughness will become an issue. Summarizing, regarding the matching properties of deep sub-micron MOS transistors, this book tries to present insight in the modeling aspects, characterization aspects, the physical origins, and technological aspects, while also extensively treating one of the main future issues. This work could therefore be useful for device physicists, characterization engineers, technology designers, circuit designers, or anybody else interested in the stochastic properties of the MOSFET.

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I'd also like to thank all my (former) colleagues in IMEC for making it such an inspiring environment to have worked in.

I'd finally like to acknowledge my family and friends for their contributions to life after working hours.

Jeroen Croon
November 2004

Chapter 1

INTRODUCTION

No two transistors are the same. When closely examined, differences can be observed at several levels, that, in one way or the other, are related to distance. For instance, when two 'identical' circuits are not fabricated in the same facility, they are produced by different people using different machines. This results in slightly nonidentical circuits and different circuit yields for the two different plants. In order to minimize differences, strategies like the 'copy EXACTLY! technology transfer method' of INTEL can be employed [1]. However, even within one production facility, differences between 'identical' circuits are observed. Different lots are not always processed using the same machines, while a machine itself shows a slight drift in time, which causes differences between wafers. On a single wafer, differences between dies are observed, which are called inter-die variations. These could for example be due to the fact that during processing the temperature is slightly different at the edge of a wafer than at its center.
The above effects are summarized in figure 1.1. The variation between circuits increases as their distance at process time increases. At the bottom of the upturned pyramid the intra-die fluctuations are present. Intra-die fluctuations are the differences between supposedly identical structures within one die. These differences can have a systematic nature when they are caused by asymmetries in layout. For instance, it was shown in [2] that the proximity of metal wiring lines can affect transistor operation. This e.g. reduces the mirror factor of a current mirror when one of the two transistors is more closely located to the metal line, which needs to be taken into account when the circuit is designed.
Besides systematic mismatch, also a stochastic component is present

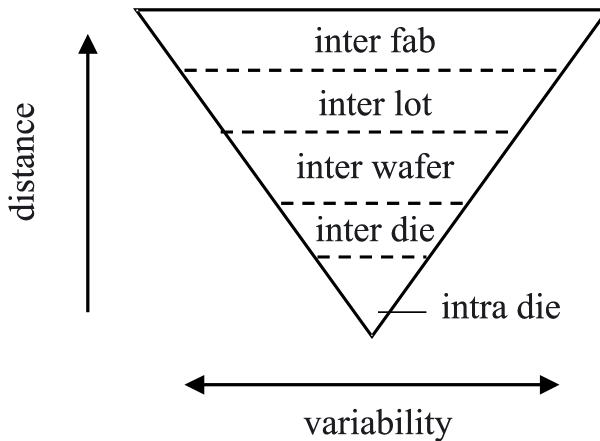

Figure 1.1. Variability at several levels

that is caused by the fact that at the microscopic level[1] transistors are not the same. One of the most well known examples of stochastic fluctuations in MOSFETs is the random nature of the amount of dopant atoms and their positions [3]. Stochastic fluctuations are independent of the distance between the devices under study, and by this they determine the maximal obtainable accuracy within a certain technology. In this work, we study the stochastic fluctuations of the MOSFET, which is the most important component of modern-day integrated circuits.

1.1 Matching analysis

The overall variability of a component is the sum of the variabilities at all levels. When studying the stochastic component, we want to filter out all other possible causes of variation. This is achieved by matching analysis, which characterizes the difference between two devices. Consider figure 1.2, which shows two types of variation: 1) Microscopic fluctuations typically have a length scale that is shorter than the device dimensions, and can be considered as spatial noise. 2) The other types of variations have length scales that are longer. Now look at the differences between the three devices that are depicted in figure 1.2. The difference between the first and third device is for the largest part due to a disturbance close to device 3, of which the impact lessens as distance increases. In other words, because the surroundings of device 1 and device 3 are nonidentical, their behavior is also nonidentical. This is often caused by

[1]Or at the nanoscale level for modern-day devices.

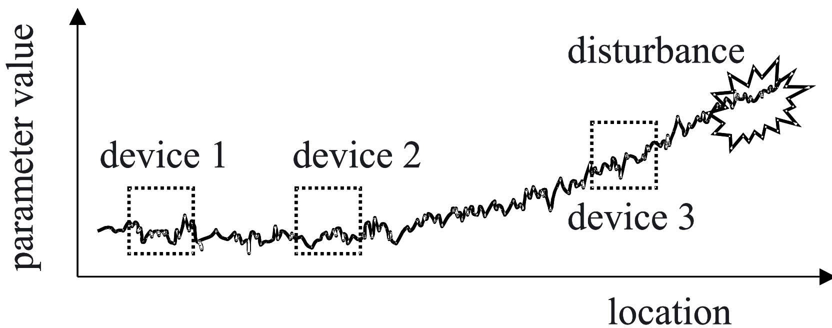

Figure 1.2. A certain device parameter as a function of the location on the chip. Devices are located at three positions.

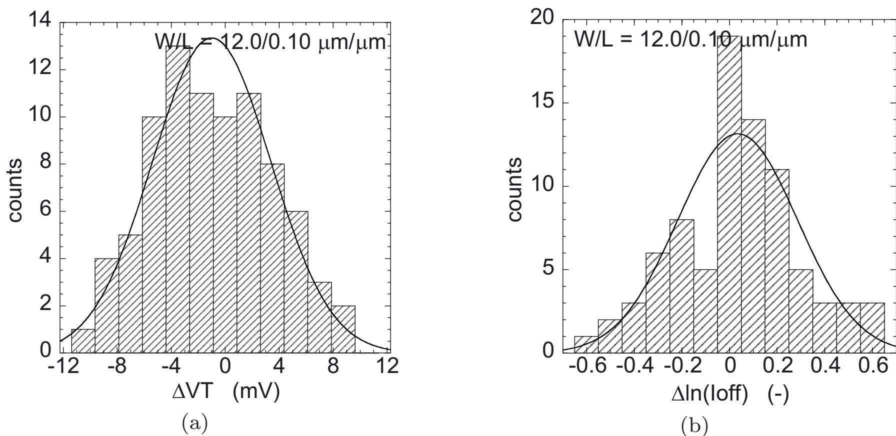

Figure 1.3. Distribution of the mismatch in the threshold voltage (a) and of the mismatch in the off-state current (b).

asymmetry in the layout, which means that the difference is systematic and the same for all processed chips. The difference between device 1 and 2 is only marginally affected by the disturbance close to device 3. Therefore, it is mainly caused by the stochastic variation. This means that the difference, or mismatch, between device 1 and device 2 is not the same as and uncorrelated to the difference observed on another chip. All this results in distributions for the mismatch as displayed in figure 1.3. Examples are shown for the mismatch in threshold voltage (ΔV_T) and the mismatch in the logarithm of the off-state current ($\Delta ln(I_{off})$). When a quantity is determined by a summation of numerous independent variables, its distribution tends to be normal, as is observed for

the mismatch in threshold voltage. The average value is determined by the systematic component of the mismatch (denoted by $\mu_{\Delta V_T}$ or $\overline{\Delta V_T}$), which is close to zero for a symmetric layout. The width of the distribution is caused by the stochastic component and it is represented by the standard deviation ($\sigma_{\Delta V_T}$) or by the variance, which is the square of the standard deviation.
Another distribution that will be encountered is the lognormal distribution, which arises when the exponent of a normally distributed parameter is taken. Lognormal distributions appear when numerous independent variables are multiplied. For the examples displayed in figure 1.3, it is observed that the mismatch in the off-state current can be approximated by such a distribution. In general, it will be found that the off-state current has a distribution in between normal and lognormal.
The difference between two devices is in most cases not represented by just one parameter. However, when more parameters are needed, these do not have to be independent from one another and correlations can exist. For instance, the off-state current is a function of the threshold voltage and a correlation between the fluctuation in these parameters can be expected.
Summarizing, when studying the matching performance of a technology, one examines the means of, standard deviations of, and correlations between the mismatch of relevant device parameters. The mismatch between two transistors increases when the distance between them is increased.

1.2 Importance for circuit design

In order to understand the impact of stochastic fluctuations, three circuit examples from literature are presented. These deal with the speed-accuracy-power trade-off in analog circuits, analog-to-digital converters, and with the SRAM circuit.
In [4] the impact of threshold-voltage mismatch on the speed-accuracy-power trade-off of analog CMOS circuits is investigated. The current mirror is examined as basic current-processing block. As basic voltage-processing block a one-transistor implementation of a voltage amplifier is taken. The size dependence of the mismatch is proportional to the inverse of the square-root of the area [5], i.e. $\sigma_{\Delta V_T} = A_{\Delta V_T}/\sqrt{area}$, where the proportionality constant $A_{\Delta V_T}$ characterizes the matching performance of a technology. Using this law, it is seen that the accuracy of a MOSFET can be increased by increasing its width or length. However, an increase in the width of a MOSFET results in a larger current and thus power dissipation. Increasing the length reduces the current, but it also reduces the speed. A similar reasoning can be applied for the

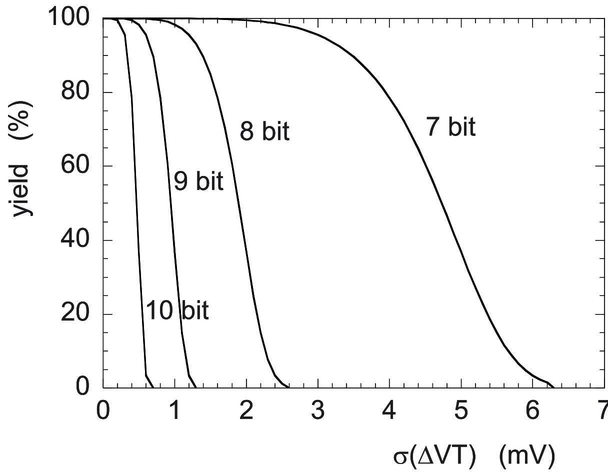

Figure 1.4. Yield of several analog-to-digital converters with different accuracies as a function of the standard deviation of the mismatch in threshold voltage. Results are taken from [6].

impact of noise. However, for the basic building blocks it is found that the impact of the matching performance of a technology on the speed-accuracy-power trade-off is one to two orders of magnitude larger than that of noise.

As second illustration, we take a look at the work presented in [6], in which the impact of stochastic variations on the yield of an analog-to-digital converter is investigated. The results of this work are copied into figure 1.4. It is indeed observed that a good matching performance is required to be able to make high accuracy analog-to-digital converters with acceptable yield.

As third example consider the SRAM circuit, which is embedded in many digital designs. Figure 1.5 shows a six transistor implementation of an SRAM cell and its transfer characteristic during read access. In [7, 8] the impact of stochastic variations in the threshold voltage on the SRAM is analyzed. This variation translates into a variation on the static noise margin (SNM), as defined in figure 1.5b. When the variation is too large, the SNM of some cells disappear, as is shown in figure 1.5 with the dashed line. In this case it is not possible to change the state of the cell and therefore it fails. It was found in [8] that in order to obtain a 90 % yield on a 1 Mbit SRAM it is required that $A_{\Delta V_T} < 6$ mVμm for a 180 nm technology and $A_{\Delta V_T} < 2.5$ mVμm for a 100 nm technology. This last number is not easy to achieve and it explains the increasing interest in research regarding stochastic parameter fluctuations.

(a)

(b)

Figure 1.5. Schematic of an SRAM cell (a) and its transfer characteristic during read access (b). b) The full lines give the transfer characteristic in case of average transistor behavior. The dashed lines represent an extreme case, for which the static noise margin is reduced to zero due to the stochastic variation in the threshold voltage. The static noise margin (SNM) is equal to the length of the side of the minimum square in the 'eyes' of the transfer characteristic. These figures are based on [7].

Summarizing, it can be stated that stochastic fluctuations limit the maximal obtainable accuracy, speed, size, yield and/or minimal obtainable power dissipation in CMOS circuits.

1.3 State of the art

Looking at the references made throughout this book, it is observed that only about one third is from before 1998, which is when this work was started. This indicates the increasing interest in research regarding the matching properties of MOSFETs. Here a brief introduction is presented to the most significant papers in this field. More complete references to literature will be made at the relevant places in this book. Three kinds of topics are distinguished. The first investigates the physical origins of MOSFET mismatch, the second models the mismatch in the drain current in terms of the mismatch in other transistor parameters, and the third investigates technology related issues. Note that one publication can treat more than one of these topics.
One of the first investigated effects of microscopic fluctuations on MOSFET operation was published in 1973 by Van Overstraeten, Declerck and Broux [9]. It shows that these fluctuations need to be taken into account for accurate modeling of the weak inversion current. The first paper that examines the impact of microscopic fluctuations on the stochastic properties of macroscopic MOSFET behavior was published in 1975 by Keyes [3]. It examines the impact of the discrete character of doping on the fluctuations in the threshold voltage. This is thought to determine the

lower obtainable boundary of threshold voltage fluctuations and it is still one of the most studied effects. A popular analytical derivation based on a charge-sheet approach was presented in 1997 by Takeuchi [10] and in 1998 by Stolk [11]. The topic has also been extensively studied by device simulations (see for instance the papers of Asenov [12]). Experimental work regarding doping fluctuations was presented in the mid-nineties by Mizuno [13] and in 2000 by Tuinhout [14]. We note that, until now, calculations regarding the impact of doping fluctuations are only able to explain half of the experimentally observed fluctuations in the threshold voltage. This indicates the presence of other fluctuation mechanisms.
Another extensively studied field is how the mismatch in MOSFET parameters translates into a mismatch in the drain current. In general, this is achieved by first order sensitivity analysis on a relatively simple model for the drain current. In most cases mismatch in the threshold voltage and mismatch in the current factor are taken into account (see for example the work of Vittoz [15] (1985), Lakshmikumar [16] (1986), Pelgrom [5] (1989), Bastos [17] (1995) and Serrano-Gotarredona [18] (2000)). Drennan [19] (1999) follows a slightly different approach by starting from a more complex compact model and by assuming prior knowledge of width and length dependencies to estimate model parameters.
Maybe the most referred to paper in matching literature is the one written in 1989 by Pelgrom [5]. This work examines the width and length dependence of the standard deviation of the mismatch at the fundamental level. This standard deviation is found to be inversely proportional to the square root of the device area. This is one of the best known laws in the field of matching.
The impact of technology-related parameters is less well understood. However, some effects were studied, like for instance the influence of metal coverage [20] (1996) and the impact of the granular structure of the gate material [21] (1997) by Tuinhout. The impact of the vertical doping profile was studied by Takeuchi [10] (1997), while e.g. Difrenza looked at the impact of halos [22] (2000). In 2001 Stolk [8] briefly outlined the required steps to optimize a technology with respect to its matching performance. However, note that technologies keep changing and that this work can never be considered complete.
Summarizing, we conclude that research of the stochastic properties of technologies is gaining in interest. Knowledge has been built up regarding the impact of doping fluctuations on the threshold voltage and of how the mismatch in the drain current depends on transistor parameters. Technology-related issues have been investigated, but are not completely understood. Furthermore, with the down-scaling to deep submicron and

sub 100 nm gate lengths, new technological and physical issues arise. In general it can be stated that full quantitative understanding of the matching properties of MOSFETs is still missing.
Finally, references should be made to the Ph.D. theses of Bastos [23] (1998), Difrenza [24] (2002) and Tuinhout, that deal with the topic of matching. Bastos mainly concentrated on the description of the mismatch in the drain current and on the impact of mismatch on a digital-to-analog converter. Difrenza focussed on the physical modeling and also discussed the impact of the gate material and the halo implantation. Based on numerous practical examples, Tuinhout extensively studied the measurement of mismatch and layout issues.

1.4 Research objectives

The main goal of this work is to understand, model and characterize the matching properties of deep submicron MOSFETs. This is further specified as:

- Develop a physics-based model that accurately describes the mismatch in the drain current over as large a bias range as possible.
- Benchmark different methods for mismatch characterization.
- Understand and provide models for the physical causes of MOSFET mismatch.
- Investigate the impact of process steps and technological parameters on the matching performance of deep-submicron technologies.
- Investigate the impact of line-edge roughness as one of the future causes for stochastic parameter fluctuations.

These objectives encompass all three matching research topics defined in the previous subsection. The work presented in this book is done on 180 nm and 130 nm CMOS technologies developed in IMEC. Experimentally investigated gate lengths range down to sub 100 nm.

1.5 Outline of this book

This book consists of five technical chapters after which it is concluded and suggestions for future work are presented. The chapters are related to the above mentioned research objectives and are presented in the same order. This also approximates the chronological order in which the work took place. Exceptions are chapter 4, for which the work was done last, and chapter 5, which shows results that were obtained during the full duration of this work.

We started our work in 1998 in IMEC by trying to describe the mismatch in the drain current as a function of other model parameters (chapter 2). We reasoned that, by taking a physical model as base, this would automatically lead to physical insight in the matching properties of the MOSFET. This turned out to be only partly true. By the time the work for chapter 2 got finalized, Philips Research and IMEC had started working together. Comparison of our extraction methodology with the one of Philips uncovered large and unexpected differences. This resulted in a small collaboration between Philips Research (Eindhoven, the Netherland), Philips Semiconductors (Nijmegen, the Netherlands), ST Microelectronics (Crolles, France) and IMEC. The same material was measured at each of these locations and the most common extraction methods were bench-marked. The results of this work are presented in chapter 3. By now it became apparent that a deeper knowledge regarding the physical origins of MOSFET mismatch was required, and a lot of the ideas that ended up in chapter 4 were developed in this period. At the same time, in the lithography group of IMEC the question arose how to deal with line-edge roughness. Another small collaboration was started, and priority was given to this work. However, some of the ideas regarding the physical origins of mismatch could already be applied for the specific case of line-edge roughness. We have therefore chosen to present the work regarding line-edge roughness in chapter 6 at the end of this book as an illustration of the more general theories presented earlier. By now our ideas regarding the physical origins of MOSFET mismatch had received time to mature. They are presented in chapter 4. In order to understand technological issues, relevant process splits were analyzed during the full duration of this work. Also, a dedicated experiment was set up, which mainly focussed on the impact of the halo implantation. The results of this work are presented in chapter 5.
A more detailed overview of the contents of the chapters will now be given.

Chapter 2: Measurement and modeling of mismatch in the drain current. The main topic of this chapter is the modeling of the mismatch in the drain current as a function of mismatch in the threshold voltage and current factor. An accurate model is required in order to fully understand the impact of variability on the MOSFET and to evaluate the impact of mismatch on circuits. We distinguish ourself from other work by our modeling approach: The impact of the mismatch in threshold voltage and current factor are treated separately. Assumptions that are required to model the impact of mismatch in the current factor are not required to model the impact of mismatch in the threshold voltage. This approach results in a continuous model that is valid in moderate

and strong inversion.
Most of the theories presented in this book are compared to experimental data. Therefore, chapter 2 starts by describing our measurement setup, test structures and measurement approach.

Chapter 3: Parameter extraction. Numerous methods exist that extract the variation in the threshold voltage and current factor. Quite often publications do not mention which method is used, but we will show that significant differences can occur. The most commonly applied methods are bench-marked with respect to model accuracy, physical meaningfulness, and measurement accuracy and speed. The following methods are examined: the maximum slope method, the three points method, the four points method, applying a current criterion and current-mismatch fitting methods.

Chapter 4: Physical origins of MOSFET mismatch. This chapter looks at the origins of fluctuations at the microscopic level and at how they affect MOSFET behavior. In order to achieve this, it is necessary to delve deeper into MOSFET theory than before and, as an introduction to this chapter, the basic equations of MOSFET operation are derived. The chapter continues by again deriving these equations, but now in the presence of microscopic fluctuations. In agreement with other published work, we find that the $1/\sqrt{area}$ law does not hold in weak inversion. Furthermore, we find in this regime of operation that edge effects, like halos or shallow trench isolation, can cause serious increases in the mismatch for long and wide transistors, which are not observed in strong inversion. In parallel and in agreement with a recent publication [25] we also find a slight departure of the $1/\sqrt{area}$ law in strong inversion for high enough values of the drain bias. Short- and narrow-channel effects are described using theories published in literature.
The chapter ends by using the theory of MOSFET operation to calculate the impact of doping fluctuations in the channel region and gate, the impact of fluctuations in the oxide charge and the impact of fluctuations in surface roughness. As in literature, the charge sheet approach is followed. The calculations include quantum mechanical effects, gate depletion and fluctuations in the mobility. We predict that Coulomb scattering gives a significant contribution to stochastic parameter fluctuations. We combine all models and fit the total model to the experimentally obtained curve of the mismatch in the drain current as a function of the gate bias. The physical content of the model is tested by predicting the mismatch in the transconductance, the mismatch at different bulk bias conditions, and the correlation of the mismatches at several bias conditions.

Chapter 5: Technological aspects. In this chapter examples are presented that demonstrate how certain process parameters can affect the

matching properties of a technology. As in literature we find that the grain structure of the gate material can have a large impact. Furthermore, the impact of the halo implantation is examined. We find that halos can seriously degrade the matching performance of a technology when they are unintentionally implanted through the gate. Also in this chapter, the scaling behavior of the matching performance is addressed.

Chapter 6: Impact of line-edge roughness on parameter fluctuations, off-state current and yield. For near-future gate-lengths, line-edge roughness is expected to cause significant parameter fluctuations, increase the off-state current and decrease yield. Therefore, it has recently become a topic of interest. The chapter starts with the description of line-edge roughness itself. Based on this information, we calculate the impact of line-edge roughness. We test our models by intentionally increasing the roughness. We then use these models to predict the moment at which line-edge roughness will become an issue. These predictions are used to present guidelines for as well device engineering as gate-patterning process development.

This book ends in *chapter 7* with the major conclusions and suggestions for future work.