Materials integration of gallium arsenide and silicon by wafer bonding

P. Kopperschmidt,[a)] S. Senz, G. Kästner, D. Hesse, and U. M. Gösele
Max-Planck-Institute of Microstructure Physics, Weinberg 2, D-06120 Halle, Germany

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We present a technique for the fabrication of materials integration of (100) silicon and (100) gallium arsenide by direct wafer bonding. GaAs wafers 3 in. in diameter were hydrophobically bonded to commercially available 3 in. silicon-on-sapphire wafers at room temperature. After successive annealings in hydrogen and arsenic atmospheres at temperatures up to 850 °C the Si/GaAs interfacial energy was increased by the formation of strong covalent bonds. Due to the difference in the lattice constants of about 4.1%, extra Si lattice planes were observed at the interface. No threading dislocations were introduced into the GaAs. © *1998 American Institute of Physics.*
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The monolithic integration of GaAs optoelectronic devices into high-speed silicon integrated circuits requires the combination of high quality single crystalline GaAs layers with silicon substrates. In this way, in principle, a wide variety of GaAs-based devices could be manufactured on silicon substrates, including majority carrier devices, field effect transistors, heterojunction bipolar transistors, and light emitting diodes.[1] Usually, GaAs layers are fabricated by heteroepitaxial growth on Si substrates. To avoid interdiffusion and reaction problems during the deposition of GaAs on silicon a low temperature process like molecular beam epitaxy or metalorganic chemical vapor deposition has been implemented.[2,3] However, two major problems exist: the formation of antiphase boundaries due to the growth of a compound semiconductor with a ZnS structure on a diamond structure substrate, and the lattice mismatch of 4.1% between GaAs and Si.[4–7] The formation of antiphase domains in the GaAs epilayer can be suppressed by using a Si (001) substrate tilted a few degrees towards the [110] direction in combination with a two-step growth procedure.[8,9] However, dislocation densities in the order of 10^6 cm^{-2} are generally observed to thread from the GaAs surface to the GaAs/Si interface through the GaAs epilayer thus affecting its electronic and optical properties as well as the lifetime of the resulting GaAs based device.[10] In addition to these problems, the thermal expansion coefficient of GaAs being nearly twice that of Si, requires a low temperature heteroepitaxy process.

Using the technique of direct wafer bonding (DWB)[11–13] instead of classical methods of GaAs-on-Si heteroepitaxy, lattice mismatch can be ignored, and threading dislocations within the GaAs can be avoided. In DWB, two mirror polished, cleaned wafers are brought into contact and hold together by van der Waals forces or hydrogen-bridge bonds at room temperature. A thermal annealing step at several hundred °C increases the bonding energy by the formation of strong covalent bonds. Thus DWB is a versatile method to join different materials regardless of their crystallographic orientation, structure, or lattice mismatch. Si wafers of large diameter can be bonded easily to GaAs at room temperature.[14,15] In this case the interface contains a layer involving silicon and GaAs related oxides. In addition, due to the difference in the thermal expansion coefficients, a subsequent thermal annealing step leads to debonding and cracking by thermally induced mechanical stress.[16] The problem of thermal mismatch, however, can be solved by DWB of commercially available silicon-on-sapphire (SOS) wafers on GaAs wafers. In earlier experiments, hydrophobic DWB of 3 in. GaAs to 3 in. sapphire wafers was investigated.[17] The thermal expansion coefficients of GaAs and sapphire are quite similar, thus allowing annealing at high temperatures in order to sufficiently enhance the bonding energy for further device processing. This favorable condition is also valid for bonding of GaAs on SOS wafers, which consist of a thin silicon layer on sapphire, instead of bare sapphire, as will be shown below. Furthermore DWB of SOS wafers on GaAs yields large-area, defect-free GaAs epilayers on (100) silicon substrates and perfect heterojunctions, free from threading dislocations, which is favorable, for example, for high-speed optoelectronic devices.

Commercially available (100) silicon-on-$(1\bar{1}.2)$ sapphire wafers of 3 in. diameter were first investigated by x-ray diffraction (XRD) and atomic force microscopy (AFM). XRD revealed the azimuthal angle φ of the Si (220) reflection to coincide with the position of the (00.6) reflection of the sapphire substrate. The in-plane full width half maximum (FWHM) $\Delta\varphi$ of these Si and sapphire reflections were obtained as 0.53° and 0.27°, respectively. By AFM a surface mean roughness $R_a = 0.2$ nm of the Si epilayer and $R_a = 0.1$ nm of the GaAs wafer was determined. Occasionally triangular terraces of various height, bounded by [110], $[1\bar{1}0]$, and [100] edges, were found at the surface of the Si thin film. After 20 min polishing with colloidal SiO_2 and cleaning in H_2O, NH_4OH, and H_2O_2 at 80 °C these terraces vanished but the surface roughness was increased, slightly insignificant for the room temperature bonding procedure.

For direct bonding, the GaAs (as received) and SOS wafers were placed into a microcleanroom with their flat lining up. After a deionized water rinse for a few minutes, the wafers were dried by 3000 rpm spinning and then joined hydrophilically by contacting the wafers' surfaces, initiated by a tong in the middle of the wafer pairs. In Fig. 1 an infrared transmission picture of a 3 in. bonded SOS/GaAs wafer pair

[a)]Electronic mail: kopper@mpi-halle.mpg.de

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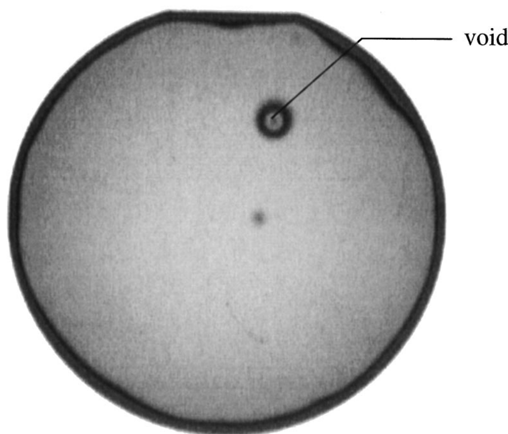

FIG. 1. Infrared transmission picture of a 3 in. SOS wafer directly bonded to 3 in. GaAs. Due to enclosed particles few voids were detected.

is shown. The bright contrast reveals the bonded area. Very few voids, resulting from enclosed particles, were detected. Hydrophobic bonding was realized by debonding the wafers at room temperature and heating them separately but in a narrow distance at 500 °C in 8 ℓ/min flowing hydrogen for a few hours. The converting of the hydrophilic wafers' surface chemistry into a hydrophobic one was proved by measuring the contact angle of a waterdroplet on the GaAs surface, which changed from 28° to 44°. After rebonding the wafers and cooling down to room temperature, the bonding energy or surface energy of the wafers, measured by introducing a blade into the interface, was determined by the well-known crack opening method as $50\ mJ/m^2$, too low for further processing. Pieces of $8\ mm \times 40\ mm$ in size of the wafer pairs were annealed in a second heating process at 850 °C for 20 h. To avoid the evaporation of arsenic vapor the pieces were enclosed in a quartz chamber and annealed in a 10^5 Pa arsenic atmosphere. During this annealing, the bonding energies increased up to energies comparable with the energy of covalent bonds in the GaAs bulk material. Attempts to open the GaAs/Si bonding interface lead to fracture of the GaAs. Due to the close match of the thermal expansion coefficients of GaAs and sapphire, the thermally induced mechanical stress is concentrated within the thin intermediate silicon layer. Thus sliding as well as cracking of the wafers during annealing can be avoided.

By cutting, grinding, and polishing, cross sections were prepared for electron microscope investigations of the SOS/GaAs interface. In Fig. 2 a scanning electron microscope (SEM) micrograph of the cross section is shown. The 480 nm thick Si epilayer was proven to be in direct contact with the GaAs wafer over a wide range. Along the interface, the Si/GaAs heterojunction seems to be homogeneous and uniform. Transmission electron microscope (TEM) [110] cross sections were also prepared. High resolution TEM micrographs were taken with a JEOL 4000EX electron microscope at 400 kV. Figure 3 shows a low magnification bright field image of the bonding interface. The silicon epilayer grown on the sapphire surface by standard heteroepitaxy shows many typical defects such as dislocations and twinned regions due to the large mismatch of the lattice constants of silicon and sapphire. At the sapphire/silicon interface, an intermediate layer of amorphous silicon oxide, about 5 nm thick, was observed in some regions. In contrast, no intermediate layer was found at the GaAs/Si interface as shown by high resolution TEM micrographs (Fig. 4). The latter also reveal steps at the interface with a height of up to nine lattice planes. Since the mean orientation of this interface is close to the crystallographic {001} planes of Si and GaAs, these steps cannot result from occasional miscut of these {001} surfaces. Instead, the steps seem to arise from a tendency to form facets of {111} orientation along the interface, probably for reasons of minimizing the surface energy. Small oxide precipitates occasionally occurred at the GaAs/Si interface, similar in appearance to those which had been found earlier

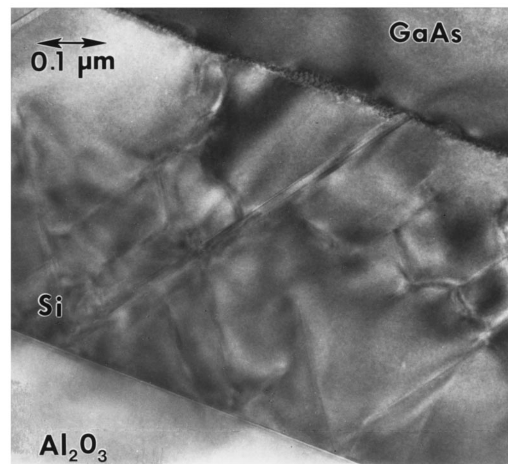

FIG. 3. TEM cross-sectional image of a bonded SOS/GaAs wafer pair. The Si epilayer reveals defects, in particular dislocations and twinned regions.

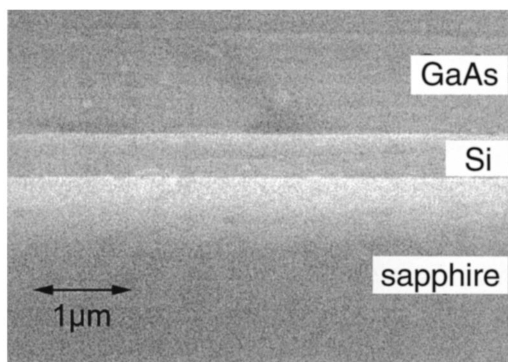

FIG. 2. Cross section of a bonded SOS/GaAs imaged by SEM. The 480 μm thick Si was found to be in direct material contact with GaAs over a wide range.

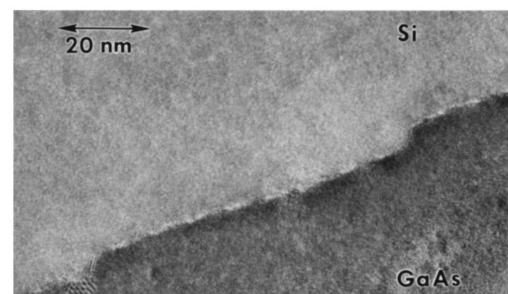

FIG. 4. High resolution TEM micrograph across the Si/GaAs interface. No intermediate layer was found between both lattices. Occasionally atomic steps were observed along the interface.

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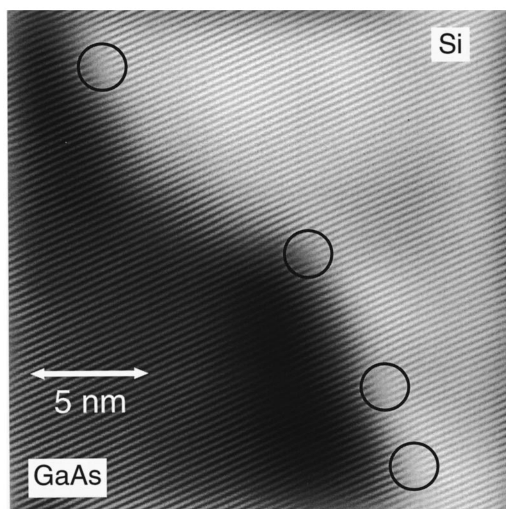

FIG. 5. TEM cross-sectional micrographs of the Si/GaAs interface including a step. Fourier filtered images reveal extra (110) Si lattice planes according to the lattice mismatch between Si and GaAs.

at GaAs/GaAs and GaAs/sapphire interfaces.[17] The GaAs was found to be in direct contact with the Si without an intermediate layer. Fourier filtered images around an atomic step in the [001] direction pointed out several extra Si lattice planes at the interface (marked rings) with a mean distance of 25 planes (Fig. 5). This indicates a mismatch of 4% in close agreement with the theoretical one. A similar mismatch of 3.6% is calculated from Fig. 4 if the periodic contrast features visible along the Si/GaAs interface are taken to result from interface dislocations having a Burgers vector edge component of $a/2$ and a mean distance of 1 nm in this micrograph. In contrast to the heteroepitaxial growth of GaAs on silicon and as expected from the fabrication procedure, no threading dislocations have been found in the GaAs lattice.

In conclusion, direct wafer bonding of commercially available SOS to (100) gallium arsenide was performed in a microcleanroom setup. A subsequent two-step annealing procedure in hydrogen and arsenic atmospheres at 500 and 850 °C allows a GaAs/Si materials integration accociated with bonding energies comparable to the intrinsic energy of the atomic bonds in GaAs bulk material. TEM investigations reveal an intimate lattice contact at the GaAs/Si interface. No threading dislocations were found in the GaAs. Extra Si lattice planes were observed at the interface due to the GaAs/Si lattice misfit of 4.1%.

By using SOS wafers with a Si epilayer of even higher quality, Si/GaAs heterojunctions over areas more than 3 in. in diameter should be possible with strong bonding, intimate contact, and free of threading dislocations in the GaAs. For practical applications, the GaAs wafer would have to be thinned down to a thickness range of about 1 μm or below. Thinning may be accomplished by the use of an epitaxial AlAs etch-stop layer or, alternatively, by a hydrogen implantation-induced ''smart cut'' procedure,[18] which has been demonstrated for Si, Ge, SiC, and diamond.[19] The wafer bonding of SOS to GaAs has the basic advantage of low thermal strains because the thermal expansion coefficients of sapphire and GaAs match closely. The procedure described may open new design possibilities for the integration of silicon and GaAs.

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