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Maximum current in nitride-based heterostructure field-effect transistors

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We present experimental and modeling results on the gate-length dependence of the maximum current that can be achieved in GaN-based heterostructure field-effect transistors (HFETs) and metal–oxide–semiconductor HFETs (MOSHFETs). Our results show that the factor limiting the maximum current in the HFETs is the forward gate leakage current. In the MOSHFETs, the gate leakage current is suppressed and the overflow of the two dimensional electron gas into the AlGaN barrier region becomes the most important factor limiting the maximum current. Therefore, the maximum current is substantially higher in MOSHFETs than in HFETs. The measured maximum current increases with a decrease in the gate length, in qualitative agreement with the model that accounts for the velocity saturation in the channel and for the effect of the source series resistance. The maximum current as high as 2.6 A/mm can be achieved in MOSHFETs with a submicron gate. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1476054]

Recently several groups, including ours, have reported on high-power microwave AlGaN/GaN based heterojunction field-effect transistors (HFETs). The dc saturation drain current I_{DS} is a key parameter controlling the maximum output rf power. This current I_{DS} increases with positive gate voltages until it reaches its maximum value, I_{DSM}. However, for conventional AlGaN/GaN GaN HFETs, gate voltages in excess of $+1.2$ V result in excessive leakage current, which limits I_{DSM}, decreases the transconductance, and increases the noise. To avoid this, we proposed and demonstrated AlGaN/GaN metal–oxide (MOSHFET)[1] and metal–insulator heterojunction field effect transistors (MISHFET).[2] In a MOSHFET or MISHFET, gate voltages as high as $+10$ V could be applied. This resulted in about 100% increase in the I_{DS} value with respect to the zero gate bias value. The gate leakage, however, remained well below 1 nA/mm.[2,3] We have also reported on the fabrication of a power switch using the AlGaN/GaN MOSHFET.[3] A switching power density as high as 7.5 kW/mm^2 was reported. This maximum power density of such a switch is also proportional to I_{DSM}. We now present a study to determine the mechanisms that limit the maximum achievable value of I_{DSM} for AlGaN/GaN HFETs and MOSHFETs.

There are several factors affecting the magnitude of I_{DSM} in HFETs and MOSHFETs. While in the devices with a long gate the drain saturation current depends on the electron mobility, in short gate devices, the electron velocity under the gate saturates, which limits the maximum current. The forward gate current, which increases exponentially as a function of gate bias, becomes a significant factor limiting the channel control at high positive gate biases in HFETs. In order to limit the gate leakage current, in many practical cases the HFET devices operate at the gate voltages ranging between the threshold and value slightly above zero. Also, at high sheet densities, electrons spill over from the two-dimensional (2D) channel into the barrier layer where the electron mobility is very low. This electron spillover limits the maximum sheet carrier density in the channel and, as a consequence, the maximum current. The model describing this mechanism of current saturation was developed in Ref. 4. Another limiting factor might be the current saturation in the ungated regions between the ohmic contacts and the gate. As mentioned above, the MOSHFETs and MISHFETs do not have the gate current limitation, and, therefore, as shown in this letter, have a substantially larger value of I_{DSM}.

The epilayers for the HFETs and MOSHFETs of this study were fabricated over SiC substrates using low-pressure metal organic chemical vapor deposition at 76 Torr. Our growth process involves using trace amounts of In in all the layers, which substantially improve materials quality. The room temperature Hall mobility and sheet carrier density were 1000 cm^2/V s and 6×10^{12} cm^{-2}. Both device types were fabricated on adjacent areas of the same wafer. HFET and MOSHFET devices were fabricated using Ti(200 Å)/Al(500 Å)/Ti(200 Å)/Au(1500 Å) for source and drain contacts, which were annealed at 850 °C for 1 min in nitrogen ambient. Pt/Au Schottky gates ranged in the lengths from 1 to 80 μm. A reactive ion etched mesa was used for the device isolation. For MOSHFET devices, a thin 7-nm-thick layer of SiO$_2$ was deposited on a part of the wafer prior to the gate metallization. A more detailed description of this fabrication procedure can be found in Ref. 5. In order to reduce self-heating effects, the devices with relatively low sheet carrier density (and the peak saturation currents below 1 A/mm) were selected for these comparative studies. For the same reason, the measurements of maximum saturation currents were done using 1 μsec pulsed bias.

In order to establish the effect of the gate length L_G on I_{DSM} the L_G value in the devices studied varied from 1 to 80 μm. Figure 1(a) shows the transfer characteristics for different gate length HFETs measured at the drain voltage sufficient to shift the operating point into saturation regime. Fig-

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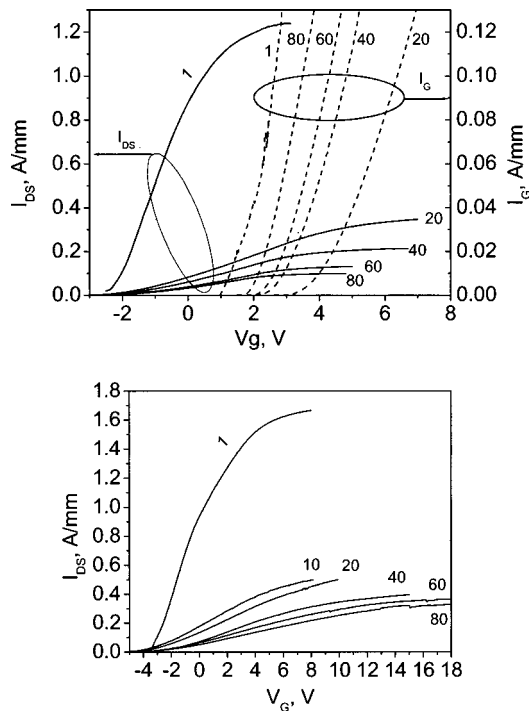[a]Electronic mail: simin@engr.sc.edu

FIG. 1. Gate bias dependencies of the drain saturation current and gate leakage current for HFET (a) and MOSHFET (b) devices. For MOSHFETs gate leakage current is negligibly small and is not shown. Drain bias corresponds to the saturation region of the device I–V characteristics.
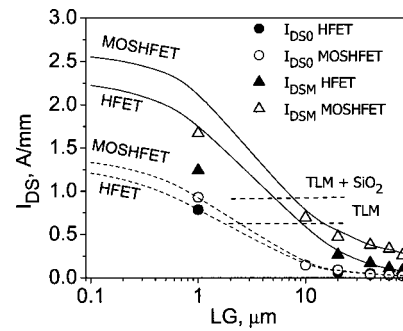

FIG. 2. Gate length dependencies of the maximum saturation current for HFETs and MOSHFETs. Symbols represent the experimental data; dashed and solid curves were plotted after Eqs. (2) and (3), respectively. Dashed lines marked TLM show the saturation currents for ungated structures with and without SiO_2 layers on the surface.

ure 1(a) also shows the gate bias dependence of the gate current in the saturation regime.

As seen, the I_{DSM} values increase with a decrease of L_G. For all gate lengths, the gate voltage corresponding to the maximum of I_{DS} in the HFETs also corresponds to the sharp increase of the gate leakage current. This indicates that the mechanism responsible for the I_{DS} saturation at high gate bias is the gate leakage current. This explains why the measured values of I_{DSM} for the HFETs at high gate bias are substantially smaller than those predicted by our model[4] as discussed later. We have calculated the internal values of the gate voltage corresponding to maximum current values I_{DSM} for different gate length HFETs using

$$V_{GM} = V_{GS} - I_{DSM} \times R_S, \qquad (1)$$

where V_{GS} is an external (measured) value of the saturation gate bias and R_S is the series resistance of the source-gate opening L_{GS}. The value of V_{MS} extracted this way from the characteristics of Fig. 1(a) was found to be $V_{GM} \approx 1.7$ V, nearly independent of L_G. This value is very close to that found from our 2D simulations as the value when a significant gate current starts to flow in the HFETs (these simulations were done using G-PISCES transistor simulator.[6])

In the MOSHFETs, in which the gate leakage is suppressed, the 2D electron spillover into the AlGaN barrier becomes a limiting mechanism. According to the model developed in Ref. 4, this electron spillover occurs at the source edge of the gate and at a certain value of the gate voltage V_{GM} that depends on the shape of 2D channel and Fermi level position. Due to this, the value of $V_{GM} \approx 5$ V extracted from the measurements for MOSHFETs differs significantly from that for HFETs. A larger gate-channel separation in MOSHFET also contributes to a higher value of V_{GM} for

MOSHFETs. The I–V characteristics for MOSHFET devices are shown in the Fig. 1(b). An important difference is that both the saturation gate voltage and the magnitude of saturation current for these devices are higher than those for HFETs. Gate leakage currents were negligibly small for MOSHFET devices (in low nanoampere range) and hence are not shown in Fig. 1(b).

In Fig. 2 we show the gate length dependence of the HFET and MOSHFET zero gate bias (I_{DS0}) and maximum (I_{DSM}) saturation currents from the experimental data of Figure 1 and from the analytical model proposed in Ref. 4:

$$I_{DSO} = \beta \cdot \frac{V_T^2}{1 + \beta \cdot R_s \cdot V_T + \sqrt{1 + 2\beta \cdot R_s \cdot V_T + \dfrac{V_T^2}{V_L^2}}} \qquad (2)$$

for the zero gate bias saturation current I_{DS0} and

$$I_{DSM} = \beta \cdot \frac{V_{GMT}^2}{1 + \sqrt{1 + V_{GMT}/V_L^2}} \qquad (3)$$

for the I_{DSM}. In these expressions, V_T is the threshold voltage ($V_T = -3$ V for HFETs and -5 V for MOSHFETs), $V_{GMT} = V_{GM} - V_T$, R_s is the source-gate series resistance, $\beta = C_i \mu / L_G$, $V_L = \nu_s L_G / \mu$, where C_i is the gate-channel capacitance per unit area, μ is the electron mobility in the channel, and ν_s is the electron saturation velocity. The values of series resistance R_s were extracted from the (TLM) measurements. The best fit for the saturation currents at zero gate bias, I_{DS0}, results in electron mobility in 2D channel $\mu \approx 1000$ cm^2/V s (quite close to the value of $\mu \approx 1000$ cm^2/V s from the Hall measurements) and electron saturation velocity $\nu_s = 1.3 \times 10^7$ cm/s. The same parameters along with experimentally found values of V_{GM} were used to fit the data for maximum currents I_{DSM} [Eq. (3)]. As seen, using these parameters the analytical expressions describe well the maximum saturation current in both HFETs and MOSHFETs with the gate length $L_G \geq 10$ μm. However, for short gate HFETs ($L_G = 1$ μm) Eq. (3) predicts much higher values of I_{DSM} than the experimental data. As mentioned above, we explain this difference by the effect of the forward gate current at high positive values of V_G. For MOSHFETs the results of Eq. (3) match better the experimental data for I_{DSM}, however, the theory still predicts higher values of

I_{DSM}. This we believe is due to the fact that Eq. (3) assumes uniform distribution of lateral electric field in the channel under the gate, which is not true. As seen from Fig. 2 MOSHFETs allow for significantly higher maximum saturation currents compared to the HFETs. Consequently, the maximum electron concentration achievable in the 2D channel of MOSHFETs is higher than that in HFETs and is only limited by the electron spillover. This means that still higher values of the maximum current can be achieved in the MOSHFETs by increasing the Al molar fraction (see, for example, Ref. 7). Such increase can be achieved by using quaternary wide band gap layers as suggested by our Strain Energy Band Engineering approach.[5]

In the limit of very short gate length the maximum current available from the transistor can be found from Eq. (3) at $L_G->0$

$$I_{DSM} = C_i \times (V_{GM} - V_T) \times v_s. \tag{4}$$

This equation results in the values of $I_{DSM} \approx 1.9$ A/mm for HFETs and $I_{DSM} \approx 2.6$ A/mm for the MOSHFETs used in our experiments. Since low current devices were deliberately used for these measurements, the MOSHFET maximum saturation currents can be substantially higher for the devices with a higher equilibrium sheet electron density.

The role of source-gate and gate-drain openings was studied using ungated transmission line model (TLM) patterns with the spacing between ohmic contacts from 2 to 20 μm. The measurements were done for AlGaN/GaN and SiO_2/AlGaN/GaN TLM structures that correspond to HFET and MOSHFET devices, respectively. The saturation current for these patterns is shown by dashed lines in Fig. 2. As expected, these currents are independent of the spacing, however, for the structure covered with the SiO_2 layer the value of saturation current is higher than that for uncovered TLM structure. This can be explained by a higher sheet density of 2D electrons in the channel covered with SiO_2. The most important observation is that the saturation currents from the TLM patterns were found to be lower than those of MOSHFET and HFET devices. This means that the source-gate and gate-drain openings in FET configurations are capable of sustaining higher current densities than the ungated 2D channel with just two ohmic contacts. One possible reason for that could be the additional strain in the AlGaN/GaN structure induced by positive gate voltage. As we proposed recently,[8] this strain should result in additional electron accumulation in the source-gate and gate-drain openings. More detailed study of this effect is ongoing.

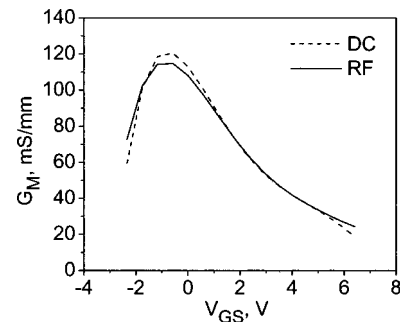To establish the effect of electron spillover into AlGaN barrier on the device rf behavior, we have extracted the val-

FIG. 3. Gate bias dependence of MOSHFET small-signal transconductance extracted from dc (dashed line) and 2 GHz rf (solid line) measurements.

ues of rf transconductance G_M for MOSHFETs at high gate bias from small-signal measurements in the frequency range 1–10 GHz. As shown in Fig. 3, these values of transconductance (at 2 GHz) coincide with those obtained from dc measurements, hence, no degradation of rf transconductance at high gate bias was observed. This can be understood by noting that electron spillover only limits the carrier concentration in the 2D channel, however the maximum current is still determined mainly by the electrons moving with the saturation velocity through the drain edge of the gate.

In conclusion, we have demonstrated that maximum achievable saturation current is substantially higher in MOSHFETs than in HFETs and increases with a decrease in the gate length. Maximum current above 2.6 A/mm can be obtained from the submicron gate MOSHFET devices, which makes them extremely attractive for high power applications.

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