Measurement Methodology for Accurate Modeling of SiC MOSFET Switching Behavior Over Wide Voltage and Current Ranges

Hiroyuki Sakairi, Tatsuya Yanagi, *Member, IEEE*, Hirotaka Otake, Naotaka Kuroda, Hiroaki Tanigawa, and Ken Nakahara, *Member, IEEE*

(Highlighted Paper)

***Abstract*—This paper presents two novel measurement methods to characterize silicon carbide (SiC) MOSFET devices. The resulting data are utilized to significantly improve the extraction of a custom device model that can now accurately reproduce device switching behavior. First, we consider the $I_{\rm d}$–$V_{\rm ds}$ output characteristics of power devices such as SiC transistors. These are typically measured using traditional curve tracers, but the characterization of the high-voltage and high-current (HVHC) region is very challenging because of device power compliance and self-heating. In this paper, we introduce a measurement technique that overcomes self-heating and derives the HVHC region from switching waveforms. The switching transient characteristics of devices are used to determine drain current $(I_{\rm d})$ as a function of drain–source voltage $(V_{\rm ds})$ in the HVHC range. Second, we consider another challenging characterization area: measurement of nonlinear capacitances when device is turned on. These capacitance characteristics of on-state devices are important for correcting disagreements between simulations and measurements in turn-off switching transient waveforms and cannot be measured using a conventional capacitance-voltage meter. We introduce S-parameter measurements as an effective method to obtain the capacitance characteristics of both off-state devices and on-state devices. These novel measurement techniques have been applied to the modeling of a SiC device. The extracted device model, a modified version of the popular Angelov—GaN high-electron-mobility transistor model, shows significant improvement in terms of the accuracy of switching waveforms of devices over a wide range of operating conditions.**

***Index Terms*—Circuit simulation, device modeling, double pulse tester, MOSFET, silicon carbide (SiC), S-parameter, switching behavior.**

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H. Sakairi, T. Yanagi, H. Otake, N. Kuroda, and K. Nakahara are with the Department of Research and Development, Rohm Co., Ltd., Kyoto 615-8585, Japan (e-mail: hiroyuki.sakairi@dsn.rohm.co.jp; tatsuya.yanagi@dsn.rohm.co.jp; hirotaka.otake@dsn.rohm.co.jp; naotaka.kuroda@dsn.rohm.co.jp; ken.nakahara@dsn.rohm.co.jp).

H. Tanigawa is with the EEsof EDA, Keysight Technologies Japan G.K., Tokyo 192-8550, Japan (e-mail: hiroaki_tanigawa@keysight.com).

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I. Introduction

WIDE-BAND-GAP semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) are promising candidate materials for power devices because they show excellent performance in low on-resistance, high-frequency, and high-speed switching, as well as in operation at high temperatures beyond the operating range of Si devices [1], [2]. Especially, the high-frequency and high-speed operation capability of SiC and GaN devices expands the possibility of miniaturizing power electronics systems [3]. However, these high-speed operations increase the time derivatives of voltage $(\mathrm{d}v/\mathrm{d}t)$ and current $(\mathrm{d}i/\mathrm{d}t)$ and deteriorate the conducted and/or radiated emissions [4]. This makes it difficult to ensure electromagnetic compatibility (EMC). Experimental approaches for improving EMC require multiple rounds of testing, which inevitably delays product launch. Thus, the front-loading design should be established for achieving EMC by maximizing the features of power devices built using the new materials.

To this end, it is crucial to establish a simulation environment that accurately predicts the electromagnetic (EM) noise in the investigated systems. This means that the simulation has to reproduce the transient waveforms of power device switching as accurately as possible, because the switching process generates high-frequency electric signal components, which mainly generate EM noise. Accordingly, the quality of the switching device model used in the simulation significantly influences simulation quality.

The power device modeling methods previously reported, however, include insufficient experimental data on the range of drain current $(I_{\rm d})$ and drain–source voltage $(V_{\rm ds})$. Measured data of several tens of amperes for $I_{\rm d}$ and $\sim$20 V for $V_{\rm ds}$ are conventionally used for extracting the parameters of a device model. However, these values are far less than the $I_{\rm d}$ and the $V_{\rm ds,}$ values used commonly in the power applications in which SiC and GaN are expected to be applied [3], [5]. Consequently, it is necessary to measure the $I_{\rm d}$–$V_{\rm ds}$ characteristics in higher current and voltage regions than usual to develop high-quality power device simulation models.

Another problem is measuring the capacitance-voltage (*C*–*V*) characteristics of power devices. The commonly used

C–V meter is capable of measuring device capacitance in the off-state. However, the on-state *C–V* curve of a MOSFET heavily affects its switching transient behavior, especially in the turning-off transition, but this type of measurement has not yet been established.

The last issue we discuss here is determining how to include the parasitic impedance of a measurement system into switching simulation because the system itself has non-negligible effects on switching waveforms. One approach is to measure parasitic impedances, for which circuit simulation is performed [6]; another is to model the system by calculating the S-parameters [7], [8]. We do not choose the first option because it requires measurements, thus conflicting with the main research focus of front-loading design.

In this study, we propose experimental procedures for extracting an accurate device model. A commercially available SiC MOSFET is examined as the research object. The characterization process is as follows:

1) static $I_{\rm d}$–$V_{\rm ds}$ characteristics of the SiC device are obtained in a high-voltage and high-current (HVHC) range by performing switching measurements;
2) the *C–V* curves of the SiC device with a forward bias applied to its gate are acquired by S-parameter measurements; and
3) EM simulation is performed to determine the S-parameter describing the measurement system and the device package, and this result can be used directly in an S-parameter-based circuit simulation.

The above modeling procedure is applied to a modified version of the Angelov−GaN high-electron-mobility transistor (HEMT) model, which serves as an example of a state of the art model capable of incorporating key effects. However, the procedure can be applied to any compact model.

In each characterization step, a subset of related model parameters of the modified Angelov−GaN HEMT was extracted by comparing measured and simulated data. Finally, the measured and the simulated switching waveforms of gate–source voltage $(V_{\rm gs})$, $V_{\rm ds}$, and $I_{\rm d}$ were compared, and very good agreement was found over a wide operation range.

II. Selected Device and Model

The examined device was a SiC MOSFET (SCT2080KE made by ROHM Co., Ltd.; Rated voltage = 1200 V; Rated current = 40 A). The Angelov−GaN HEMT model was employed as the base model for the SiC MOSFET model used in this work [9]. Fig. 1 shows an equivalent circuit schematic of the device model used. The original Angelov−GaN HEMT topology was modified by adding a pn-diode model between the source and the drain. The current and charge model equations were modified to better represent the *I–V* and the *C–V* characteristics of the SiC MOSFET. The modified parts of the equations are explained in this section.

A. Drain Current Equations

As shown in Fig. 7 in Chapter III, we found that the drain current of the SiC MOSFET at each $V_{\rm gs}$ was not saturated in the measured HVHC range (the so-called saturation region), and

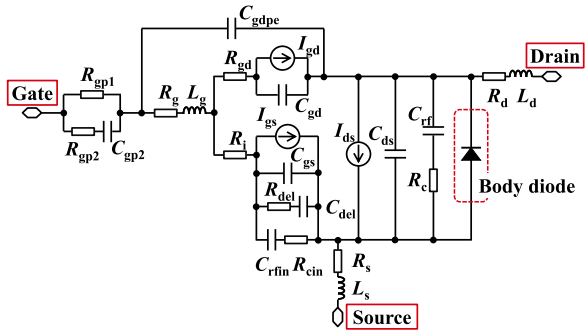

Fig. 1. Equivalent circuit of the original Angelov model that was adapted to add a pn-diode as the body diode of a SiC MOSFET.

the gradient of the drain current depended on $V_{\rm gs}$. Therefore, we added a gate bias-dependent term to the original Angelov−GaN HEMT model equation [9] to better represent the actual $I_{\rm d}$–$V_{\rm ds}$ characteristics of the SiC MOSFET in the HVHC range.

The drain current equations are given as follows:

$$I_{\rm ds} = 0.5 \times (I_{\rm dsp} - I_{\rm dsn}) \tag{1}$$

$$I_{\rm dsp} = A \times g_1(V_{\rm gs}) \times (1 + f_1(V_{\rm gs},\ V_{\rm ds})) \times (1 + g_3(V_{\rm gs}) \times f_2(V_{\rm gs}, V_{\rm ds}) + B \times g_4(V_{\rm ds})) \tag{2}$$

$$I_{\rm dsn} = A \times g_1(V_{\rm gd}) \times (1 + f_1(V_{\rm gd},\ V_{\rm ds})) \times (1 + g_3(V_{\rm gd}) \times f_2(V_{\rm gd}, V_{\rm ds})) \tag{3}$$

$$g_1(V_i) = 1 + \tanh\left(0.5 \times \left(e^{g_2(V_i)} - e^{-g_2(V_i)}\right)\right) \tag{4}$$

$$g_2(V_i) = C_1 \times (V_i - f_3(V_{\rm dg}, V_{\rm ds}) + C_2 \times (V_i - f_3(V_{\rm dg}, V_{\rm ds}))^2 + C_3 \times (V_i - f_3(V_{\rm dg}, V_{\rm ds}))^3\Big) \tag{5}$$

$$g_3(V_i) = G_1 + G_2 \times g_1(V_i) \tag{6}$$

$$g_4(V_{\rm ds}) = e^{J \times (V_{\rm ds} - K)} \tag{7}$$

$$f_1(V_i,\ V_{\rm ds}) = \tanh((E + F \times g_1(V_i)) \times V_{\rm ds}) \tag{8}$$

$$f_2(V_i,\ V_{\rm ds}) = \tanh((H_1 \times \tanh(1 + H_2 \times V_i)) \times V_{\rm ds}) \tag{9}$$

$$f_3(V_{\rm dg}, V_{\rm ds}) = D - L + L \times \tanh(F \times V_{\rm ds}) - M \times (V_{\rm dg} - K)^2. \tag{10}$$

The term added for the current equation is (9). H_1 and H_2 are channel length modulation parameters, and they are used for fitting the SiC MOSFET model to measurements. H_2 is an added parameter for describing the dependence of output conductance on $V_{\rm gs}$ in the large $V_{\rm gs} \times V_{\rm ds}$ region. $A, B, C_1, C_2, C_3, D, E, F, G_1, G_2, H_1, H_2, J, K, L,$ and M are fitting parameters in the SiC MOSFET model, and V_i is $V_{\rm gs}$ or gate–drain voltage $(V_{\rm gd} = -V_{\rm dg})$.

B. Charge Equations

We modified the charge equations of the SiC MOSFET model. The parasitic capacitances of the SiC MOSFET were modeled using the following mathematical scheme.

First, the charge between the gate and the source Q_{gs} is expressed as follows:

$$Q_{gs} = (C_{gs0} + C_{gs1} \times f_{32}(V_{gs}, V_{ds})) + (C_{gs0} + (C_{gs1} \times f_{31}(V_{gs}, V_{ds}) + C_{gs2} \times f_{33}(V_{gs}, V_{ds})) \times f_{32}(V_{gs}, V_{ds})) \quad (11)$$

$$f_{3i}(V_{gs}, V_{ds}) = 1 + \tanh(L_i + N_i \times V_{gs} + P_i \times V_{ds}) \quad (i = 1 \sim 6) \quad (12)$$

C_{gs0} is a gate–source pinch-off capacitance, and C_{gs1} and C_{gs2} are gate–source capacitance parameters. $C_{gs0}, C_{gs1}, C_{gs2}, L_i, N_i, P_i$ are fitting parameters of the SiC MOSFET model. As for Q_{gs}, capacitances with two types of dependence on the gate–source voltage can be expressed by using f_{31} to express a positive bias dependence on the gate–source voltage and f_{33} to express a negative bias dependence.

Second, the charge between the gate and the drain Q_{gd} is expressed as follows:

When V_{ds} is greater than $-F_{cp}$

$$Q_{gd} = C_{gd1} + g_5(V_{ds}) \times f_{34}(V_{gs}, V_{ds}) + C_{gd2} \times g_5(V_{ds}) \times f_{35}(V_{gs}, V_{ds}) + C_{gd3} + C_{gd4} \times f_{36}(V_{gs}, V_{ds}) \quad (13)$$

$$g_5(V_{ds}) = C_{gd0} \times \left(1 + \frac{V_{ds}}{V_j}\right)^{-Mm}. \quad (14)$$

When V_{ds} is smaller than $-F_{cp}$

$$Q_{gd} = C_{gd1} + g_6(V_{ds}) \times f_{34}(V_{gs}, V_{ds}) + C_{gd2} \times g_6(V_{ds}) \times f_{35}(V_{gs}, V_{ds}) + C_{gd3} + C_{gd4} \times f_{36}(V_{gs}, V_{ds}) \quad (15)$$

$$g_6(V_{ds}) = \frac{C_{gd0}}{(1 - F_c)^{Mm}} \times \left(1 + \left(\frac{Mm}{V_j(1 - F_c)}\right) \times (-V_{ds} - F_c \times V_j)\right). \quad (16)$$

Here F_{cp} is defined as follows:

$$F_{cp} = F_c \times V_j \quad (17)$$

where F_c is a forward bias junction parameter of C_{gd}, and V_j is the junction potential of C_{gd0}.

Where C_{gd1} is a gate–drain pinch-off capacitance, C_{gd0} is a gate–drain capacitance parameter, Mm is a grading coefficient for C_{gd0}, and C_{gd2} is a gate–drain capacitance parameter. $C_{dg0}, C_{dg1}, C_{dg2}, C_{dg3}, C_{dg4}, V_j, Mm$, and F_c are fitting parameters of the SiC MOSFET model. Q_{gd} consists of two numerical expressions with junction capacitance, which results in more accurate drain voltage dependence. The f_{36} function provides a good fit of the simulation data to the experimental data in the low drain voltage region.

C. Body-Diode Model

The SiC MOSFET has a body diode in its device structure, which is not considered in the original Angelov−GaN HEMT model because GaN HEMTs have dissimilar structures. Therefore, we adapted this model to create the SiC device model by adding a pn-diode model between its drain and source electrode to reproduce the C_{ds}–V_{ds} capacitance characteristics, as shown in Fig. 1. In this work, the *I–V* characteristics of the body diode were not used in the inductive load switching circuit that we used for model validation because the high-side device in the switching circuit is a Schottky barrier diode and the low-side device does not use the reverse current characteristics. Therefore, we fitted the reverse *I–V* characteristics of the SiC MOSFET very roughly. More accurate modeling of the reverse I_d–V_{ds} characteristics could be a topic for a future investigation.

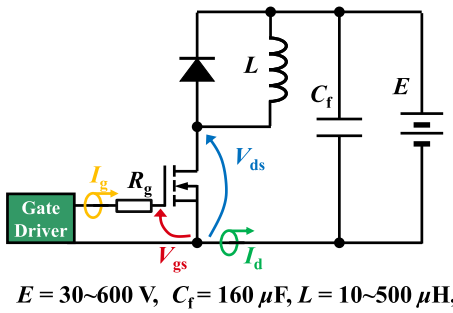

Fig. 2. Schematic diagram of clamped inductive load circuit used to acquire switching behavior of SiC MOSFET. The direction of the arrows shows the high-side of the voltage and the positive direction of the flowing current.

The most important part in this study was establishing a measurement procedure to obtain accurate experimental data, so that the model can predict device behavior in a circuit. The details of the developed measuring techniques are described in the following sections.

III. I_D–V_{DS} Characteristics Measurement

A. Principle of Measuring Static I_d–V_{ds} Characteristics Based on Switching Behavior

Previous static I_d–V_{ds} characteristic measurements, as described in the introduction, did not cover the voltage and current areas where SiC MOSFETs are expected to be applied. Self-heating of the device under test (DUT) cannot be avoided when using the conventional methodology. Therefore, we developed a new method to measure the I_d–V_{ds} characteristics by utilizing switching transient behavior measurements. A similar method has already been proposed elsewhere [9], but we improved it to acquire the I_d–V_{ds} characteristics over wider voltage and current regions than those in the reference. The main differences from the previous study [10] pertain to the method of measuring I_g and the gate plateau voltage used to derive V_{gs}.

A clamped inductive load switching circuit (see Fig. 2) allows us for the characterization of the switching transient waveforms of the SiC MOSFET. Three SiC Schottky barrier diodes (SCS240KE2 made by ROHM Co., Ltd.) were connected in parallel and used as the high-side device. E, C_f, L, and R_g denote a power source (600 V), film capacitor ($160\,\mu$F), load inductance ($500\,\mu$H), and gate resistance ($240\,\Omega$), respectively.

The switching data acquired with $I_d = 20$ A are plotted as a trajectory curve in the I_d–V_{ds} plane (pale orange line) in Fig. 3. This figure includes the red lines denoting the I_d–V_{ds} characteristics measured using a curve tracer (CT).

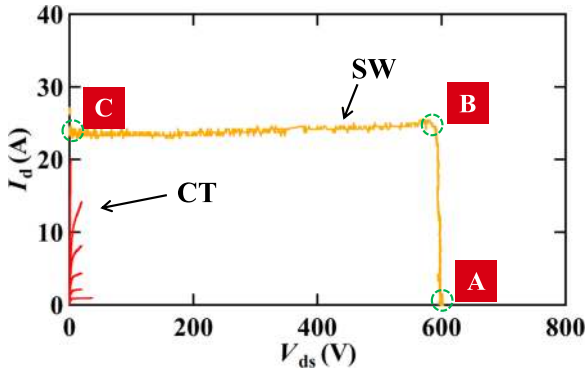

Fig. 3. I_d–V_{ds} plane including SW of SiC MOSFET (solid pale yellow line "SW"), and CT measurement results (red solid lines "CT"). A, B, and C denote the discriminative switching points detailed in the main text.

First, Fig. 3 shows that the CT data do not cover the actual operating area at all. The I_d–V_{ds} characteristics region delineated by the switching trajectory (SW) in this figure is the least data necessary to predict the switching behavior of this power device.

Second, the SW line indicates the method of measuring the I_d–V_{ds} characteristics in real operating ranges by obtaining switching measurements. When the DUT was switched on, the track shifted from A (off-state) through B to C (on-state). I_d cannot increase beyond the load current determined by the high-side closed loop composed of an inductor and diodes. Therefore, at this moment, the direction of the I_d–V_{ds} trajectory must be changed. Point B in Fig. 3 denotes the moment at which V_{gs} reaches the so-called gate plateau voltage (V_p). This means that point B in Fig. 3 identifies the I_d–V_{ds} characteristics specified by $V_{gs} = V_p$ in a high-V_{ds} region. Our measurement method, which allows us for the determination of I_d–V_{ds} over wider voltage and current regions without self-heating of the DUT, is based on this experimental observation, and details of the associated procedures are given in the following two sections.

Fig. 4 shows the switching waveforms of a SiC MOSFET in the turn-on transient, as measured using the circuit displayed in Fig. 2. The operating conditions are as follows: $E = 600\,\text{V}$, $R_g = 240\,\Omega$, and $L = 500\,\mu\text{H}$. The symbols A, B, and C in the figure denote the respective operation points, as in Fig. 3. The plateau region must be long to improve the accuracy of the transient response measurement. Thus, gate resistance was set to a large value of 240 Ω.

I_d remains zero from the beginning of switching to the operation point A, when the time zone V_{gs} does not exceed the threshold voltage (V_{th}) of the DUT. In the operating region from A to B, I_d increases while V_{ds} remains constant. When I_d reaches the load current, V_{ds} starts to decrease while I_d remains constant and V_{gs} is pinned to V_p [11], [12]. As explained above, this data point provides the static I_d–V_{ds} characteristics specified by point B. If this process is repeated with different E and I_d, the obtained dataset including V_{gs}, I_d, and V_{ds} allows us to determine the I_d–V_{ds} characteristics in the HVHC region.

In addition, device self-heating is negligible when using this method. The energy equivalent to the heat generated during one switching process is calculated to be 6.6 mJ when

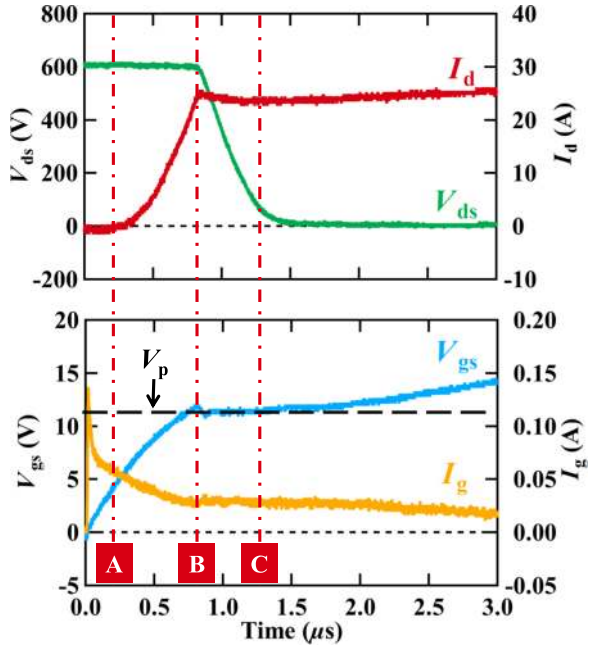

Fig. 4. Experimental switching waveforms of SiC MOSFET in inductive load switching using circuit shown in Fig. 2.

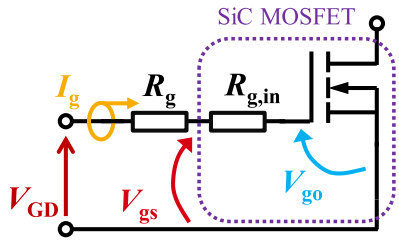

Fig. 5. Equivalent gate-driving circuit; $R_{g,in}$ denotes internal gate resistance of SiC MOSFET die, and V_{GD} is output voltage of gate driver.

$V_{ds} = 600\,\text{V}$ and $I_d = 20\,\text{A}$. By contrast, when using the conventional method, it can be as much as 1.2 J when the CT pulse width is 100 μs, which is the general setup for the CT measurements. This finding validates that our method is appropriate for obtaining the true static I_d–V_{ds} characteristics of a DUT at room temperature. Therefore, we used the switching behavior data to acquire the static I_d–V_{ds} characteristics over a wide I_d–V_{ds} range.

B. Adapting V_{gs} and RT Static I_d–V_{ds} Curves

We should note, however, that the V_{gs} measured using our method is not the same as that captured using the CT. The CT measures I_d at $I_g = 0\,\text{A}$, because the measurement is performed after adequate time elapses for V_{gs} to become constant. Thus, the conventionally measured V_{gs} is always equal to the voltage applied to the gate oxide layer of a MOSFET (V_{go}), which determines the I_d–V_{ds} curves. As shown in Fig. 4, however, I_g is not 0 A with this method, and $V_{go} \neq V_{gs}$. Accordingly, the V_{gs} measured by this method must be adapted to obtain the static I_d–V_{ds} curves.

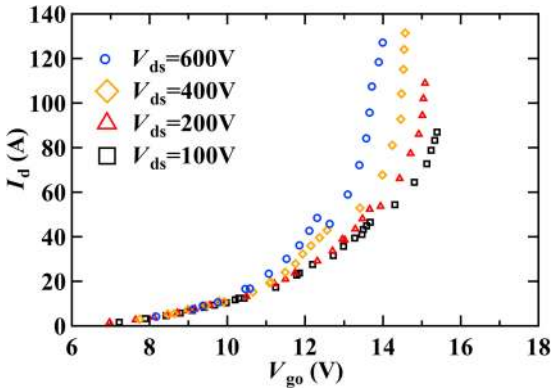

Fig. 6. RT I_d–V_{go} characteristics obtained by multitudinous switching measurements.

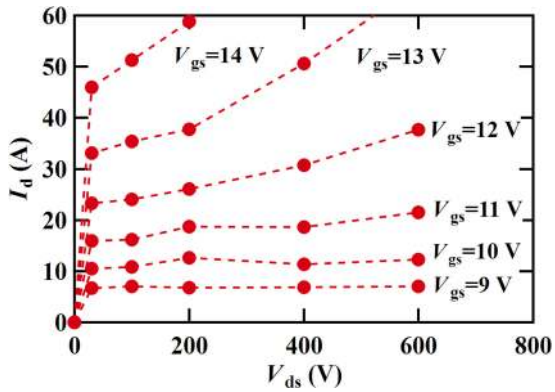

Fig. 7. I_d–V_{ds} characteristics acquired from switching waveform data in HVHC region.

The equivalent gate-driving circuit is shown in Fig. 5. As indicated in the figure, the output voltage of the gate driver (V_{GD}) decreases due to R_g and the internal gate resistance $(R_{g,in})$ when I_g flows in the manner shown in this figure. Thus, V_{gs} differs from V_{go}.

As described in detail in Section A, we collect I_d and V_{gs} at various E to acquire the I_d–V_{ds} characteristics, but it is very difficult to specify I_d, I_g, and V_{go} from the measured data due to non-negligible jitter (see Fig. 4). Thus, the mean value over the plateau region is used to obtain the I_d–V_{ds} characteristics.

The measured V_p and I_g data in the plateau region of a switching waveform are averaged ($V_{p,ave}$ and $I_{g,ave}$) to eliminate jitter in the data. This is validated by the facts that I_g is constant in the plateau region because I_g can be simply calculated by

$$I_g = \frac{V_{GD} - V_{gs}}{R_g} \tag{18}$$

and V_{GD} and R_g are constant with V_{gs} being fixed at V_p.

Accordingly, V_{go} is computed as

$$V_{go} = V_{p,ave} - R_{g,in} I_{g,ave}. \tag{19}$$

This V_{go} corresponds to the V_{gs} conventionally obtained by the CT.

Furthermore, we should consider that the SiC MOSFET has positive I_d–V_{ds} curves, even in the saturation region, owing to its short channel effect [11], [13]. Consequently, V_p depends on V_{ds} even at the same I_d; therefore, V_p must be measured under different V_{ds} and I_d. Accordingly, in this study, the switching characteristics are measured at $E = 30, 100, 200, 400$, and 600 V, and the equation (19) provides V_{go}, which is regarded as V_{gs} in the conventional context. The measured I_d values are plotted as a function of V_{go} at each V_{ds} $(= E)$, leading to the I_d–V_{go} characteristics. Fig. 6 shows the I_d–V_{go} characteristics at $V_{ds} = 100, 200, 400$, and 600 V, as examples.

In the switching measurements, V_{ds} and I_d can be specified intentionally, whereas V_{go} cannot be. The I_d and V_{ds} values at a specific V_{go}, however, are necessary to draw an I_d–V_{ds} curve, and, thus, a number of measured I_d–V_{go} curves are fitted by polynomial approximation by using the least squares method.

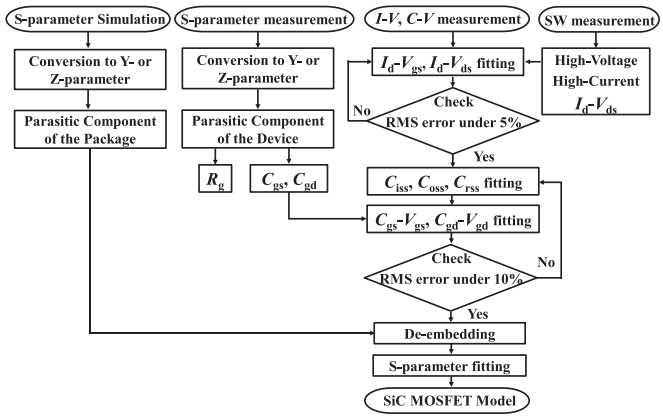

Fig. 8. Modeling flow chart for the parameter extraction.

The function used is a polynomial expression as follows:

$$y = \sum_{i=0}^{n} a_i X^i. \tag{20}$$

We chose a value of n between 3 and 6 to obtain the best fit. These fitted curves provide the dataset of I_d and V_{ds} at a specific V_{go}, and finally the static I_d–V_{gs} characteristics are shown in Fig. 7, wherein V_{gs} is used as V_{go} to place the curves in the conventional context. In this figure, the plotted points are the measured data.

C. Parameter Extraction Using I_d–V_{ds} Characteristics With HVHC Region Data

Using measured I_d–V_{ds} data from HVHC region, parameter extraction was performed with a commercially available parameter extraction tool (IC-CAP; Keysight Technologies, Inc.). IC-CAP includes the original and modified Angelov–GaN model. The measured *I–V* and *C–V* data were fed into IC-CAP, and the simulated data were fitted to the measured data for a parameter extraction. The fitting procedure was performed with the nonlinear least-squares-fit algorithm in IC-CAP until the root mean squared (RMS) error was less than 5% and 10% for the *I–V* and *C–V* curves, respectively. Fig. 8 presents a flow chart for the parameter extraction.

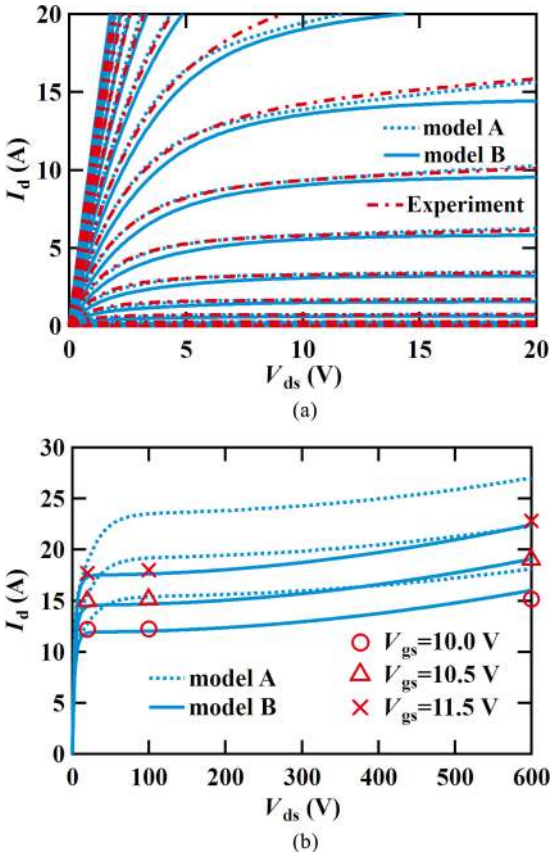

Fig. 9. (a) Fitted results of I_d–V_{ds} characteristics in the CT measurement region. (b) Fitted results of I_d–V_{ds} characteristics in the HVHC region. The red lines in (a) and the circles, triangles, and crosses in (b) are measured data. The blue dot and solid lines show the I_d–V_{ds} curves fitted by models A and B, respectively.

In the parameter extraction for *I–V* characteristics, first, the I_d–V_{ds} characteristics in the CT measurement region were roughly fitted. Second, the I_d–V_{ds} characteristics in the HVHC region were accurately fitted. Finally, the I_d–V_{ds} characteristics in the CT measurement region were fitted once again with increased accuracy; however, in this step, we considered only the accuracy of the linear region (R_{on}) of the I_d–V_{ds} curves.

The parameter extraction results are shown in Fig. 9. Fig. 9(a) and (b) shows the fitted results of I_d–V_{ds} characteristics in the CT measurement region and the HVHC region, respectively. We compared the two types of device models. One was fitted with model A using only the *I–V* data from CT measurements, which is plotted with dotted blue lines in Fig. 9. The other was fitted with model B using datasets from both the CT measurements and the HVHC switching measurements, which is plotted with solid blue lines in Fig. 9. In Fig. 9(a), models A and B both agree well with the experimental curve obtained with the CT. Conversely, in Fig. 9(b), although model A does not agree with the experimental data, model B agrees well with it. In this case, because the slope of I_d–V_{ds} characteristics in the HVHC region is important for the modeling, a few points from the HVHC region were used to fit the simulated curve to the experimental data.

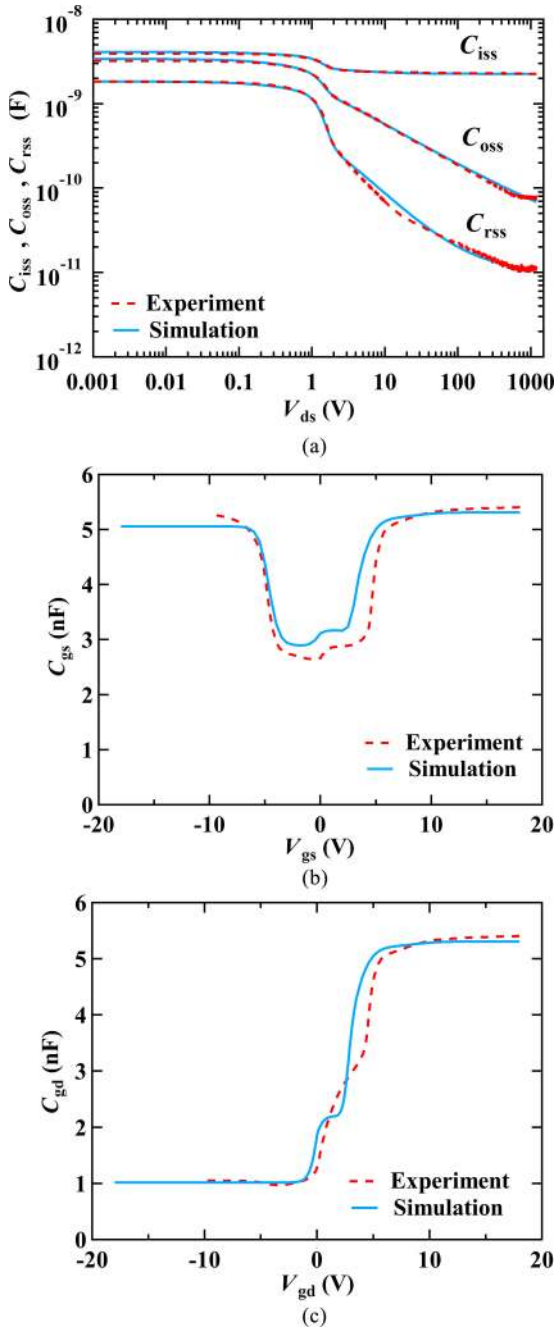

Fig. 10. (a) C_{iss}, C_{oss}, and C_{rss} of off-state SiC MOSFET as a function of V_{ds}. $V_{gs} = 0$ V. (b) C_{gs} of off-state SiC MOSFET as a function of V_{gs}. $V_{ds} = 0$ V. (c) C_{gd} of off-state SiC MOSFET as a function of V_{gd}. $V_{ds} = 0$ V. The broken red lines represent experimental data, and the solid blue lines represent the simulated data after extracting the parameters for the applied device model.

IV. *C–V* Characteristics Measurement

A. *Off-State C–V Measurement*

A *C–V* meter is used to measure the input capacitance (C_{iss}), output capacitance (C_{oss}), and reverse transfer capacitance (C_{rss}) of the SiC MOSFET in the off-state $(V_{gs} = 0\,\text{V})$ at $V_{ds} = 0$ to 1200 V. The red broken lines in Fig. 10(a) represent the experimental data of C_{iss}, C_{oss}, and C_{rss}, as a function of V_{ds}. The gate bias dependence of C_{gs} and C_{gd} was

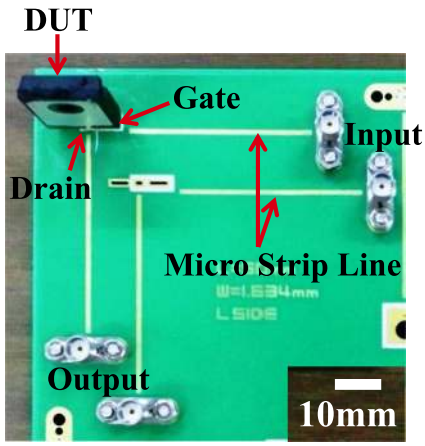

Fig. 11. Evaluation board for measuring S-parameters of SiC MOSFET.

also measured over the range $V_{gs} = -5$ to 18 V, as shown in Fig. 10(b) and (c). The parameters in the polynomial model were optimized to reproduce these *C–V* characteristics. First, the V_{ds} dependence of C_{rss} shown in Fig. 10(a) was fitted with $g_5(V_{ds})$ and $f_{36}(V_{gs}, V_{ds})$ in (13) and the C_{gd}–V_{gd} characteristic in Fig. 10(c) was fitted with $f_{34}(V_{gs}, V_{ds})$ and $f_{35}(V_{gs}, V_{ds})$ in (13). Second, the C_{oss} was fitted with the capacitance parameters of the conventional pn-diode, which was added as a body diode, as shown in Fig. 1. Finally, the C_{iss} and C_{gs}–V_{gs} characteristics were fitted with (11). The simulated *C–V* curves are also shown in Fig. 10 as pale blue solid lines. This figure shows that the simulated capacitances agree well with the experimental data examined over the entire range of V_{ds}, V_{gs}, and V_{gd}.

B. S-Parameter Measurement

S-parameters of the SiC MOSFET were measured by mounting it on a board dedicated to high-frequency response evaluation. The evaluation board comprised an insulating layer made of dielectric material (Megtron4), Copper (Cu) microstrip lines (characteristic impedance $Z_0 = 50\,\Omega$) on the surface, and a Cu ground plane on the backside. SMA connectors were adopted as the input and the output terminals. The configuration of the board is shown in Fig. 11, and the S-parameters were measured using a packaged discrete device mounted on the evaluation board, also shown in the figure.

The measurement frequency ranged from 50 kHz to 3 GHz, and a vector network analyzer was used for measuring the S-parameters. V_{gs} was 0 to +18 V, and V_{ds} was 0 to +3 V, and they were biased for generating various on-states of the device. $I_d = 0$ to 8 A appeared under the measurement conditions employed. The phase shift in the microstrip line was corrected by auto-port-extension through the network analyzer. The S-parameters of the package were obtained by using an EM simulator (EMPro; Keysight Technologies, Inc.), and the S-parameters of the bare die were finally obtained by de-embedding the S-parameters of the package from the measurement results.

We utilized the S-parameter data of the bare die to acquire the parasitic capacitances not only of the off-state devices, but also of the on-state devices. S-parameter data were also used for the confirmation of the frequency dependence of the parasitic capacitances. As explained in Section VI, C_{iss} of the on-state device is necessary to reproduce its switching waveforms accurately [14]. However, capacitances of the on-state device cannot be measured by *C–V* meters because it is difficult to measure the alternating current that induces the parasitic capacitance of the device when the drain current flows. Thus, we employed S-parameter measurement to obtain the gate–drain capacitance C_{gd}, gate–source capacitance C_{gs} of the on-state device. This method is often used for determining the small-signal equivalent circuit parameters of microwave devices [15], [16].

The resulting on-state capacitances C_{gd} and C_{gs} derived from the S-parameters are plotted with a red broken line in Fig. 12. In the figure, $V_{ds} = 3$ V and $V_{gs} = 3$ to 6 V. The simulated curves (pale blue solid lines) of the gate–drain capacitance model $C_{gd} = C_{rss}$ and gate–source capacitance model C_{gs} are also plotted in Fig. 12(a) and (b). These calculated capacitances are extracted solely from the off-state *C–V* measurements shown in Fig. 10. Because S-parameters are measured in the frequency domain, the calculated C_{gd} and C_{gs} were also plotted in the frequency domain, as shown in Fig. 12. In this study, the S-parameters were measured only under limited bias conditions because of the bias tee current limit of 2 A (PSPL5544; TEKTRONIX). However, in the turned-on state, the drain voltage of the device maintains on-voltage (near 0 V), so the S-parameter data at $V_{ds} = 0$ to 3 V are adequate to calculate the C_{gd} and C_{gs} of the on-state from the S-parameters. In addition, the measured C_{gd} data at $V_{gs} > 6$ V is almost overlapped on the data at $V_{gs} = 6$ V, so the date at $V_{gs} = 3$ to 6 V are adequate. Therefore, we show C_{gs} and C_{gd} data at $V_{gs} = 3$ to 6 V in Fig. 12.

From Fig. 12, although the simulated curves of the C_{gs} agree well with the measured curves at frequencies under 10 MHz, the simulated C_{gd} curve is less than the measured data by an order of magnitude. Fig. 12(c) shows the C_{gd} model adapted to match the on-state capacitance features. Comparing Fig. 12(a) and (c) clearly demonstrates that using only off-state measurements insufficiently reproduces the on-state capacitance characteristics. By contrast, the S-parameter measurements explained here constitute a good method to reproduce the on-state capacitance features of a switching device.

The vertical lines in the experimental data in Fig. 12 are likely to be caused by resonance between device capacitance and inductance of the wiring in the test fixture. We believe they have nothing to do with the characteristics of the device and neglected them.

V. Modeling Test Fixture

The test fixture drawn in Fig. 13(a) shows parts of the switching measurement circuit depicted in Fig. 2. The parasitic components in the circuit modify the switching waveforms. Thus, the simulation to predict the switching waveforms must appropriately include the parasitic components of the measurement system. The parasitic components are usually measured using an LCR meter or calculated using an EM simulator, and expressed as lumped-parameter elements. However, construction

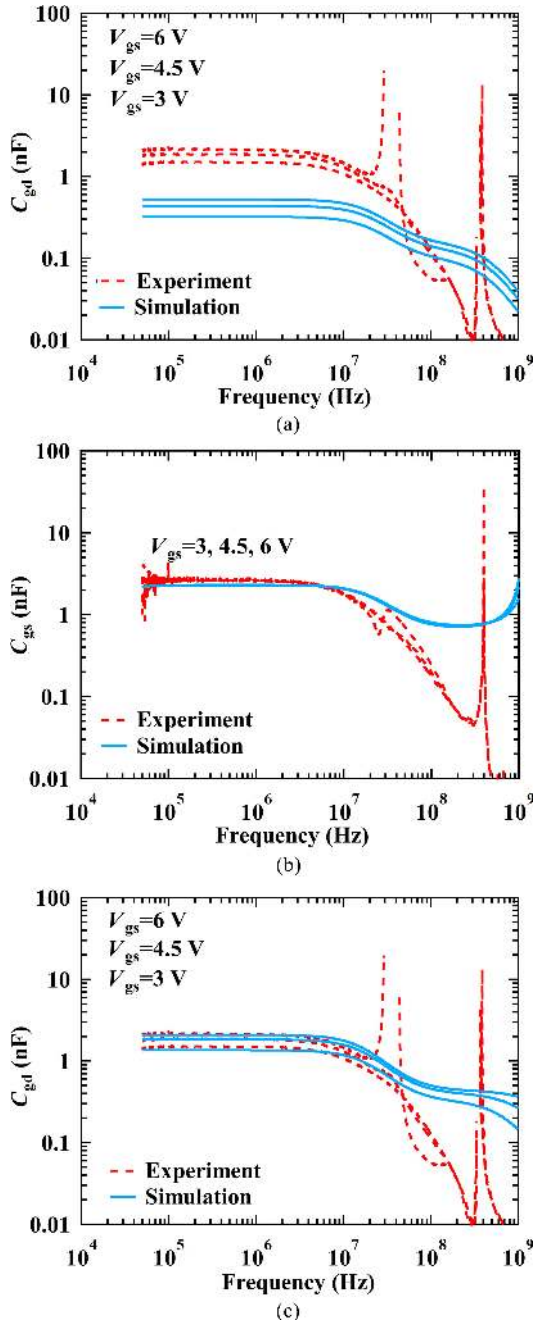

Fig. 12. C_{gd} and C_{gs} as a function of input signal frequency. The red broken lines are the experimental curves, and the blue solid lines are the simulated ones. $V_{ds} = 3$ V. (a) Model expression of C_{gd} in Fig. 10 is used to draw the simulation curves. (b) Model expression of C_{gs} in Fig. 10 is used to draw the simulation curves. (c) Model of C_{gd} optimized to fit the on-state experimental data is used to draw the simulation curves.

of the lumped-parameter equivalent circuit by considering all parasitic components in the measurement system is tedious and time consuming.

Therefore, we modeled the entire test fixture, as shown in Fig. 13(a), calculated its S-parameters with EMPro (Finite Element Method), and imported these S-parameters into the circuit simulator (ADS; Keysight Technologies, Inc.). A circuit schematic for the simulation is shown in Fig. 13(b). The box of blue squares in the figure show the circuit components that

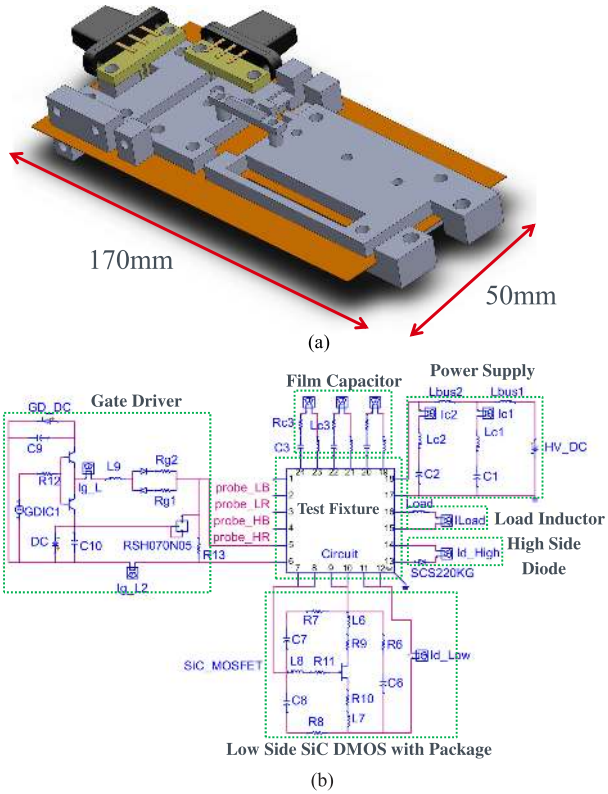

Fig. 13. (a) CAD model of the switching measurement circuit shown in Fig. 2. (b) Schematic for the clamped-inductive-load-switching circuit simulated via ADS.

describe the S-parameters of the test fixture. The SiC MOSFET model comprise a bare die model and an equivalent circuit for the package.

After circuit simulation in the frequency domain was completed, S-parameters were converted to the time domain via a convolution integral method included with ADS. Thus, the S-parameters were analyzed as a circuit component, and parasitic components of the test fixture were considered in the simulation of the clamped inductive load switching circuit shown in Fig. 2.

Finally, to simulate the switching behavior of the SiC MOSFET, we combined all models in ADS: the intrinsic device model extracted above, test fixture model, and SPICE models of the passive circuit components.

VI. Model Validation

A. Measurement Versus Simulation

In this section, we validate SiC MOSFET model made by this characterization technique. The validation was carried out clumped inductive load switching circuit in Fig. 2.

Figs. 14–16 show the experimental results obtained under the operating conditions of $V_{ds} = 600$ V, $I_d = 20$ A, $R_g = 5.6\,\Omega$, and $L = 500\,\mu$H, as well as their simulated counterparts. The measurement circuit is a double pulse tester, as shown in Fig. 3. The switching waveform was obtained using an oscilloscope (DL7480; YOKOGAWA). V_{gs}, V_{ds}, and I_d were measured using

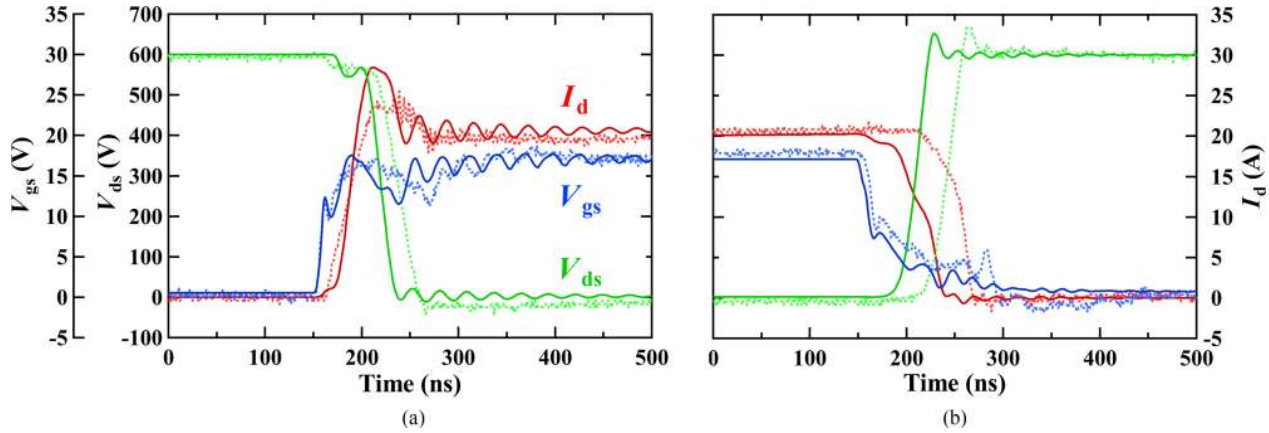

Fig. 14. Switching transient experimental and simulated waveforms of V_{gs}, V_{ds}, and I_d. The device model optimized using the I_d–V_{ds} and off-state C–V properties were employed to obtain the simulation results. (a) Turn-on waveforms. (b) Turn-off waveforms.

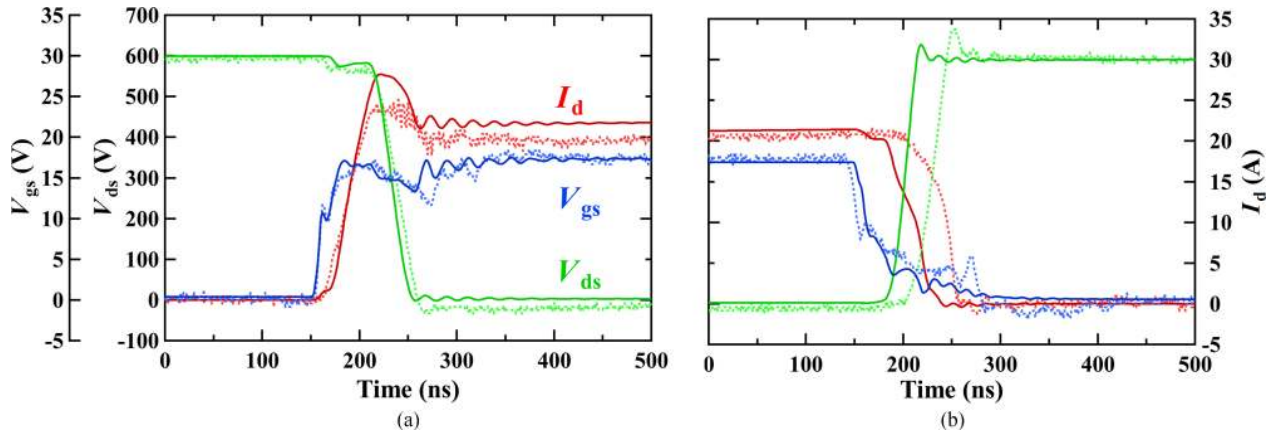

Fig. 15. Switching transient experimental and simulated waveforms of V_{gs}, V_{ds}, and I_d. The device model optimized using the I_d–V_{ds} characteristics shown in Fig. 9 and the off-state C–V properties were employed to obtain the simulation results. (a) Turn-on waveforms. (b) Turn-off waveforms.

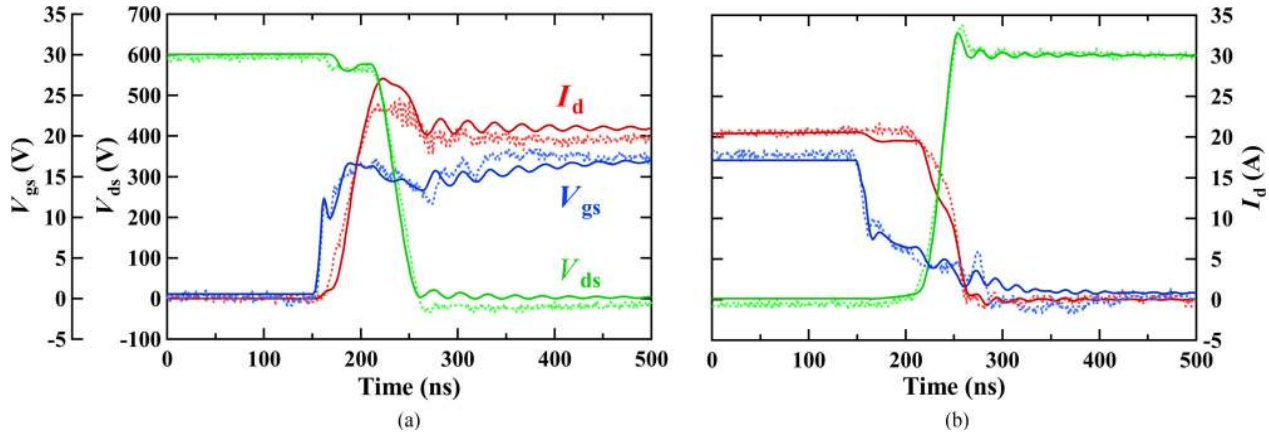

Fig. 16. Switching transient experimental and simulated waveforms of V_{gs}, V_{ds}, and I_d. The device model optimized using the I_d–V_{ds} characteristics shown in Fig. 9 and the off- and on-state C–V properties shown in Figs. 10 and 12 was employed to obtain the simulation results. (a) Turn-on waveforms. (b) Turn-off waveforms.

differential probes (701921 and 700924; YOKOGAWA) and a current probe (model 2877; Pearson) connected to the test fixture in Fig. 13.

In Figs. 14–16, (a) shows turn-on waveforms, and (b) shows the turn-off counterparts. The broken lines denote the experimental data, and the solid lines show the simulated waveforms.

Furthermore, in this section, we describe the development of our device model step-by-step. First, we summarize the results in the simplest simulation configuration in Fig. 14. In the figures, the employed device model (model A) is optimized using the off-state capacitance properties shown in Fig. 10 and the I_d–V_{ds} properties obtained using the CT shown as dotted blue lines in

Fig. 9, ignoring the data shown in Figs. 9(b) and 12(c). This means that the device model used in Fig. 14 do not follow the on-state capacitance characteristics and the $I_{\rm d}$–$V_{\rm ds}$ curves in the HVHC range. Consequently, this device model does not present the time lags and the rise and fall times; in addition, it does not show sufficiently the ringing of the waveforms.

Next, we use the device model (model B), which reproduces the static $I_{\rm d}$–$V_{\rm ds}$ characteristics shown as blue solid lines in Fig. 9, but follows only the off-state *C*–*V* characteristics in Fig. 10. The results are shown in Fig. 15. This model successfully improves the turn-on time lags, $V_{\rm ds}$ decreasing gradient, and $I_{\rm d}$ increasing and decreasing gradients in comparison with the first device model described above. However, the turn-off time lags of the waveforms of $I_{\rm d}$ and $V_{\rm ds}$, which are about 40 ns, remain. Because the turn-off time depends on the discharge time of $C_{\rm iss}$ and the MOSFET is active (in the on-state) before the turn-off period, the turn-off time depends on the $C_{\rm iss}$ of device when it is on-state. Thus, we hypothesize that this mismatch is caused by the insufficient modeling of the on-state $C_{\rm iss}$ characteristics. $C_{\rm iss}$ is expressed as follows:

$$C_{\rm iss} = C_{\rm gs} + C_{\rm gd}. \tag{21}$$

We considered that the $C_{\rm gd}$ and/or $C_{\rm gs}$ of the on-state device might be different from the $C_{\rm gd}$ and/or $C_{\rm gs}$ of the off-state device measured by the *C*–*V* meter [14]. Unfortunately, because we cannot measure the capacitance of the on-state of the device by using a conventional *C*–*V* meter, we measured the S-parameters of the SiC MOSFET and derived the $C_{\rm gd}$ of the on-state device from the S-parameters by using a π–equivalent circuit topology. From this analysis, as for $C_{\rm gs}$, we confirm that the modeled on-state $C_{\rm gs}$ was matched to the measured on-state $C_{\rm gs}$, as shown in Fig. 12(b). Conversely, we found that the modeled $C_{\rm gd}$ did not match the measurement data, as shown in Fig. 12(a). Herein, two methods are available to match the modeled $C_{\rm gd}$ to the measured $C_{\rm gd}$. While one method is changing the model parameters, the other is changing the model equations. Because the simulated off-state capacitances were already matched very well to the measured ones, as shown in Fig. 10, we modified the $C_{\rm gd}$ model equation without changing any model parameters. However, because the $Q_{\rm gd}$ equations (13) and (15) were already rather complex, we modified an existing variable in the $Q_{\rm gd}$ equations (13) and (15). In concrete terms, we changed $V_{\rm ds}$ to $V_{\rm ds} - V_{\rm gs} = V_{\rm dg}$ in (14) and (16). Because $V_{\rm dg} = V_{\rm ds}$ in the off-state ($V_{\rm gs} = 0\,{\rm V}$), the off-state parameters did not need to be changed.

Finally, we use the device model C that considers the on-state capacitance shown in Fig. 12(c), and the results are summarized in Fig. 16. The turn-off time lags in the waveforms of $I_{\rm d}$ and $V_{\rm ds}$ disappear. This shows that the on-state capacitance properties of the device significantly affect the way in which the device transitions from the on-state to the off-state. Furthermore, the change of $g_5(V_{\rm ds})$ to $g_5(V_{\rm dg})$ was sufficient to run out the turn-off time lags and match the simulated capacitance-frequency curves to the measured ones under 10 MHz in Fig. 12(b) and (c).

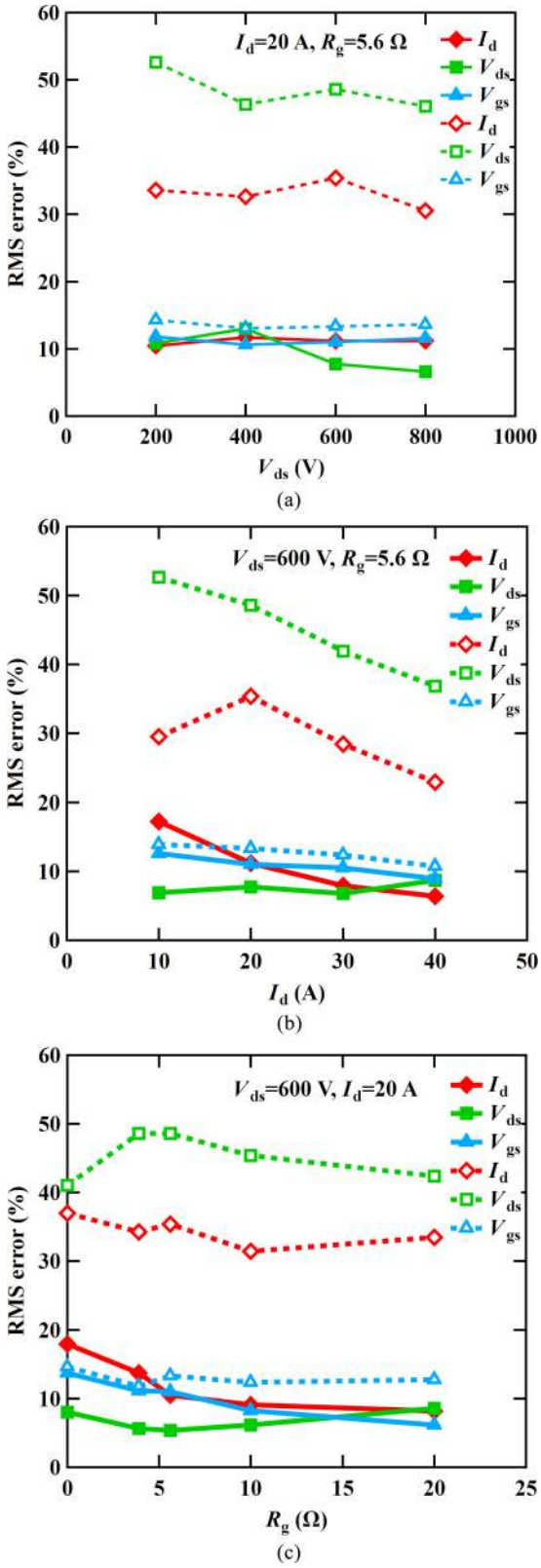

Fig. 17. RMS errors defined by (22) are shown as functions of $V_{\rm ds}$, $I_{\rm d}$, and $R_{\rm g}$ in subpanels (a), (b), and (c), respectively. The common experimental settings for each case are described at the top right corners of the graph panels. The solid lines denote the RMS errors obtained using the proposed device model, whereas the broken lines denote the results obtained using the conventional SPICE device model. (a) RMS errors as a function of $V_{\rm ds}$. (b) RMS errors as a function of $I_{\rm d}$. (c) RMS errors as a function of $R_{\rm g}$.

B. Comparison With Conventional SPICE Model

To further demonstrate the advances facilitated by the proposed measurement and modeling techniques, we compare the new model with the conventional SPICE model, that is, the equation-based model published on the ROHM website [17].

Fig. 14 shows only the switching waveforms when the device operates at $V_{\rm ds} = 600\,{\rm V}$, $I_{\rm d} = 20\,{\rm A}$, and $R_{\rm g} = 5.6\,\Omega$, but the model can also predict the switching behavior in other voltage and current ranges. Here we verify that our model can reproduce measurement waveforms in the operating ranges of $V_{\rm ds} = 200$ to $600\,{\rm V}$, $I_{\rm d} = 10$ to $40\,{\rm A}$, and $R_{\rm g} = 0$ to $20\,\Omega$.

In addition, we use the relative RMS error to validate quantitatively the capability and general versatility of the model.

The RMS error used herein is given as follows:

$$\text{Relative RMS Error} = \sqrt{\frac{\sum_{i=1}^{N} |m_i - s_i|^2}{\sum_{i=1}^{N} |m_i|^2}} \times 100\ [\%] \quad (22)$$

where i, m_i, s_i, and N denote the number of data, measured and simulated values ($I_{\rm d}, V_{\rm ds}$, and $V_{\rm gs}$) at the i-th data point, and total number of data points, respectively. The time domain calculation is defined by the switching cycle, which starts 25 ns before $V_{\rm gs}$ starts to fall or rise and ends 25 ns after $I_{\rm d}$ reaches zero or is saturated.

Fig. 17(a)–(c) shows the RMS errors as a function of $V_{\rm ds}, I_{\rm d}$, and $R_{\rm g}$, respectively. In each graph, the green squares, red diamonds, and blue triangles indicate the RMS errors in $V_{\rm ds}, I_{\rm d}$, and $V_{\rm gs}$, respectively. The unaltered experimental settings are also shown in the same figures. The solid lines denote the results obtained using our device model, and the broken lines denote the results obtained using the conventional SPICE model.

In Fig. 17, the RMS errors obtained using the presently developed device model show a rather flat dependence on $V_{\rm ds}, I_{\rm d}$, and $R_{\rm g}$, which means these device models show the same accuracy as that of the model shown in Fig. 16, even over a wide operation range. Furthermore, in all tested cases, the RMS errors obtained using the presently developed device model is smaller than the ones obtained using the conventional SPICE models. Consequently, our model can successfully predict voltage and current waveforms under various practical power electronics circuit operating conditions.

VII. Conclusion

In this paper, we introduced novel measurement methods to characterize SiC MOSFET devices and new modeling techniques to accurately reproduce their switching behavior. The on-state transient waveforms were improved significantly by using *I–V* data of HVHC range derived from switching waveforms of the SiC MOSFET, thereby preventing device self-heating. The off-state time lag of the transient waveforms was predicted accurately by measuring the capacitance characteristics of the on-state device extracted from the S-parameters of the device. EM simulations were used to de-embed the bare die device model of the SiC MOSFET by removing the parasitic components of the package and to develop a computational model of the test fixture.

To demonstrate the validity and usefulness of the newly obtained measured data, we deployed a custom version of the Angelov–GaN RF model, modified to account for power SiC device behavior. The model can be extracted by using these new measurement techniques.

The new model can predict switching waveforms of the SiC MOSFET device under wider voltage and current operation conditions, and it is significantly more accurate than the existing SPICE models across different bias conditions. In conclusion, because this novel measurement and modeling technology can predict switching waveforms accurately, we believe the solution is valuable for simulating power electronic circuit performance, including estimating precisely their power conversion efficiency and EM noise.

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Hiroyuki Sakairi was born in Tochigi, Japan, in 1982. He received the B.S degree in applied physics from Tokyo University of Science, Tokyo, Japan, in 2007, and the M.Eng. degree in material science from Nara Institute of Science and Technology, Nara, Japan, in 2009.

He joined ROHM Co., Ltd., Kyoto, Japan, in 2009. From 2009 to 2012, he was engaged in development of SiC power devices, and since 2013, he has been working in the development of system applications of power devices and modeling power devices.

Tatsuya Yanagi (M'14) was born in Osaka, Japan, in 1985. He received the B.Eng. degree in electrical and electronic engineering and M.Eng. degree in electrical engineering from Kyoto University, Kyoto, Japan, in 2010 and 2012, respectively.

He joined ROHM Co., Ltd., Kyoto, Japan, in 2012. His research interest includes the behavior of power devices, Si, SiC and GaN power devices, in power converter circuits.

Hirotaka Otake was born in Chiba, Japan, in 1981. He received the B.Eng. and M.Eng. degrees in applied physics from Waseda University, Tokyo, Japan, in 2004 and 2006, respectively.

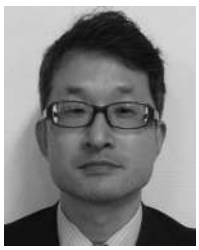
He joined ROHM Co., Ltd., Kyoto, Japan, in 2006. From 2006 to 2011, he was engaged in the development of GaN power devices, and since 2011, has been engaged in the development of power modules and circuits using SiC devices.

Naotaka Kuroda received the B.E. and M.E. degrees in electrical engineering from Kyoto University, Kyoto, Japan, in 1985 and 1987, respectively.

In 1987, he joined the Central Research Laboratories, NEC Corporation, Kawasaki, Japan, where he was engaged in the research and development of compound semiconductor devices. Since 2011, he has been with the Research and Development Division, ROHM Co., Ltd., Kyoto. His current research interests include the modeling of power devices and simulation for the electro-thermal and electromagnetic compatibility design.

Hiroaki Tanigawa received the B.S. degree in electronics engineering from Fukuoka University, Fukuoka, Japan, in 1997.

In 2001, he joined Keysight Technologies Japan G.K. (formerly Agilent Technologies Japan), Tokyo, Japan, where he had a role as a semiconductor device modeling. He is currently a Global Services and Support Engineer for EEsof EDA Organization, Keysight Technologies Japan G.K. His current research interests include electrical characterization/modeling of III-Nitride devices and power semiconductor devices.



Ken Nakahara (M'12) was born in Hyogo, Japan, in 1972. He received the B.S. degree in physics from Kyoto University, Kyoto, Japan, in 1995, and the Ph.D. degree in chemical from Tohoku University, Sendai, Japan, in 2010.

He is the Division Manager of the Research and Development Division, ROHM Co., Ltd., Kyoto. His current research interests include power devices and their applications.