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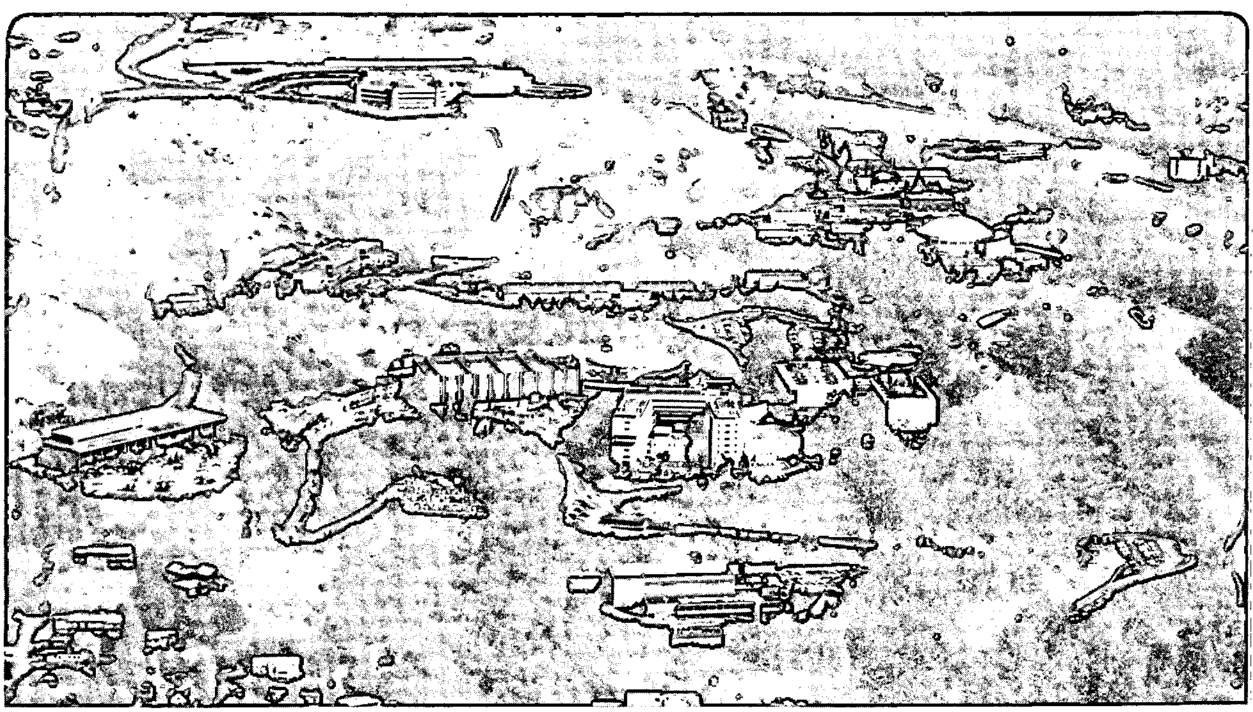

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Measurement of MOS Current Mismatch in the Weak Inversion Region

Francesco Forti and Michael E. Wright *

Abstract

We have measured the current matching properties of MOS transistors operated in the weak inversion region. We measured about 1400 parts produced in four different processes and report here the results in in terms of mismatch dependance on current density, device dimensions and substrate voltage, without using any specific model for the transistor.

1 Introduction

The MOS transistor matching properties in the weak inversion region have not received, in the past, the attention that the mismatch in the strong inversion region has. The importance of weak inversion biased transistors in low power CMOS analog systems calls for more extensive data on the mismatch in this region of operation. The study presented in this paper was motivated by the need of controlling the threshold matching in a low power, low noise amplifier–discriminator circuit used in silicon radiation detector readout, where the transistor dimensions had to be kept to a minimum. The goal is to design a big array of such circuits with a threshold mismatch smaller than the noise figure.

In the literature, there exist a number of theoretical approaches to mismatch modeling, based on certain assumptions on the behaviour of defects that cause the mismatch. Shyu *et al.*[1, 2] analyze the effect of edge roughness, surface state and implanted charge fluctuations, oxide thickness variations and mobility fluctuations in terms of short range (*local*) and long range (*global*) parameter variations. Pelgrom *et al.*[3] introduce a powerful spatial Fourier transform technique to build a general frame in which different transistor geometries can be accommodated. In most cases a more or less elaborate transistor model was used, and the measurements were translated to variations of the model parameters that are hard to extrapolate to regions of operation where that model is no longer valid. Pan and Abidi [4] report weak to strong inversion match without a model, but for only one MOSFET geometry and without transconductance data.

In this paper, considering that the MOS subthreshold region lacks a satisfactory mathematical model, especially in moderate inversion, we have decided to present results in the most direct manner, as drain current mismatch distributions in MOS differential pairs. We will be concerned with the dependance of mismatch on the device dimensions, on the operating point, and will consider a few processes with different oxide thicknesses and feature sizes: MOSIS/HP, MOSIS/Orbit, UTMC and IBM (see Table 1 for more detail). The last two processes are designed to be radiation hard.

2 Measurement description

For each of the four processes, one lot of test dice were produced. Each die lot contained various transistor sizes, as listed in Table 2. All the devices were connected as differential pairs and the two drain currents were measured at the same time to get rid of possible temperature dependencies. We have estimated that in order to perform an absolute measurement in the subthreshold region keeping $\Delta I_D/I_D < 1\%$, we would require a temperature control of about 0.1–0.2°C, which is not possible in our present laboratory setup.

The drain, source and substrate were held at fixed voltage while the two gates were connected together and ramped in the range 0–1.5 V. The two drain currents were measured and recorded on disk for subsequent analysis. Four sets of measurements were collected for each device with V_{DS}= 1 and 2.5 V and V_{SUB}= 0 and −1 V for N-type transistors. Of course, P-type transistors had all signs reversed.

Because of the very small currents that must be measured in the subthreshold region, particular care was devoted to having a clean setup with leakage current below 1 pA.

Process	Feature size (μm)	Well type	Gate Oxide	Number of dice
M/HP	1.2	N	20 nm	42
M/Orbit	2.0	P	40 nm	16
UTMC	1.2	P	20 nm	7
IBM	1.2	N	20 nm	14

Table 1: Process characteristics.

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Process	Drawn W/L (μm)
MOSIS/HP	1.8/4.8, 1.8/1.8, 1.8/1.2, 2.4/1.2, 12/12, 15/1.2, 600/4.8, 600/1.8, 600/1.2
MOSIS/Orbit	3/8, 3/3, 3/2, 4/2, 20/20, 25/2, 1000/8, 1000/3, 1000/2
UTMC	3/1.2, 3/6, 3/30, 15/1.2, 15/6, 75/1.2, 75/30
IBM	NMOS: 2.7/1.3, 50/10, 250/1.3 PMOS: 2.7/1.2, 250/1.2

Table 2: Transitor dimensions.

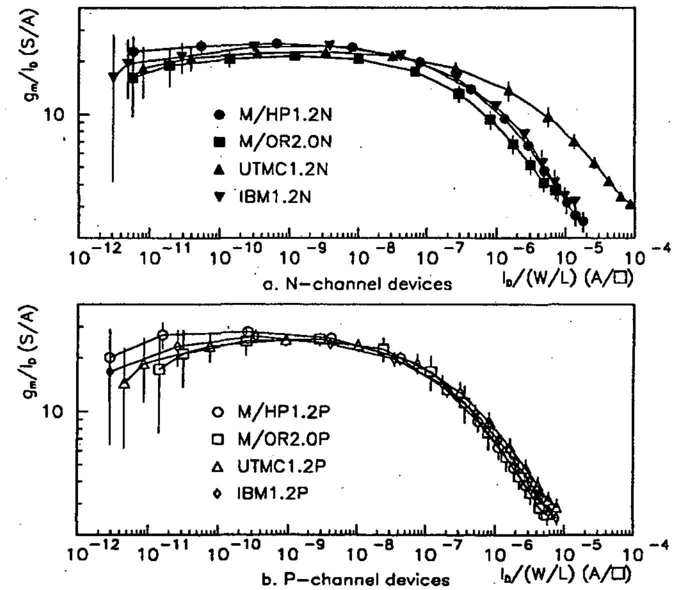

Figure 1: Average g_m/I_D vs. $I_\square$ for all transistor sizes and all processes. The error bars represent the spread of g_m/I_D.

In the offline analysis, the transconductance is computed and plotted in Fig. 1 against the scaled current $I_\square \equiv I_D/(W/L)$. Notably, using this horizontal scale, all transistor sizes fall more or less on the same curve and the points in Fig. 1 represent the average of all transistor sizes for a given process, while the vertical bars represent the spread (standard deviation) of g_m/I_D at a given current level.

In calculating the transconductance, it turned out that a simple finite difference method was not good enough, given the relatively large (0.1 V) V_{GS} ramp step, and we therefore used a logarithmic derivative, $g_m/I_D = \partial \ln I_D/\partial V_{GS}$, together with a second order finite difference approximation[5] to preserve precision. We estimate an error of about 1% on g_m/I_D.

Of the 1400 differential pairs we have tested, we have rejected those that have a low transconductance or a high leakage, or both, that account for about 20 % of the total. It must be noted that these test structures have small or non-existent input protection.

3 Analysis

For each V_{GS} value and each device size we calculated the mean $\overline{\delta}$ and and the standard deviation σ_δ of the quantity $\delta = \Delta I_D/I_D$ where ΔI_D is the difference of the currents in the two transistors of the differential pair. We expected $\overline{\delta}$ to be near 0 and σ_δ to depend on the transistor size as well as on the bias point.

$\overline{\delta}$ is in fact 0 within the measurement errors for most V_{GS} values, except for a few points at high current ($I_D > 1$ mA) in large transistors, where a small difference in the sources resistance of the order of $2\,\Omega$ causes a systematic deviation from 0. We disregard these points.

We also calculated the error on σ_δ in the following way: assuming that the parent distribution is gaussian with an unknown variance σ_δ, elementary statistics states that $(n-1)s_\delta^2/\sigma_\delta^2$ (where s_δ^2 is the sample variance and n is number of sample points) has a chi-squared distribution with $n-1$ degrees of freedom. We plot the 68% confidence interval (C.I.) for the parent σ_δ, calculated from the chi-squared distribution. The 68% C.I. is customary chosen because it corresponds to one standard deviation for gaussian distributions.

In the following sections we first analyze the dependance of σ_δ on the current density and on the device dimensions at a fixed bias, with V_{SUB}= 1 V and the substrate or well grounded. We then measure the effect of changing the bias point.

Current density

For a MOS transistor in strong inversion and in saturation the current mismatch has two contributions coming from the threshold voltage and the current factor mismatch. If V_{GS} is small ($< V_{T0} + 1.5V$), the first term dominates and the overall dependance is roughly $1/\sqrt{I_D}$. At still smaller V_{GS}, when entering moderate and weak inversion σ_δ is expected to flatten out and become essentially independent of the current density. This behaviour is reflected in our data, shown in Fig. 2 for the MOSIS/HP 1.2 μm process, with the notable and as yet not understood exception that small devices with a small W/L ratio (less than about 2) roll off at a much lower rate than expected. The same effect is not present in the slightly coarser MOSIS/ORBIT 2.0 μm process portrayed in Fig. 3. Apart from this effect, the current density dependance can be parametrized by a simple "low–pass" model $\sigma_\delta \propto (1 + I_\square/I_0)^{-1/2}$ with the "corner" current I_0, fairly independent of the process and the device dimension, lying in the range .1–.2 μA/$\square$. The

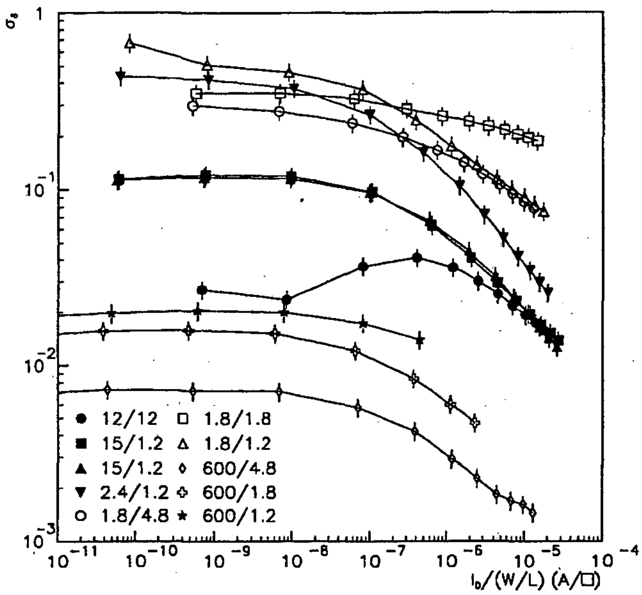

Figure 2: Current mismatch vs. current density for Mosis/HP 1.2 μm NMOS transistors. Note the crossing lines of the small transistors with small W/L ratio.

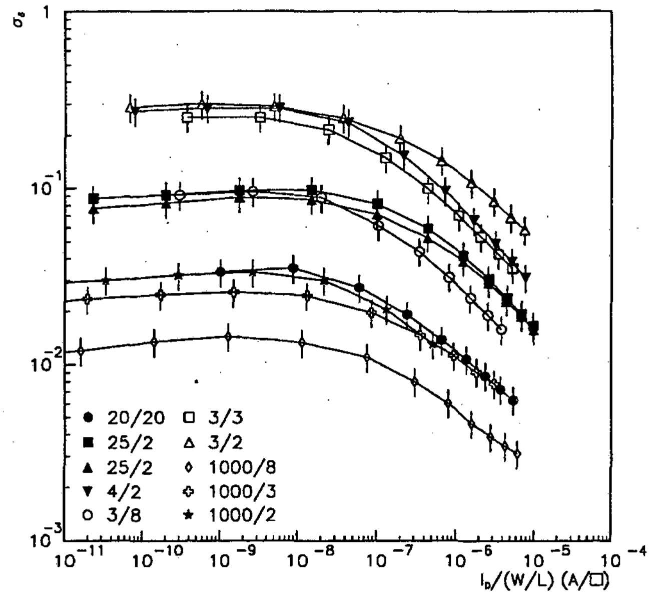

Figure 3: Current mismatch vs. current density for Mosis/Orbit 2 μm NMOS.

same threshold for the onset of strong inversion can be deduced from the transconductance plot.

Device dimensions

We pass now to an analysis of the dependance of the current mismatch on device dimensions at a fixed current level. We have chosen $I_\square \approx 1$ nA/□ because it lies in our range of interest and because σ_δ is fairly independent of current density in that region. Since we have data points only at fixed and rather coarse values of V_{GS}, and we prefer not to interpolate, the definition of the $I_\square$ level is only accurate within a factor of about 10. This uncertainty doesn't really matter thanks to the insensitivity of σ_δ to $I_\square$ in the weak inversion regime.

It is suggested in several papers [3] that the mismatch should be roughly proportional to the inverse of the square root of the area of the device, and we certainly have evidence in Fig. 4 of this general behaviour with a relatively good agreement between different processes. The Mosis/Orbit process, having a thicker gate oxide than the other processes (40 nm instead of 20 nm) is expected to and does have a larger mismatch.

It must be noted, however, that it does not quite follow the $1/\sqrt{WL}$ law, as it's particularly evident for the big transistors and for the PMOS transistors (Fig. 5). Lakshmikumar *et al.*[6] suggest that the higher mismatch of P-channel devices is possibly due to higher mobility variations and poorer gate oxide capacitance matching. We have no explanation for the non $1/\sqrt{WL}$ mismatch scaling, and attempts to explain the measurements with edge variations (see [1]) or long-range (global) parameter variations [3] have failed.

Bias point

To compare the different values of V_{DS} and V_{SUB} we again fix the current density at $I_\square \approx 1$ nA/□ and form the ratio of σ_δ at the new bias point to σ_δ at the base bias (V_{DS}=1 V, V_{SUB}=0 V). We find that there is hardly any dependance in V_{DS}, while there is a significant deterioration with the substrate/well voltage. In Fig. 6 we plot the distribution of $\sigma_\delta(V_{SUB} = 1V)/\sigma_\delta(V_{SUB} = 0V)$ for all device sizes and all processes. It can be seen that on average there is a 50% worsening of σ_δ, although the relatively low statistics and consequent large errors cause the distribution to be rather broad. A possible explanation of this effect goes as follows. When V_{SUB} increases from 0 to 1 V, the depletion region, in the bulk under the channel charge sheet, widens. The back-gate transconductance falls and drain current conduction is less controlled by the back gate. The mismatch causes directly related to surface effects (like oxide charge and thickness variations) now contribute to the overall mismatch more than before.

4 Summary

We have analysed the mismatch properties of MOSFET transistors produced in four different process and operated in the weak inversion region. Using the current per square as a reference, a fairly good uniformity of response

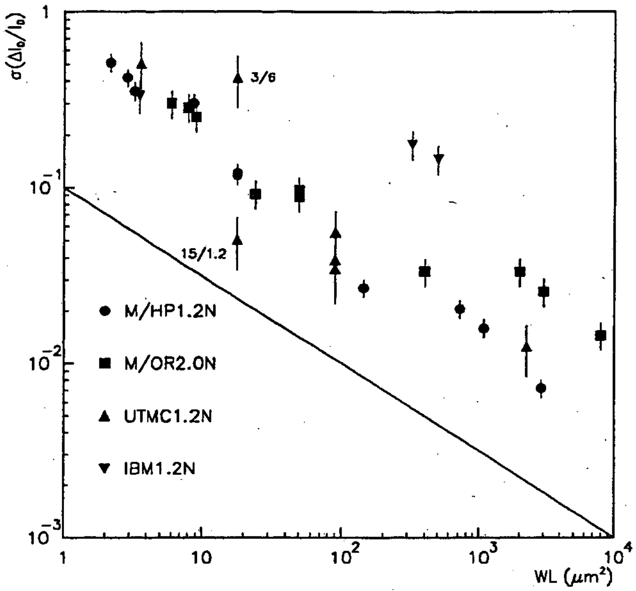

Figure 4: Current mismatch vs. drawn device area for all processes NMOS transistors at $I_{\square} = 1$ nA/□. The straight line represents the slope of the expected $1/\sqrt{WL}$ dependance.

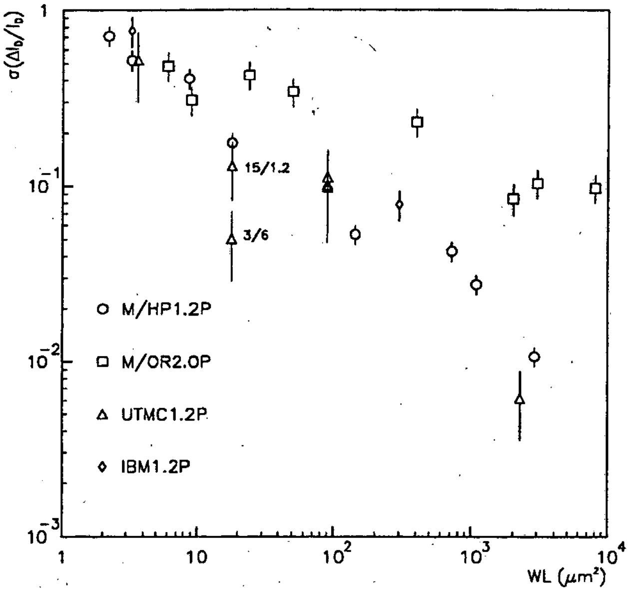

Figure 5: Current mismatch vs. drawn device area for all processes, PMOS transistors at $I_{\square} = 1$ nA/□.

is found over a wide variety of sizes and V_{GS} values. The current density dependance of the current mismatch shows a plateau at low currents that we have further analysed in terms of device area and substrate voltage. The expected inverse square root of area behaviour is found for most processes, with the notable exception of the MOSIS/Orbit P-channel devices. A worsening of the current mismatch is observed when a substrate voltage is applied.

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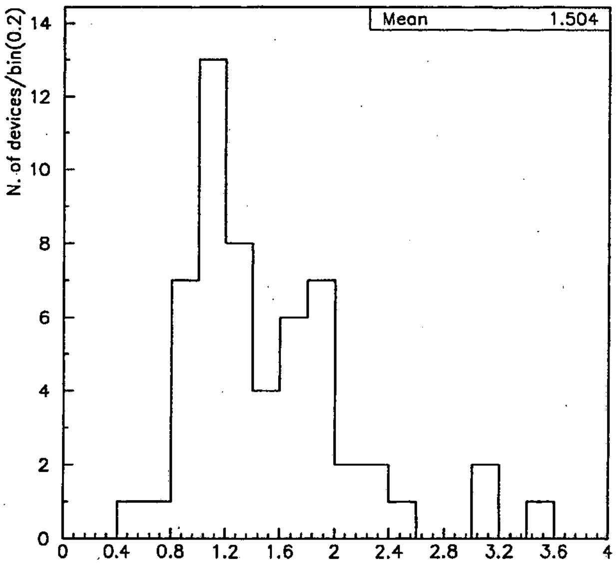

Figure 6: Distribution of the ratio $\sigma_\delta(V_{SUB} = 1\text{ V})/\sigma_\delta(V_{SUB} = 0\text{ V})$ for all device at $I_{\square} = 1$ nA/□.

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