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Measurement of proton induced radiation damage to CMOS transistors and p-i-n diodes — Source link

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MEASUREMENT OF PROTON INDUCED RADIATION DAMAGE TO CMOS TRANSISTORS AND PIN DIODES

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Abstract

As part of our program to develop a silicon tracking device for the SSC we have exposed radiation-hard CMOS transistors and PIN diodes to the 800 MeV LAMPF proton beam. The fluences accumulated in a week corresponded to the expected radiation levels of about 10 SSC years. We determine the leakage current constants for PIN diodes and threshold voltage shifts for CMOS transistors under different biasing conditions.

One of the main requirements for detectors and front-end electronics at the SSC is to be radiation-resistant. The SSC Workshop on Radiation Levels in the SSC [1] found that, for example, a silicon tracking device at a radius of 10 cm has to survive a yearly dose of about 0.3 MRad due to charged particles and a yearly neutron fluence of a few times 10^{12} neutrons/cm^2 at the design luminosity of 10^{33} cm^{-2}sec^{-1}.

For our program to develop a large tracking device based on Si μ strip detectors for the SSC [2], an important part is the identification of radiation hard VLSI technologies for the front-end electronics and the testing of the radiation damage of silicon detectors. The pipe lining of the data requires a low power technology and thus we are building a digital time slice chip (DTSC) in the form of a SRAM in CMOS [3]. There is a question as to the radiation hardness of MOS transistors under irradiation by ionising particles [4] and neutrons [5]. On the other hand, radiation-hard CMOS processes have been developed in the last years and are now commercially available [6].

To compare different CMOS technologies, we have tested the radiation resistance of various VLSI technologies at Los Alamos National Laboratory. We have reported [7] before on the irradiation of n and p transistors on 2 μm CMOS test structures with neutrons in the LAMPF neutron spallation source. We have now extended our measurement to 800 MeV protons in the HRS line at LAMPF. To determine the proton fluence [8], the activation of an aluminum foil covering the active area of each test structure was measured. Both ^{7}Be and ^{22}Na production were determined from their respective γ decay rate as measured by a 17% hyperpure Germanium detector. The fluences obtained from both isotopes agree well after a correction for the different lifetimes. The radiation damage effects have been determined from measurements of current-voltage characteristics employing the Hewlett-Packard Model 4145B Semiconductor Parameter Analyser.

For digital application the radiation damage to CMOS transistors is characterised by a shift of the threshold voltage V_{th}, i.e., the gate voltage at which the transistor turns on. We have tested transistors of 1.2 μm feature size pro-

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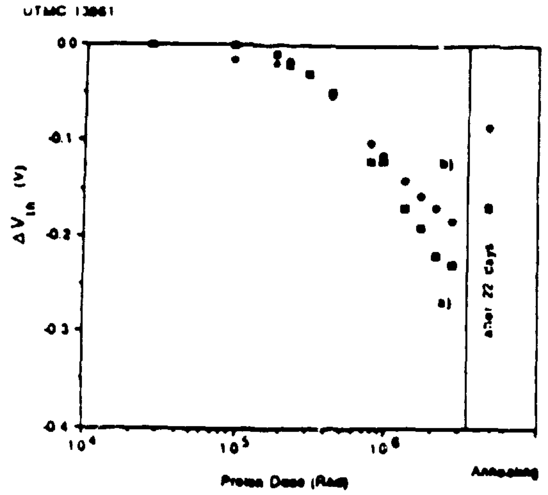

Fig. 1. Threshold voltage shift ΔV_{th} for UTMC transistors as function of fluence and after unbiased room temperature annealing of 22 days. a) p transistor (W/L = 50/1.6μm) [Bias: $V_{Gate} - V_{Substrate}$ =−5 V]. b) n transistor (W/L = 50/1.4μm) [Bias: $V_{Gate} - V_{Substrate}$ = 5 V].

duced by UTMC [9]. The damage on a few representative transistors was tracked during the exposure. All the transistors were analysed 22 days after the end of the exposure, subject to room temperature annealing without bias. In Fig. 1 we show for one p and one n transistor the threshold voltage shifts ΔV_{th} as a function of fluence during exposure and 22 days after exposure. We can see clearly the saturation effect during exposure and the rebound during annealing, similar to the data of Ref. 10. In Figs. 2 and 3 we show ΔV_{th} after doses of 2.7 MRad (10^{14} protons/cm^2) and 22 days annealing for many different transistor sizes (width/length) and for several biasing conditions during irradiation. The observed threshold voltage shifts for worst case biasing are of the order of $\Delta V_{th} \approx$ 150 mV for p transistors (Fig. 2b) and $\Delta V_{th} \approx$ 100 mV for n transistors (Fig. 3b). They show that the UTMC process is radiation hard into the many MRad. With this performance we can expect sufficient radiation resistance for application in the SSC, LHC and HERA.

We tested PIN photo diodes #S1723 produced by Hamamatsu Photonic [11]. They deplete at voltages between 20 and 25 V. Six diodes were subjected to low fluxes ($3 \cdot 10^6$ cm^{-2} s^{-1}) for 128 hours and six diodes were subjected to high fluxes ($2 \cdot 10^8$ cm^{-2} s^{-1}) for 174 hours, giving fluences of approximately 10^{12} and 10^{14} protons/cm^2 respectively. In each case two of the six diodes were left unbiased. The biasing voltage during irradiation was 40 V. The leakage current was checked in constant time intervals.

We define the leakage current constant α as follows

$$\frac{i_l}{\mathrm{Vol}} = \alpha \cdot \Phi$$

where i_l is the increase in leakage current, Vol is the diode

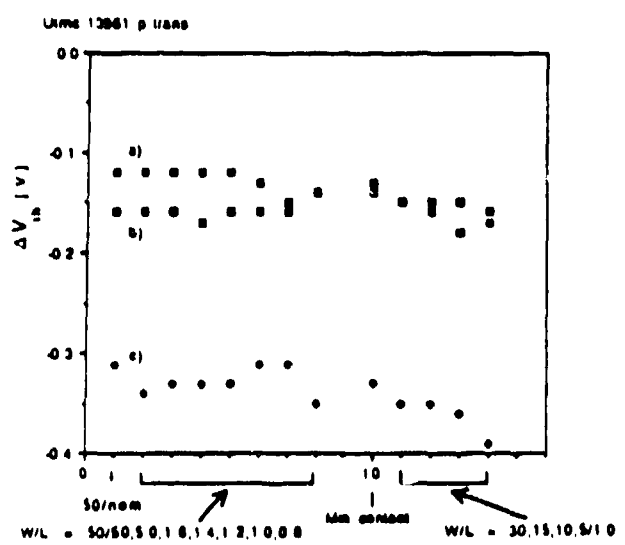

Fig. 2. Threshold voltage shift ΔV_{th} for UTMC p transistors of various sizes (W/L = width/length in μm) after a dose of 10^{14} protons/cm^2 and unbiased room temperature annealing of 22 days for different biasing conditions during exposure: a) unbiased, b) $V_{Gate} - V_{Substrate}$ =−5 V. c) $V_{Gate} - V_{Substrate}$ = 5V.

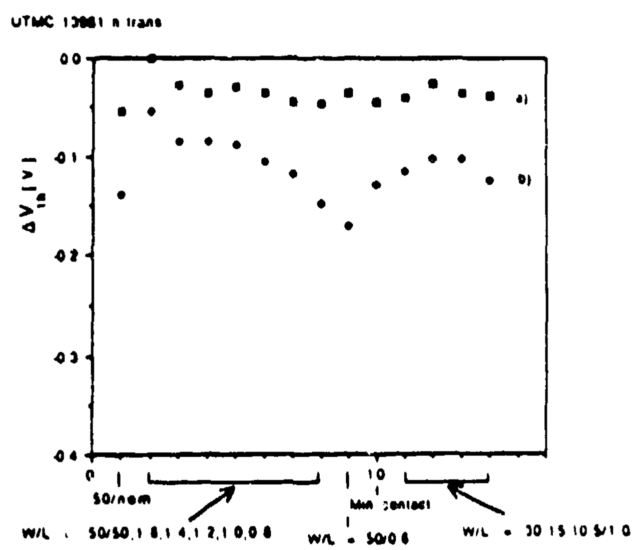

Fig. 3. Threshold voltage shift ΔV_{th} for UTMC n transistors of various sizes (W/L = width/length in μm) after a dose of 10^{14} protons/cm^2 and unbiased room temperature annealing of 22 days for different biasing conditions during exposure: a) unbiased, b) $V_{Gate} - V_{Substrate}$ = 5 V.

Table 1
Average Leakage Current Constants

FLUX	BIASED	α (A/cm)
Low	Yes	$(4.57 \pm 0.63) * 10^{-17}$
Low	No	$(4.36 \pm 0.69) * 10^{-17}$
High	Yes	$(3.94 \pm 0.30) * 10^{-17}$
High	No	$(3.86 \pm 0.37) * 10^{-17}$

volume and Φ the proton fluence. In Table 1, we show the average leakage current constants for the diodes. Note that we find the same leakage current constant for the biased diodes and for unbiased ones. Moreover, we find that the average leakage current constants for high flux $[\alpha_H = (3.91 \pm 0.29) * 10^{-17}$ A/cm$]$ agree with the ones for low flux $[\alpha_L = (4.51 \pm 0.62) * 10^{-17}$ A/cm$]$ within the errors. These leakage current constants are somewhat lower than for 1 MeV neutrons [12].

We have measured room temperature annealing of diodes without further biasing after 29 days and 58 days for low flux and 21 days and 50 days for the high flux samples. Parametrizing the annealing by the function

$$i(t) = i_i \exp(-t/\gamma)$$

we find that the average annealing time factor γ is $\gamma_L = (124 \pm 28)$ days for the low flux and $\gamma_H = (139 \pm 36)$ days for the high flux sample. We also find that the annealing stops after the current reaches about 50% of the initial current i_i. Both observations are in agreement with data of Ref. 13.

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