Measurement on Snapback Holding Voltage of High-Voltage LDMOS for Latch-up Consideration

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Abstract—In high voltage (HV) ICs, the latch-up immunity of HV devices is often referred to the TLP-measured holding voltage because the huge power generated from DC curve tracer can easily damage HV device during measurement. An n-channel lateral DMOS (LDMOS) was fabricated in a 0.25-μm 18-V bipolar CMOS DMOS (BCD) process to investigate the validity of TLP-measured snapback holding voltage to the device immunity against latch-up. Experimental results from curve tracer measurement and transient latch-up test show that 100-ns TLP underestimates the latch-up susceptibility of the 18-V LDMOS. By using the long-pulse TLP measurement, snapback holding voltage of the HV device has been found to degrade over time due to the self-heating effect. As a result, since the latch-up event is a reliability test with the time duration longer than millisecond, TLP measurement is not suitable for applying to investigate the snapback holding voltage of HV devices for latch-up.

I. INTRODUCTION

With the rapidly increasing demands on high voltage (HV) ICs in field applications such as automotive electronics, power management ICs, LED and LCD driver ICs, HV devices have been widely used in nowadays IC products. In HV ICs, the power supply voltage (V_{DD}) can be over ten volts, a few tens of volts, or even higher. To fabricate devices those can sustain such high voltage, not only the process complexity but also the difficulty to guarantee the reliability of HV ICs are increased.

To ensure the reliability and effectiveness of an ESD protection design, it has been generally approved that the I-V characteristics of an ESD protection device should locate within the ESD protection window. The ESD protection window defines the trigger voltage (V_{t1}) of ESD protection devices to be smaller than both junction and gate-oxide breakdown voltages of internal circuits ($V_{BD,Internal}$), so that ESD protection devices can successfully protect internal circuits from being damaged by ESD energy. Although the $V_{t1} < V_{BD,Internal}$ ensures that ESD protection device can effectively clamp down the ESD transient voltage to protect the internal circuits, the snapback holding voltage (V_h) smaller than V_{DD} voltage can result in the latch-up issue. The latch-up issue can arise from the mis-triggering of ESD protection devices under normal circuit operation condition with noise inputs. The ESD protection window is depicted in Fig. 1, where V_{t1} should be smaller than $V_{BD,Internal}$ to ensure successful protection, and V_h should be higher than V_{DD} to accomplish a latch-up free design.

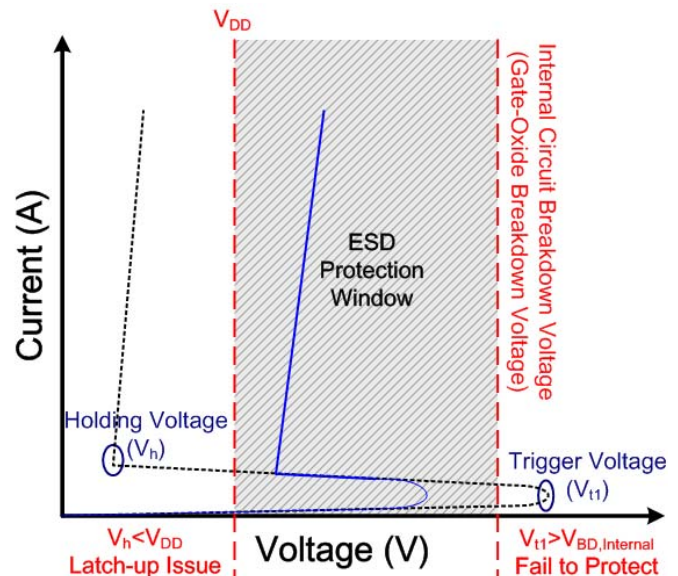

Figure 1. Typical device I-V curve showing the ESD protection window of ESD protection devices.

In HV ICs, due to the high operating voltage in field applications of HV devices, latch-up issue has therefore become one of the main concerns, especially on the power-rail ESD protection devices [1]-[3]. Moreover, the base push-out of n-channel lateral DMOS (LDMOS) under ESD stress has been reported to result in large avalanche multiplication factor (M) [4]. The large M factor results in strong snapback and low holding voltage of n-channel LDMOS. Consequently, ESD design effort is usually focused on increasing the

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holding voltage and minimizing the latch-up sensitivity in HV ICs.

II. Holding Voltage Measurement on High Voltage ICs

To analyze the device characteristics under ESD stresses, 100-ns transmission-line-pulsing (TLP) system has been widely adopted to measure device parameters such as trigger voltage, snapback holding voltage, and secondary breakdown current (I_{t2}) [5]. TLP is a system which pre-charges the transmission line (T-line) through a high-voltage power supply and then discharges the precharged energy into the device under test (DUT). T-line of a TLP system is equivalent to an impedance-matched capacitor which generates a square wave to stress the DUT. While gradually increase the precharged voltage on T-line, TLP system is capable of measuring the snapback I-V characteristics of devices. Different from the 100-ns TLP system, a traditional curve tracer which sweeps a low-frequency voltage sine wave over the DUT can measure the snapback I-V characteristics, too. The frequency of the sine wave is low enough, so that the curve tracer measurement is considered as a DC measurement. At the same time, due to the long measurement duration, a curve tracer may damage the DUT especially under the snapback I-V measurement. Therefore, the snapback holding voltages measured from the 100-ns TLP are sometimes regarded as reference data to latch-up sensitivity in IC industry.

In this work, the snapback holding voltages of an ordinary power-rail ESD protection device in high voltage CMOS ICs, the n-channel LDMOS, have been investigated by TLP systems with different pulse widths and curve tracer. Transient latch-up (TLU) test was exploited to validate the measurement results.

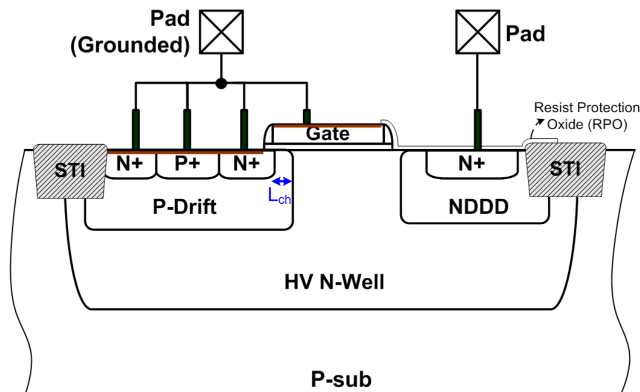
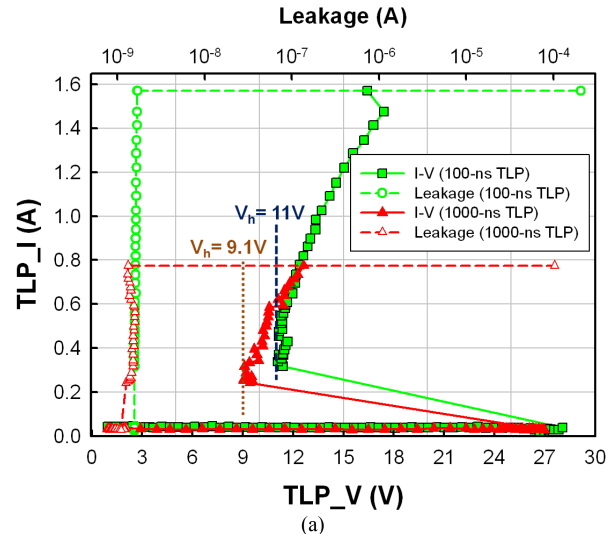


Figure 2. Device cross-sectional view of the n-channel LDMOS in an 18-V BCD process.

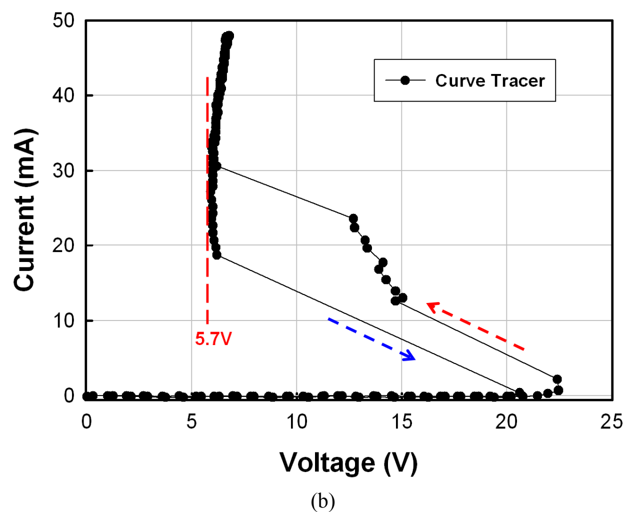
III. Device Structure and Experimental Results

The device cross-sectional view of the n-channel LDMOS in a 0.25-µm 18-V BCD process is shown in Fig. 2. The N+ extension from the drain contact and the gate length L_{ch} (poly gate overlap P-Drift) of the n-channel LDMOS are optimized for ESD robustness in this work. Gate and source electrodes of the n-channel LDMOS are shorted together through internal metal wiring. The n-channel LDMOS is laid out in finger type with each finger width of 50µm, and the total device width is 400µm.

Device secondary breakdown current measured by TLP is usually adopted as a reference of ESD robustness. In order to approximate the device characteristics under human-body-model (HBM) ESD stresses, typical pulse width of TLP system is 100ns [5]. The I-V characteristic of the n-channel LDMOS under 100-ns TLP measurement is shown in Fig. 3(a) (in square). Steps of the T-line pre-charge voltage are 0.5V, and the TLP I/V are the averaged data of the measured current/voltage waveforms from 50% to 90% of the pulse period. I_{t2} of the n-channel LDMOS with a channel width of 400µm is 1.5A, and the corresponding HBM ESD robustness can be over the general requirement of 2kV. From the 100-ns TLP measurement, the n-channel LDMOS shows a snapback holding voltage of 11V. However, distinct from the results of low voltage devices, the holding voltage of n-channel LDMOS under curve tracer measurement shows a substantial inconsistency to that measured by 100-ns TLP. As shown in Fig. 3(b), the snapback holding voltage of n-channel LDMOS under curve tracer measurement is 5.7V only.



(a)

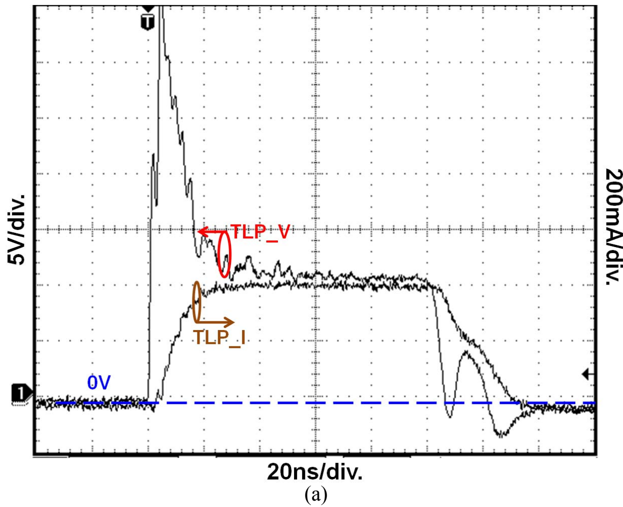


(b)

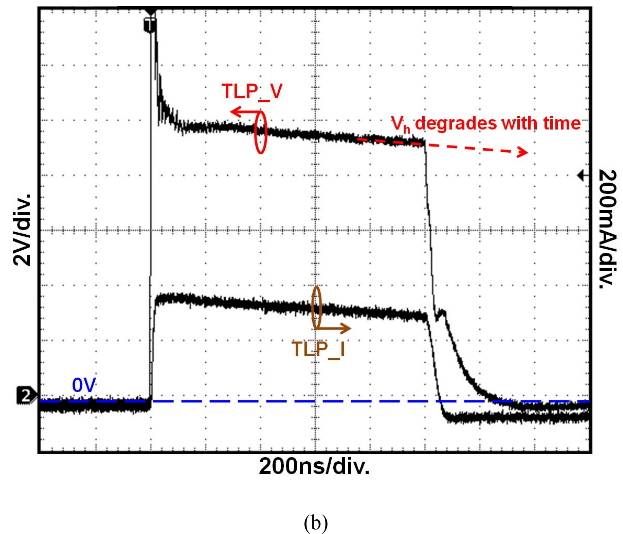
Figure 3. The I-V characteristics of the n-channel LDMOS measured by (a) 100-ns and 1000-ns TLP, and (b) DC curve tracer.

From the 100-ns TLP measurement and curve tracer measurement, snapback holding voltage of the LDMOS shows quite a inconsistency. To investigate such a huge V_h roll off from 100-ns TLP (11V) to curve tracer (5.7V), long-pulse TLP system with 1000-ns pulse width [6] was exploited. The long-pulse TLP system is capable of providing pulse widths longer than100ns, so that the time-domain device behavior of HV devices after 100ns can be further observed.

Measurement result of the 1000-ns TLP is appended in Fig. 3(a) with the measurement result of 100-ns TLP. As the measured result shown in Fig. 3(a) (in solid triangle), n-channel LDMOS under 1000-ns TLP has V_h of 9.1V, which is lower than the V_h under 100-ns TLP measurement but higher than the V_h under curve tracer measurement.



(a)



(b)

Figure 4. The time-domain waveforms of n-channel LDMOS under (a) 100-ns TLP and (b) 1000-ns long-pulse TLP measurement.

IV. MEASUREMENT ANALYSIS AND LATCH-UP SUSCEPTIBILITY OF THE LDMOS

For further investigation of the holding voltage degradation over time, corresponding time-domain current and voltage waveforms of 100-ns and 1000-ns TLP measurement are shown in Figs. 4(a) and 4(b). In the 100-ns TLP measurement shown in Fig. 4(a), the TLP_V is clamped down by the LDMOS after the voltage on transmission line exceeds the bipolar trigger voltage of LDMOS. TLP_V is therefore clamped down to 11V, as the measured V_h value in Fig. 3(a). However, for the 1000-ns TLP measurement, a perceptible voltage drop over time is observed, as shown in Fig. 4(b).

From the Wunsch-Bell model [7], the simplified temperature model under the power source of a rectangular pulse can be expressed as

$$T(0,\tau) = \frac{q_0}{\sqrt{\pi D}}\sqrt{t} \quad \text{, where } t < \tau \qquad (1)$$

As a result, device temperature increases with time (t) during the duration of TLP pulses (τ). In high-voltage devices, the high device holding voltages can further accelerate the self-heating effect. With the increasing device temperature over time, β-gain of the parasitic bipolar inherent in n-channel LDMOS also increases. The holding voltage of n-channel LDMOS therefore degrades while the time increases, as the waveform shown in Fig. 4(b).

To estimate the degradation rate of the holding voltage under long-pulse TLP measurement, waveforms of the 1000-ns TLP measurement are appended with 1500-ns TLP measurement, as shown in Fig. 5. From the measurement result, waveforms of the 1000-ns TLP and 1500-ns TLP fully overlapped to each other except that waveforms of 1500-ns TLP measurement extend the additional 500ns. As a result, the self-heating speed of the LDMOS is found to be 1.5V/μs. Extrapolating from the measured voltage waveform in Fig. 4(b) with the 1.5V/μs self-heating speed, the time for n-channel LDMOS to reach V_h of 5.7V (that measured by curve tracer) is estimated as 3.2μs.

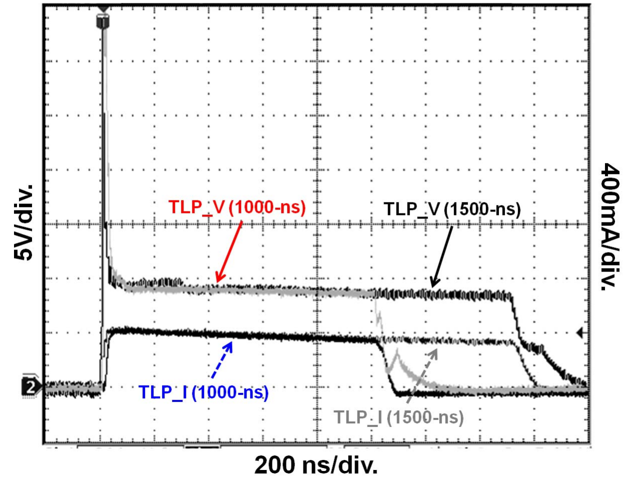


Figure 5. The time-domain waveforms of n-channel LDMOS under 1000-ns and 1500-ns long-pulse TLP measurement.

The measured snapback holding voltages under different TLP pulse widths are summarized in Fig. 6, where the snapback holding voltages under 100-ns, 500-ns, 1000-ns, and DC measurement are 11V, 9.7V, 9.1V, and 5.7V, respectively. The degradation phenomenon on holding voltage of a silicon controlled rectifier (SCR) device has also been reported in [8]. From the measurement result in [8], snapback holding voltage of the SCR at 100ns is ~8V and degrades to ~6V at 1000ns.

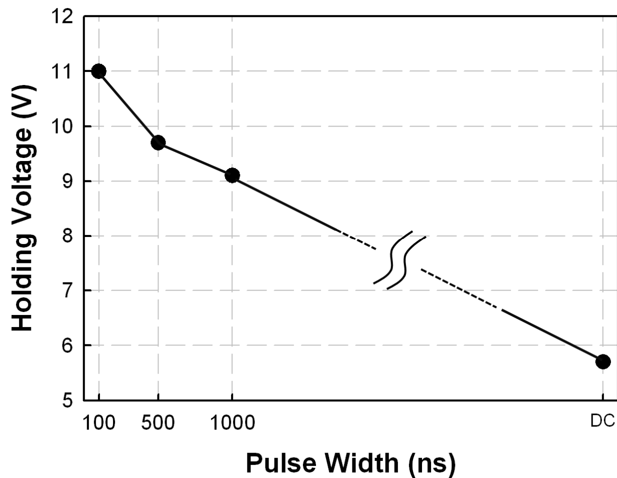


Figure 6. Snapback holding voltages of the 18-V n-channel LDMOS under TLP measurement with different pulse widths.

Transient latch-up test has been verified as an effective test method to evaluate the susceptibility of CMOS ICs to the latch-up induced by transient noises in field applications [9]–[11]. The test setup for TLU is shown in the inset of Fig. 7. In the TLU test, the n-channel LDMOS was initially biased at normal circuit operating voltage, 18V. A transient noise is injected into n-channel LDMOS from the transient trigger source with precharged voltage V_{charge} of +30V. After the transient triggering, the n-channel LDMOS was driven into latch-up state and clamped down the supply voltage. From the measured voltage waveform of TLU test in Fig. 7, the n-channel LDMOS clamped the supply voltage to ~5.7V, which is the same value of V_h under curve-tracer measurement. Moreover, time for n-channel LDMOS to clamp the supply voltage into a steady state is roughly around 1000ns, whereas the voltage at 1000ns under 1000-ns TLP measurement in Fig. 4(b) is ~9V. The difference on the settling time between TLU and long-pulse TLP measurement can come from the larger peak voltage under TLU test, which results in the higher impact ionization current and the shorter settling time. In consequence, the TLU test has obviously verified that the TLP system overestimates the snapback holding voltage of an HV device, which in turn could underestimate its susceptibility to latch-up.

V. CONCLUSION

The snapback holding voltage of n-channel LDMOS in a high voltage BCD process has been investigated by TLP measurements with different pulse widths and DC curve tracer. It is found that the snapback holding voltages of an 18V n-channel LDMOS measured by 100-ns TLP system and curve tracer are substantially different, 11V and 5.7V, respectively. The self-heating effect which degrades the snapback holding voltage of n-channel LDMOS over time has been observed. By using the long-pulse TLP, the self-heating speed of the HV transistors can be quantitatively estimated, where the 1.5V/μs self-heating speed has been found in this work. TLU test further verifies that TLP systems overestimate the snapback holding voltage of n-channel LDMOS and underestimate its susceptibility to latch-up. As a result, TLP measurement is not suitable for applying to investigate the snapback holding voltage of HV devices for latch-up, whereas the latch-up event is a reliability test with the time duration longer than millisecond.

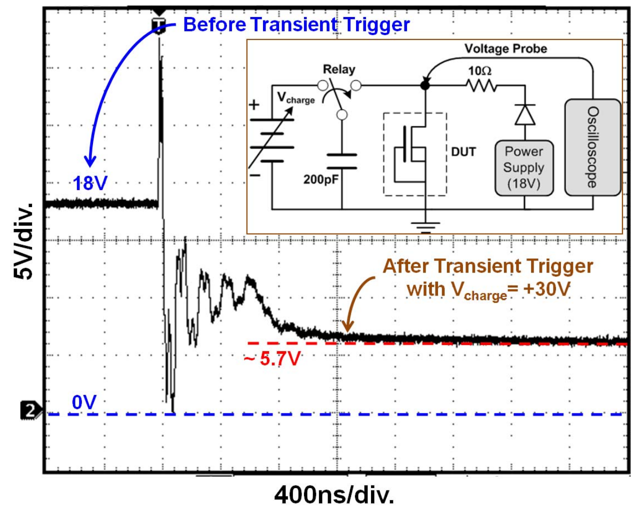


Figure 7. The time-domain voltage waveform of n-channel LDMOS under transient latch-up measurement with initial positive V_{charge} of 30V.

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