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Invited Paper

Mechanically Flexible Optically Transparent Silicon Fabric with High Thermal Budget Devices from Bulk Silicon (100)

Muhammad M. Hussain*[a], Jhonathan P. Rojas[a], Galo A. Torres Sevilla[a]
[a]Integrated Nanotechnology Lab, Electrical Engineering, Computer Electrical Mathematical Science and Engineering Division, King Abdullah University of Science and Technology, Thuwal 23955-6900 Saudi Arabia

ABSTRACT

Today's information age is driven by silicon based electronics. For nearly four decades semiconductor industry has perfected the fabrication process of continuingly scaled transistor – heart of modern day electronics. In future, silicon industry will be more pervasive, whose application will range from ultra-mobile computation to bio-integrated medical electronics. Emergence of flexible electronics opens up interesting opportunities to expand the horizon of electronics industry. However, silicon – industry's darling material is rigid and brittle. Therefore, we report a generic batch fabrication process to convert nearly any silicon electronics into a flexible one without compromising its (i) performance; (ii) ultra-large-scale-integration complexity to integrate billions of transistors within small areas; (iii) state-of-the-art process compatibility, (iv) advanced materials used in modern semiconductor technology; (v) the most widely used and well-studied low-cost substrate mono-crystalline bulk silicon (100). In our process, we make trenches using anisotropic reactive ion etching (RIE) in the inactive areas (in between the devices) of a silicon substrate (after the devices have been fabricated following the regular CMOS process), followed by a dielectric based spacer formation to protect the sidewall of the trench and then performing an isotropic etch to create caves in silicon. When these caves meet with each other the top portion of the silicon with the devices is ready to be peeled off from the bottom silicon substrate. Release process does not need to use any external support. Released silicon fabric (25 μm thick) is mechanically flexible (5 mm bending radius) and the trenches make it semi-transparent (transparency of 7%).

Keywords: Flexible, transparent, mono-crystalline, bulk silicon (100), semiconductor.

1. INTRODUCTION

Silicon has played vital role to create today's information centered world. Computation, communication, navigation, high-resolution displays, sensors, and such electronics are enabling convenience to our complex lifestyle. For over four decades, semiconductor industries have continuously expanded its influence in our life and in world economy by contributing one third of it. Semiconductor industries heart and soul have depended on silicon – an excellent semiconductor with great electrical characteristics, suitable mechanical properties and natural abundance to make it affordable in price. In addition its natural oxidized form is a great insulator and it can be doped suitable to tune its electrical properties. All these unique attributes have made it the first choice for expansion of electronics industry. Silicon's main usage has been in building a tiny switch which is known as transistor (Figure 1).

2. TREND IN HIGH TECH WORLD

More specifically a metal oxide semiconductor field effect transistor (MOSFET) which operates on three basic principles:

$$I_d \approx \mu \frac{W}{l} C_{ox}(V_g - V_t)^n \qquad \tau = \frac{C_g V_{dd}}{I_d} \qquad P_{off} = W_{total} V_{dd} I_{off}$$

In these equations, I_d = Drive current

μ = Channel mobility (substrate property)

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W = Width of the MOSFET

l = Length of the MOSFET channel (gate length)

C_{ox} = Dielectric capacitance = Dielectric constant/dielectric thickness

τ = Delay in inverter

C_g = Gate capacitance

V_{dd} = Drive-in voltage

P_{off} = Stand-by power

W_{total} = Total width of all the turned-off devices

I_{off} = Average off-current per device width at 100 °C

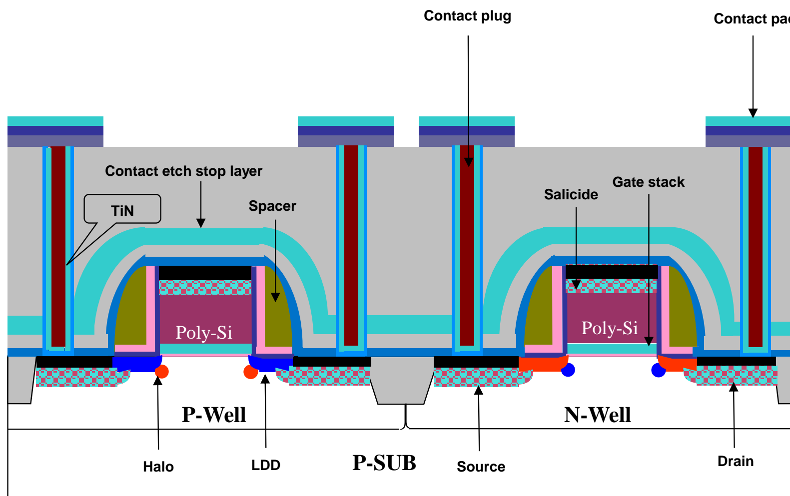

Figure 1. Schematic of a complementary metal oxide semiconductor field effect transistor – popularly known as CMOS.

For high performance computation we need to reduce the inverter delay and thus increasing the drive current is critical. In the past, just by simple scaling of gate length (l), drive current has been enhanced. However, presently the transistor gate length is below 20 nm. Therefore, soon enough the gate length reduction will stop. Next, by artificially straining the silicon substrate channel area[1-4], mobility has been enhanced modestly. Beginning of the new millennium intense focus has been given to increase the dielectric capacitance (C_{ox}) by using high permittivity (high-κ) materials which give a cushion to increase the dielectric constant while at the same time increasing the dielectric thickness to eventually achieve a higher dielectric capacitance[5,6]. And this necessitated an inevitable replacement of classical silicon oxide dielectric by high-κ dielectric such as hafnium, zirconium, aluminum oxide or such. Because of their sensitivity to thermal budget, poly silicon gate could not have been used[7-12]. This phenomenon introduced metal gate. With these changes semiconductor industries have adopted high-κ/metal gate stacks – according to Intel Co-founder Gordon Moore "the most remarkable change in industry's three decades". The demand of consumer electronics is increasing at such a high pace, which is not only about variety of the electronic gadgets rather their higher performance and lower cost too. As a consequence, after introduction of high-κ/metal gate stacks in 2008, in the last two years semiconductor industry has moved towards non-planar three-dimensional (3D) architecture devices known as multiple gate FETs (MugFETs), tri-gate FETs or FinFETs[13-16]. All these rapid changes show the increased complexity in device technology and relevant fabrication intricacy. While performance has driven a lot of these changes, introduction of multiple gate devices is directed towards better gate control to suppress short channel effects associated with continued gate length scaling. Short channel effects (SCE) cause higher drain induced barrier lowering, unwanted leakage and thus increased static power

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dissipation. While we aspire for more mobile technologies, none of our electronic gadgets, like tablets, can perform like laptops. This comes from compromised performance to retain longer battery lifetime, which is an inherent necessity for mobile electronics. As seen from the first empirical relationship, we cannot increase the width of the device as that will increase the static power (from third relationship), also it will consume more substrate real estate. It is to be noted that to reduce both the inverter delay and the static power, we need to use lower drive-in voltage (V_{dd}). However, that is correlated to gate voltage (V_g) – higher the drive-in voltage, higher the drive current. With all these complex relationships and convoluted dependencies, in modern electronics and as well as in future electronics several trends will have to follow:

- Gate length scaling until we reach physical gate length of 2 nm using Extreme Ultraviolet (EUV) technology which is still in the research and development phase and extremely expensive. It is to be noted that smaller devices not only ensures higher performance but also enables integration of more devices to increase multi-tasking capability. As an example today's smart phones are used not only for communication but also for browsing internet, video streaming and such.
- Maximizing available carriers in channel areas to take advantage of velocity saturation. This can be accomplished by thinning down the channel thickness as well as increasing electrostatic control by introducing more gates.
- Utilizing high-κ or higher-κ/metal gate stacks for leakage control and drive current enhancement. At the same time the new kind of dielectrics need to be scaled which requires ultra-thin but uniform, conformal and high quality nano-scale dielectric deposition. Semiconductor industry believes atomic layer deposition (ALD) is such system to provide necessary dielectrics. From the current trend it seems to be that higher temperature deposition (150 °C or above) is critical to achieve such high quality films.
- Innovative architecture such as FinFET or one-dimensional nanowire devices need to be used. In the recent past we have shown nanotube made up of conventional channel materials can provide both the high performance and ultra-low power operation with area efficiency[17-21]. In most of the occasions such non-planar architecture requires complicated fabrication process and integration.
- One last but not the least change we may expect is the change in channel material. It is highly anticipated that III-V materials such as InSb, InGaAs will be used for n-type MOSFETs while SiGe will be used for p-type MOSFETs[22-25]. Electron and hole mobility for these two material sets are higher than those of silicon. Discovery of two dimensional materials has surged in their research. Specially for graphene which promises higher mobility, however, being a semi-metallic film it's on and off distinction is barely minimum – hindering their potential usage as switching element. One specific point is growth or deposition of these materials is cost exhaustive. And thus one of the big pushes is to continue using silicon as host substrate and then to use other channel materials either grown, deposited or transferred on silicon platform. Therefore, the usage of silicon as cost effective and widely studied substrate will continue.

3. FLEXIBLE SILICON ELECTRONICS

All the above mentioned criteria indicate a complex future for semiconductor devices. However, the demand for higher performance, multi functionality, longer battery lifetime and lower cost is rising with growing world population. Recent advent of social media and online education has shown that the connectivity among Internet users is increasing, changing our socio-economic landscape. In the recent past, social media has been effectively used for political reforms as well as political contest (example: past two US Presidential Elections). Additionally, rise of usage in smart phones and tabs like iPad or various tabs and complementary expansion of wi-fi technology, appropriately marriages rise in social media usage. In near future we can predict to see better health care by creating universal health database, wide deployment of sensors for food, water, environment monitoring, more widely used electronic financial system and augmented reality.

Empowering world population with more data (information) at an affordable price will facilitate these opportunities and this can only happen by expansion of ultra-mobile computation which will leverage emergence of cloud computing. And this is where flexible and transparent electronics will play critical role. Because future gadgets will not only be of higher performance with multi functionality and longer battery lifetime, they must be smaller, light-weight and potentially flexible to be folded and/or worn. We may also expect even transparency as an additive criterion especially for wearable electronics. In the long run we may also expect stretchable, transient, transformable, convertible and recoverable features. But for now, we can understand that usage of silicon is inevitable for such electronics system. And as we know,

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silicon is a rigid inorganic material which is also brittle. Therefore, it is imperative to obtain flexible silicon or a process which will help obtaining flexible silicon. Many interesting attempts have been made towards that direction and before discussing them it is important to discuss briefly the status-quo of flexible electronics.

Since 1990 researchers have been working vigorously to find out the best possible electronic devices (which can match or out-perform silicon based electronics). They have been exploring usage of plastic as flexible substrate and organic chemistries as basis of organic and molecular electronics[26,27]. Although transparent plastic substrates provide interesting and cost-effective solutions, two fundamental issues prevent its full potential: (i) inherent low mobility makes it unsuitable for high performance computation applications and (ii) incompatibility with high thermal budget processes which have been leveraged for many modern silicon based diversified technologies. Even then, flexible thin film transistors, displays, photovoltaic, sensors, photodetectors are fabricated through wafer thinning technologies such as back-grinding and carrier techniques[28], or through physical transfer of thin semiconductor segments (as large as 450 μm x 45 μm or 200 μm x 7 cm) or membranes onto plastic substrates[29-31]. For example J. Rogers et. al. demonstrated the fabrication of thin and flexible nano-ribbons by using isotropic wet etch in a <111> Si or silicon-on-insulator (SOI) wafer then transferred onto a plastic substrate[32-35]. However, inherently transfer technology suffers from complexity with physical transferring of small silicon pieces and higher substrate cost. The price of a Si (111) wafer or a SOI wafer is higher than a Si (100) wafer. Finally, although optically transparent and mechanically flexible electronics can be useful tools for next generation see-through devices and technologies, existence of such silicon substrate is rare too[36]. Specially, cost effective process technology such as inkjet printing on plastics, drives the niche of this emerging technology for flexible RFID tags, sensors, displays and medical devices[37–45]. In addition to their low cost manufacturing, their relatively low voltage operation projects them as energy efficient and hence natural contender for portable device applications. In short, contrary to today's silicon based electronics whose key trend is scaling device dimension and thus transforming from micro to nanoelectronics, solution based processing on everyday materials like plastic originates the concept of macroelectronics[46]. Flexible displays, sensory electronics, e-textiles and active antennas are example of this division[34]. Rather than small device dimension, this kind of electronics depends on the overall size of the system. To move this technology to the next level of higher performance electronics comparable to silicon's main forte of computation, significant research is yet to be done. Unfortunately although chemically formed organic electronics have interesting properties, their semiconducting performance is yet to match that of poly-crystalline silicon[47–51]. Limited process temperature (≤150 °C), age defined reliability and controlled manufactuability of conventional organic electronics, are yet to be improved. To provide an alternate solution to make hybrid electronics like peeled silicon and other materials and their integration on plastic substrates has generated immense interest in the scientific community[52]. Extreme level integration has been demonstrated in this area by J. Rogers et. al. on various applications[33,53–55].

4. FLEXIBLE SILICON FABRIC BASED ELECTRONICS

Before comparing with various techniques used to obtain silicon based flexible electronics, we will discuss our generic batch fabrication process to obtain flexible silicon electronics. In our process (Figure 2) we use bulk mono-crystalline silicon (100) wafer which is the most widely used substrate in the industry because of its superior electrical behavior (electron mobility is higher in silicon (100) plane – in a digital circuit we use more n-type MOSFET than p-type MOSFET which runs on hole mobility) and low cost (compared to silicon (110), silicon (111) or silicon-on-insulator the price of silicon (100) is 50% or less). Next, we fabricate the devices as if it would have been done in a typical process flow for silicon electronics. However, we pay specific attention while designing the mask (to place the devices on the silicon substrate) that the inactive areas are 20 μm apart from each other and each inactive areas are at least 5 μm wide. After fabrication of devices (including multi-level interconnect, albeit very complex), we use a mask to pattern photoresist on the top layer and then use reactive ion etching to perform anisotropic etch through the respective materials and subsequently silicon substrate to form trench of 5 μm width. It is to be noted our calculation shows we only waste 16% of area in such way. However, this area loss is comparable to that of in a normal integrated circuit where shallow trench isolations or mesa isolations are used to ensure appropriate isolation among the devices. Moving forward, we deposit an insulating dielectric thin film (examples include but not limited to furnace oxidation based silicon oxide, plasma enhanced chemical vapor deposition based silicon oxide or atomic layer deposition based high-k dielectric) followed by directional etching to remove its horizontal portion while protecting the vertical portion. This way we form "*spacers*" to protect the trench wall. Next we use an isotropic etch process to etch off silicon vertically as well as laterally. In this way we create caves or scallops inside silicon substrate (leaving at least 25 μm thick silicon from top surface under the device areas). Our current process capability can ensure 10 μm lateral etch on each side resulting in 20

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µm lateral etch (cave or scallop maximum width). It is to be noted that this 20 µm x 20 µm area is where the devices are located. The throughput of such process is high enough (less than an hour). When two adjacent caves or scallops are meeting forming a continuous chain of vaguely attached top silicon fabric with devices and trenches and bottom remaining substrate. One bottle neck of our process is thickness limitation as scallops are of elliptical to circular shape which constitutes uneven silicon loss in the vertical direction. Excitingly we have overcome that issue which will be chronicled in near future. To peel off the top portion of silicon (fabric) we do not need external support or additional processes.

Finally after release we can perform chemical mechanical polishing (CMP) to planarize the bottom substrate and to reuse them. As it can be seen from our process description this is a generic batch process based on conventional micro-fabrication processes which increase mask count by one (one additional lithographic step), two thin film deposition processes and three reactive ion etch processes. Although this will increase the cost, in a CMOS foundry it is customary to use thousands of steps to fabricate ICs with multi-level interconnects. And hence the described processes will not increase the cost in an extravagant way compared to use highly expensive and low throughput epitaxial process. In addition, our study shows that we can obtain six layer of silicon fabric with devices by recycling a silicon substrate with original thickness of 0.5 mm. This also shows that 16% loss in each layer is recovered by 6 layers of silicon fabrics.

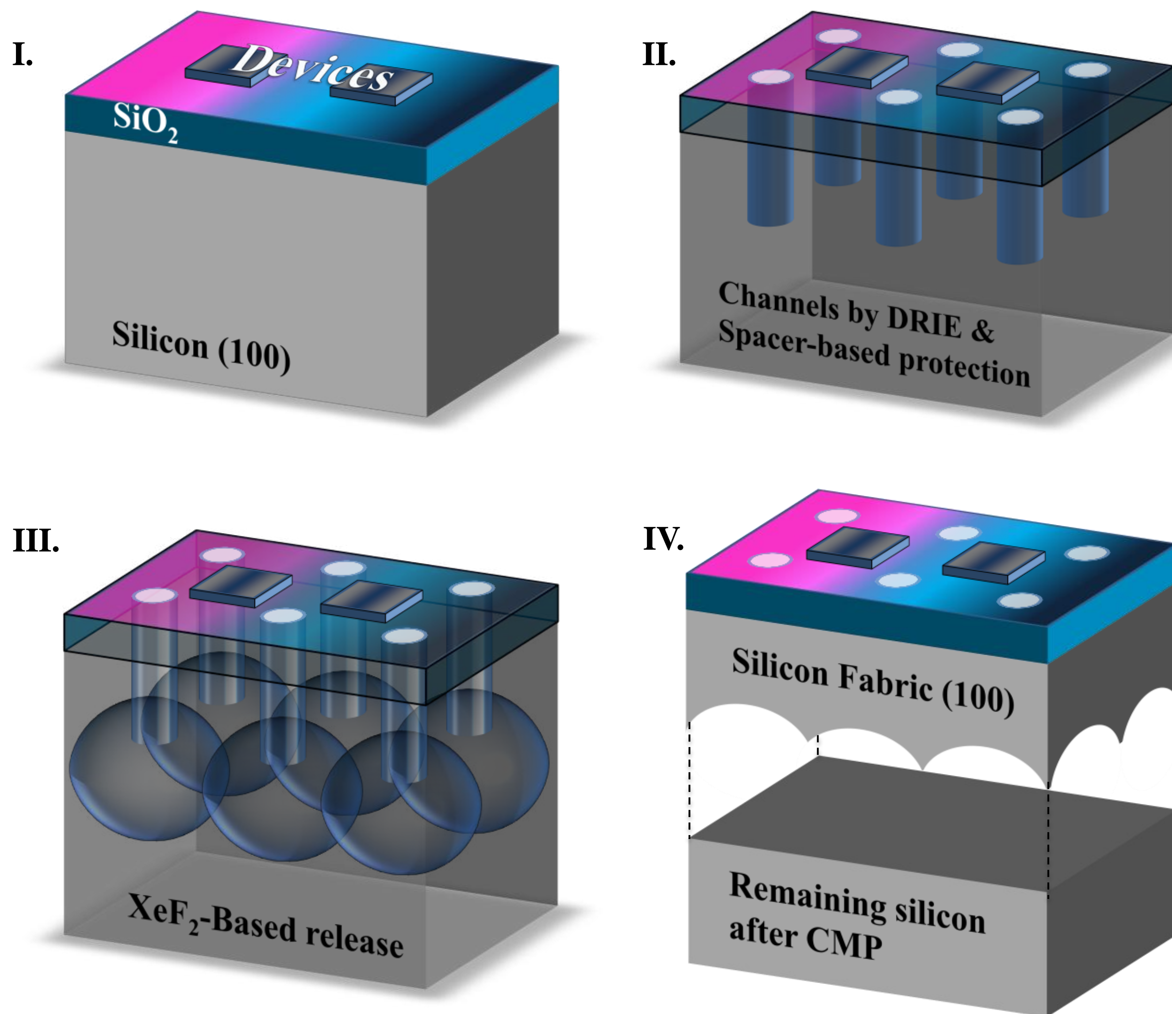

Figure 2. 3-D schematic of generic process flow to convert any silicon electronics into flexible and transparent silicon fabric based electronics.

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5. RESULTS AND DISCUSSION

A comparative analysis of various methods used to obtain flexible electronics is depicted in the following table:

Technique	Size	Thickness	Temp. stability	Flexibility	Speed	Device size	Apps.	Challenges
Solution based[27]	Whole wafer	<100 μm	150 °C	On plastic	Extremely slow	μm	Display RFID Sensors	Slow speed Low thermal budget
Back-grinding[28]	Whole wafer	<100 μm	1100 °C	Flexible	Good	nm	Photovoltaic	Cost related to wastage of whole substrate, produces roughness and causes damage to the substrate and devices
Carrier techniques [56, 57]	Whole wafer	12 μm	~400 °C	Flexible	Good	μm	Discrete devices, photovoltaic, opto-electronics	Cost related to wastage of whole substrate, bonding
Exfoliation [52]	Ultra small	<5 nm	Depends on substrate where it is transferred	Flexibility depends on substrate where it is transferred	Expected to be faster than silicon electronics	nm	Exploratory	Uncontrolled exfoliation
Controlled release from SOI [52]	Small	50 nm	Depends on substrate where it is transferred	Flexible	Good for discrete devices and TFT	μm	Display Discrete devices Sensors	Size, expensive substrate, lack of fully state-of-the-art silicon electronics compatible processing, transfer process
Controlled release from bulk substrate [52]	Small	~100 nm	Depends on substrate where it is transferred	Flexible	Good for TFT	μm	Display Discrete devices Sensors	Size, expensive substrate, lack of fully state-of-the-art silicon electronics compatible processing, transfer process
State-of-the-art silicon	Whole wafer	500 μm	1100 °C	N/A	3.2 GHz	nm	Computation Display Sensors	Not flexible, complex and costly

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electronics [58]								fabrication
Proposed Flex-Si (present status)	*18 cm^2*	*25 μm*	*1100 °C*	*Comparable to plastic*	*Should be same as state-of-the-art silicon electronics*	*nm*	*Electronics Photovoltaic Membrane*	*Area penalty*

Based on all the relevant works and their pros and cons it is confirmed that none of these techniques is comparable to existing state-of-the-art silicon electronics. Thus, our technique leverages the already existing silicon infrastructure without performance compromise but with some area penalty. For the first time it also uses bulk mono-crystalline Si (100) – the industry standard substrate for silicon electronics.

The closest work that has shown the most promising techniques in this area is by J. Rogers et. al. Their recent paper shows silicon electronics with thermal grade SiO_2 dielectrics extracted (removed from) specially prepared silicon-on-insulator (SOI) wafers[59]. In this technique, they built the individual devices including SiO_2 growth, source and drain formation to fabricate full transistor. Then the individual devices were transferred to an arbitrary substrate (here plastic). A final interconnection step yields functional systems. Although the electrical properties achieved on thin plastic substrates in this manner significantly exceed those of previous demonstrations, they still suffer from usage of expensive SOI wafers, larger device sizes (20 μm gate length) which result in less number of devices per unit area, absence of state-of-the-art high-κ/metal gate based silicon electronics processing and finally compromised device data (drive-in voltage of 4.1 volts, whereas today's transistor technology uses 1 volt or less). Drive-in voltage can increase the drive current – indicator of high performance or faster computation but it also increases the power consumption thus making the chip set unsustainable for longer battery lifetime – defeating the purpose of mobile applications.

As stated earlier, these works are extraordinary achievements towards a new paradigm than the conventional organic or molecular electronics integrated on flexible substrate[27]. However, the integration challenges such as making significantly large devices to transfer them in an efficient way on the plastic substrate, usage of basic silicon materials (like SiO_2 as dielectric) cannot be overruled by further improvement using these techniques. Finally, a basic cost comparison will show that a prime grade epi bulk silicon wafer is 35% less expensive than a monitor grade SOI wafer.

J. Rogers et. al. have also demonstrated that they can achieve ultra-small nanowires, ribbons from bulk silicon (111) wafer and transfer them on plastic substrate multiple times to fabricate thin film transistor (TFT) based display system[60]. The challenges remain with use of Si (111) which is not used for standard silicon electronics, inability to fabricate transistor for computation and transfer process.

In the past, S. Fonash et. al. has shown usage of sacrificial layer to fabricate high performance poly-Si TFT and subsequent large area transfer to plastic substrate[61]. Yet, metal oxide semiconductor field effect transistor (MOSFET) fabrication on bendable platform is not realized. Recently Z. Ma et. al. has shown high performance poly-Si TFT with pre-transfer doping, the challenges remain with devices sizes and full fabrication[29–35].

Lately exfoliation of exciting novel materials like graphene, MoS_2 have shown exceptional promise for many interesting applications[52]. But their growth and exfoliation both are uncontrolled and unreliable. Also, graphene is semi-metallic – does not show an on/off switching behavior.

Solution based or ink-jet printing based organic and molecular electronics lack in inherent mobility (slow speed) and yet to be demonstrated multi-level interconnect based integration for complex circuitry which is required to be competitive for next generation computation.

Back grinding and carrier transport – both these techniques can eventually transfer the fully fabricated wafer (with all the necessary silicon electronics) on a plastic substrate or such. However, they will consume the whole wafer making it less appealing for the objective of flexible substrate where one of the key salient points is cost reduction. Also, the release processes are aggressive which cause extensive damage to tiny devices.

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Although some recent process techniques have used nickel deposition based strain engineering to exfoliate silicon chips (with devices) and they show promising electrical results[62-67], they are cost exhaustive (using ultra-thin body SOI, high energy implantation), opaque, and they suffer from nickel removal process related damage. Ultra-thin flexible silicon wafers are expensive, have more defects than usual device grade wafers, because of their ultra-thin nature during high thermal budget they are strained and deformed, require extra-ordinary care even in the clean room environment to handle them. Therefore their usage is restricted to sensors applications. Another method uses pore formation followed by epitaxial growth which itself is cost prohibitive for wide deployment applications like flexible electronics[68]. It is to be noted that performance per cost is the best driving force behind rise of information age and we must have to be cost conscious. Finally although our process resembles the single-crystal reactive etching and metallization (SCREAM) technology they have clearly different application[69]. Also, there have been works to create channels using a similar approach to the one described here[70]. However, those works generated vertical channels and then channels inside the wafer using different methods and with the different purpose to improve the cooling of a chip.

Using our developed process we have so far fabricated: (i) high-κ/metal gate stack based metal-oxide-semiconductor capacitors with ultra-scaled effective oxide thickness (EOT) and reduced gate leakage; (ii) high-κ/metal gate stack based metal-insulator-metal capacitors (MIMCAPs) – building block of memory devices specially for dynamic random access memory (DRAM); (iii) high-κ/metal gate stack based MOSFETs; (iv) thermoelectric generators; (v) movable microelectromechanical systems (MEMS) based actuators; (vi) micro-fabricated lithium-ion-batteries (μLB) (Figure 3) [71-75]. We have successfully used the process on poly and amorphous silicon, silicon oxide and silicon germanium. We can safely say that our *trench-spacer-release* process is expanding its spectrum both from materials and applications perspective.

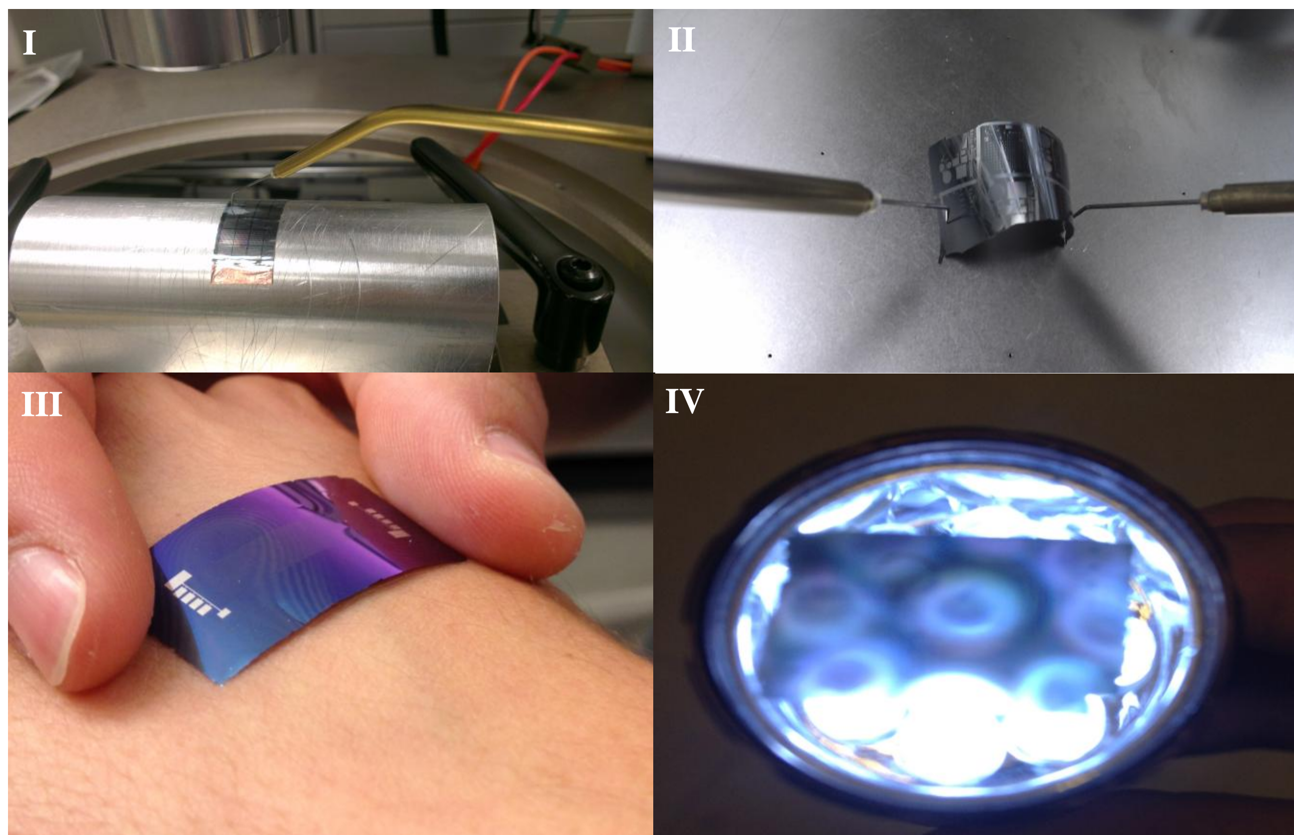

Figure 3. Digital images of various examples of flexible and transparent silicon fabric with devices like high-κ metal gate stack integrated devices and energy harvesting components such as thermoelectric generators.

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6. CONCLUSION

We envision to use silicon based flexible electronics for rapid deployment of ultra-mobile electronic gadgets. Reviewing the required trend for future generation devices, our process offers: (i) ultra-large-scale-integration capability; (ii) usability of advanced materials like high-κ/metal gate, salicidation technology; (iii) state-of-the-art CMOS process compatibility including high thermal budget processes; (iv) integration of vertically aligned complex non-planar 3D geometric devices such as nanowire FETs and/or Mug or FinFETs. Since we have successfully used our technique to demonstrate energy harvesting as well as storage and movable components we believe this technique will enable rapid rise of flexible inorganic electronics systems comprising of computation and communication gadgets with sensors, displays and power autonomy for ultra-mobile electronics.

References

1. M. M. Hussain, C. Smith, S. C. Song, B. H. Lee, R. Jammy, "Metal Gate Induced Strain Engineering for High-k/Metal Gate MOSFETs", ISAGST 2007, Dallas, Texas, USA

2. M. M. Hussain, K. Rader, C. Smith, C. Young, S. Suthram, C. Park, M. Cruz, P. D. Kirsch, R. Jammy, "Additive Process Induced Strain (APIS) Technology for 32nm High-k/Metal Gate MOSFETs", SSDM 2008, Ibaraki, Japan

3. S. Suthram, M. M. Hussain, H. R. Harris, C. Smith, H. –H. Tseng, R. Jammy, S. E. Thompson, "Comparison of Uniaxial Wafer Bending and Contact-Etch-Stop-Liner Stress Induced Performance Enhancement on Double-Gate FinFETs", IEEE Elect. Dev. Lett. 29, No.5 (2008)

4. C. Y. Kang, R. Choi, S. C. Song, K. Choi, B. S. Ju, M. M. Hussain, B. H. Lee1, G. Bersuker, C. Young, D. Heh, P. Kirsch, J. Barnet, J-W. Yang, W. Xiong, H-H Tseng, R. Jammy, "A Novel Electrode-Induced Strain Engineering for High Performance SOI FinFET utilizing Si (110) Channel for Both N and PMOSFETs", IEDM 2006, San Francisco, CA, USA

5. M. M. Hussain, M. Quevedo-Lopez, H. N. Alshareef, D. Larison, B. Gnade, M. El-Bouanani, "Thermal Annealing Effects on Physical Properties of a Representative High-k/Metal Film Stack", Semicond. Sci. Technol. 21, 1437-1440 (2006)

6. M. M. Hussain, S. C. Song, C. Y. Kang, M. Quevedo-Lopez, H. N. Alshareef, B. Sassman, R. Choi, B. H. Lee, "Compatibility of ALD HfSiON with Dual Metal Gate CMOS Integration Scheme", SSDM 2006, Japan

7. S. C. Song, M. M. Hussain, J. Barnett, B. S. Ju, B. H. Lee, "Advances and Challenges in Dual Work Function Metal Gate CMOS Integration", Solid State Technology, (Aug 2006) [Invited paper]

8. S. Song, M. Hussain, J. Barnett, C. S. Park, C. Park, P. Kirsch, B.H. Lee, and R. Jammy, "Integration Challenges and Opportunities for Nanometer Scale CMOSFET with Metal/High-k Gate Stack", ECS Trans. 11, (6) 315 (2007) [Invited paper]

9. Z. B. Zhang, S. C. Song, C. Huffman, J. Barnett, N. Moumen, H. Alshareef, P. Majhi, M. Hussain, M. S. Akbar, J. H. Sim, S. H. Bae, B. Sassman, and B. H. Lee, "Integration of Dual Metal Gate CMOS with TaSiN (NMOS) and Ru (PMOS) Gate Electrodes on HfO2 Gate Dielectric", VLSI 2005, Kyoto-Japan

10. S. C. Song, Z. Zhang, M. M. Hussain, C. Huffman, J. Barnett, S. H. Bae, H. J. Li, P. Majhi, C. S. Park, B. S. Ju, H. K. Park, C. Y. Kang, R. Choi, P. Zeitzoff, H. H. Tseng, B. H. Lee, R. Jammy, "Highly Manufacturable 45nm LSTP CMOSFETs Using Novel Dual High-k and Dual Metal Gate (DHDMG) CMOS Integration", VLSI 2006, Hawaii, USA [First three authors equally contributed to this paper]

11. M. M. Hussain, S. C. Song, J. Barnett, B. S. Ju, B. W. Sassman, B. H. Lee, "Realization of high-k/metal gate stack in dual metal gate CMOS: an integration perspective", ISAGST 2006¸ Austin, TX, USA

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12. C. S. Park, M. M. Hussain, J. Huang, C. Park, K. Tateiwa, C. Young, H. K. Park, M. Cruz, D. Gilmer, K. Rader, J. Price, P. Lysaght, D. Heh, G. Bersuker, P. D. Kirsch, H. -H. Tseng, and R. Jammy, "A Scalable and Highly Manufacturable Single Metal Gate/High-k CMOS Integration for Sub-32nm Technology for LSTP Applications", VLSI 2009, Kyoto, Japan [First two authors equally contributed to this paper]

13. M. Hussain, C. Smith, R. Harris, C. Young, B. Sassman, H. Tseng and R. Jammy, Gate-First Integration of Tunable Work Function Metal Gates of Different Thicknesses Into High-k/Metal Gates CMOS FinFETs for Multi-V_{Th} Engineering, *IEEE Transactions of Electron Devices* **2010**, 57, 626. [doi:10.1109/TED.2009.2039097]

14. R. Harris, M. M. Hussain, C. Smith, J. -W. Yang, P. Majhi, H. Adhikari, H. -H. Tseng, R. Jammy, "FinFETs: Challenges in Material and Processing for a New 3D Device Paradigm", Future Fab Intl. Volume 23, July 09, (2007) [Invited paper]

15. R. Harris, M. Hussain, C. Smith, J-W. Yang, J. Barnett, B. Sassman, S. Song, B.H. Lee, H. –H. Tseng, and R. Jammy, "Critical Components of FinFet Integration: Examining the Density Trade-off and Process Integration for FinFET Implementation", ECS Trans. 11, (6) 331 (2007) [Invited paper]

16. M. M Hussain, G. Gebara, J. Yang, P. Kalra, J. Price, B. Sassman, K. Matthews, H. R. Harris, H. H. Tseng, R. Jammy, "Highly manufacturable novel process for achieving vertical and smooth fins in sub-40 nm FinFET applied to high-K/metal gate stack", ESSDERC 2007, Munich, Germany

17. Muhammad M. Hussain, Hossain M. Fahad, Ramy Qaisi, "Contact Engineering for Nano-scale CMOS", physica status solidi (a), http://dx.doi.org/10.1002/pssa.201200343. [Invited paper]

18. Hossain M. Fahad, Muhammad M. Hussain, "Are nanotube architectures advantageous than nanowire architectures for field effect transistor applications?", Scientific Reports (Nature Publishing Group), doi:10.1038/srep00475.

19. H. M. Fahad, C.E. Smith, J. P. Rojas, M. M. Hussain, "Silicon Nanotube Field Effect Transistor with Core-Shell Gate Stacks for Enhanced High Performance Operation and Area Scaling Benefits", Nano Lett., 2011, 11 (10), pp 4393–4399

20. Hossain Fahad, Muhammad Hussain, "Vertically Aligned Epitaxial Silicon Nanowires and Tubes", MRS Fall Meeting 2012, Boston, Massachusetts, USA.

21. H. M. Fahad, M. M. Hussain, "High Performance Silicon Nanotube Tunneling FET for Ultra-Low Power Logic Applications", IEEE Trans. Elect. Dev. [DOI 10.1109/TED.2013.2243151]

22. H. Rusty Harris, Pankal Kalra, Pashant Majhi, Muhammad Hussain, David Kelly, Jungwoo Oh, Dawei He, Joel Barnett, Paul Kirsch, Gabriel Gebara, Jess Jur, Daniel Lichtenwalner, T.P. Ma, Scott Thompson, Byoung Hun Lee, Hsing-Huang Tseng and Raj Jammy, "Band-Engineered Low PMOS V_T with High-K/Metal Gate Including High Performance Dual Channel CMOS Integration", VLSI 2007, Kyoto, Japan

23. C. S. Park, M. M. Hussain, K. Tateiwaa, J. Huang, J. Linb, T. Ngai, S. Lian, K. Rader, B. Taylor, P. Kirsch, R. Jammy, "Alternative Approaches for High-k/Metal Gate CMOS: Low Temperature Process (Gate Last) and SiGe Channel", VLSI-TSA 2010, Taiwan [First two authors equally contributed to this paper]

24. M. M. Hussain, H. Fahad, J. Rojas, M. Hasan, A. Talukdar, J. Oommen and J. Mink, "Self-powered integrated systems-on-chip (energy chip)", Proc. SPIE 7679, 767914 (2010); doi:10.1117/12.850811 [Invited]

25. M. M. Hussain, C. S. Park, K. Tateiwa, C. Y. Kang, K. Rader, J. Huang, M. Cruz, P. Majhi, P. Kirsch, R. Jammy, "Integration of SiGe Channel PMOS and Si NMOS into Dual Channel High-k/Metal Gate CMOS for Low Standby Power Logic Applications", 5th International conference on SiGe Technology and Device (ISTDM) 2010, Stockholm, Sweden

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26. C. C. Striemer, T. R. Gaborski, J. L. McGrath, P. M. Fauchet, Charge- and size-based separation of macromolecules using ultrathin silicon membranes, *Nature* **2007**, 445, 749. [doi:10.1038/nature05532]

27. J. Sun, B. Zhang, H. E. Katz, Materials for Printable, Transparent, and Low-Voltage Transistors, Advanced Functional Materials, 2011, 21 (1), 29. [doi:10.1002/adfm.201001530]

28. J. Burghartz, Ultra-thin Chip Technology and Applications, Springer, Germany **2000**, Ed. 1

29. H. Yuan, J. Shin, G. Qin, L. Sun, P. Bhattacharya, M. G. Lagally, G. K. Celler, Z. Ma, Flexible photodetectors on plastic substrates by use of printing transferred single-crystal germanium membranes, *Applied Physics Letters* **2009**, 94, 013102. [doi:10.1063/1.3062938]

30. G. Qin, H. Yuan, H. Yang, W. Zhou, Z. Ma, High-performance flexible thin-film transistors fabricated using print-transferrable polycrystalline silicon membranes on a plastic substrate, *Semiconductor Science and Technology* **2011**, 26 025005 [doi:10.1088/0268-1242/26/2/025005]

31. L. Sun, G. Qin, J. Seo, G. K. Celler, W. Zhou, Z. Ma, 12-GHz Thin-Film Transistors on Transferrable Silicon Nanomembranes for High-Performance Flexible Electronics, *Small* **2010**, 6(22), 2473. [doi:10.1002/smll.201090076]

32. S. Mack, M. A. Meitl, A. J. Baca, Z.-T. Zhu, J. A. Rogers, Mechanically flexible thin-film transistors that use ultrathin ribbons of silicon derived from bulk wafers, *Applied Physics Letters* **2006**, 88, 213101. [doi:10.1063/1.2206688]

33. J. Yoon, A. J. Baca, S. Park, P. Elvikis, J. B. Geddes, III, L. Li, R. H. Kim, J. Xiao, S. Wang, T. Kim, M. J. Motala, B. Y. Ahn, E. B. Duoss, J. A. Lewis, R. G. Nuzzo, P. M. Ferreira, Y. Huang, A. Rockett, J. A. Rogers, Ultrathin silicon solar microcells for semitransparent, mechanically flexible and microconcentrator module designs, *Nature Materials* **2008**, 7, 907. [doi:10.1038/nmat2287]

34. A. Baca, J.-H. Ahn, Y. Sun, M. Meitl, E. Menard, H.-S. Kim, W. Choi, D.-H. Kim, Y. Huang, J. Rogers, Semiconductor Wires and Ribbons for High- Performance Flexible Electronics, *Angewandte Chemie International Edition* **2008**, 47, 5524. [doi:10.1002/anie.200703238]

35. M. M. Roberts, L. J. Klein, D. E. Savage, K. A. Slinker, M. Friesen, G. Celler, M. A. Eriksson, M. G. Lagally, Elastically relaxed free-standing strained-silicon nanomembranes, *Nature Materiasl* **2006**, 5, 388. [doi:10.1038/nmat1606]

36. S. Ju, A. Facchetti, Y. Xuan, J. Liu, F. Ishikawa, P. Ye, C. Zhou, T. J. Marks, D. B. Janes, Fabrication of fully transparent nanowire transistors for transparent and flexible electronics, *Nature Nanotechnology* **2007,** 2, 378. [doi:10.1038/nnano.2007.151]

37. J. A. Rogers, Z. Bao, K. Baldwin, A. Dodabalapur, B. Crone, V. R. Raju, V. Kuck, H. Katz, K. Amundson, J. Ewing, P. Drzaic, Paper-like electronic displays: Large-area rubber-stamped plastic sheets of electronics and microencapsulated electrophoretic inks, *Proceedings of National Academy of Sciences USA* **2001**, 98, 4835. [doi:10.1073/pnas.091588098]

38. H. Sirringhaus, T. Kawase, R. H. Friend, High-Resolution Ink-Jet Printing of All-Polymer Transistor Circuits, *MRS Bulletin* **2001**, 26, 539. [doi:10.1557/mrs2001.127]

39. G. H. Gelinck, H. E. A. Huitema, E. Van Veenendaal, E. Cantatore, L. Schrijnemakers, J. Van Der Putten, T. C. T. Geuns, M. Beenhakkers,J. B. Giesbers, B. H. Huisman, E. J. Meijer, E. M. Benito, F. J. Touwslager, A. W. Marsman, B. J. E. Van Rens, D. M. De Leeuw, Flexible active-matrix displays and shift registers based on solution-processed organic transistors, *Nature Materials* **2004**, 3, 106. [doi:10.1038/nmat1061]

40. L. S. Zhou, A. Wanga, S. C. Wu, J. Sun, S. Park, T. N. Jackson, All-organic active matrix flexible display, *Applied Physics Letters* **2006**, 88, 3. [doi:10.1063/1.2178213]

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41. S. Lee, B. Koo, J. G. Park, H. Moon, J. Hahn, J. M. Kim, Development of High-Performance Organic Thin-Film Transistors for Large-Area Displays, *MRS Bulletin* **2006**, 31, 455. [DOI: 10.1557/mrs2006.118]

42. S. E. Burns, K. Reynolds, W. Reeves, M. Banach, T. Brown, K. Chalmers, N. Cousins, M. Etchells, C. Hayton, K. Jacobs, A. Menon, S. Siddique, P. Too, C. Ramsdale, J. Watts, P. Cain, T. von Werne, J. Mills, C. Curling, H. Sirringhaus, K. Amundson, M. D. McCreary, A scalable manufacturing process for flexible active-matrix e-paper displays, *J. Soc. Information Display* **2005**, 13, 583. [doi:10.1889/1.2012644]

43. T. W. Kelley, P. F. Baude, C. Gerlach, D. E. Ender, D. Muyres, M. A. Haase, D. E. Vogel, S. D. Theiss, Recent Progress in Organic Electronics: Materials, Devices, and Processes, *Chemistry Materials* **2004**, 16,4413. [doi: 10.1021/cm049614j]

44. R. Parashkov, E. Becker, T. Riedl, H. H. Johannes, W. Kowalsky, Large Area Electronics Using Printing Methods, *Proceedings of IEEE* **2005** ,93, 1321. [doi:10.1109/JPROC.2005.850304]

45. T. Someya, Y. Kato, T. Sekitani, S. Iba, Y. Noguchi, Y. Murase, H. Kawaguchi, T. Sakurai, Conformable, flexible, large-area networks of pressure and thermal sensors with organic transistor active matrixes, *Proceedings of National Academy of Sciences, USA* **2005**, *102*, 12321. [doi:10.1073/pnas.0502392102]

46. Y. Sun, J. Rogers, Inorganic Semiconductors for Flexible Electronics, *Advanced Materials* **2007**, 19, 1897. [doi:10.1002/adma.200602223]

47. V. C. Sundar, J. Zaumseil, V. Podzorov, E. Menard, R. L. Willett, T. Someya, M. E. Gershenson, J. A. Rogers, Elastomeric Transistor Stamps: Reversible Probing of Charge Transport in Organic Crystals, *Science* **2004**, *303*, 1644. [doi:10.1126/science.1094196]

48. A. L. Briseno, R. J. Tseng, M.-M. Ling, E. H. L. Falcao, Y. Yang, F. Wudl, Z. Bao, High-Performance Organic Single-Crystal Transistors on Flexible Substrates, *Advanced Materials* **2006**, 18, 2320. [doi: 10.1002/adma.200600634]

49. R. Zeis, T. Siegrist, Ch. Kloc, Single-crystal field-effect transistors based on copper phthalocyanine, *Applied Physics Letters* **2005**, 86, 022 103. [doi:10.1063/1.1849438]

50. R. W. I. de Boer, M. E. Gershenson, A. F. Morpurgo, V. Podzorov, *Physica Status Solidi A* **2004**, *201*, 1302. [doi:10.1002/pssa.200404336]

51. I. N. Hulea, S. Russo, A. Molinari, A. F. Morpurgo, Reproducible low contact resistance in rubrene single-crystal field-effect transistors with nickel electrodes, *Applied Physics Letters* **2006**, 88, 113512. [doi:10.1063/1.2185632]

52. J. A. Rogers, M. G. Lagally, R. G. Nuzzo, Synthesis, assembly and applications of semiconductor nanomembranes, *Nature* **2011**, 477, 45. [doi:10.1038/nature10381]

53. D.-H. Kim, N. Lu, R. Ma, Y.-S. Kim, R.-H. Kim, S. Wang, J. Wu, S. M. Won, H. Tao, A. Islam, K. J. Yu, T. Kim, R. Chowdhury, M. Ying, L. Xu, M. Li, H.-J. Chung, H. Keum, M. McCormick, P. Liu, Y.-W. Zhang, F. G. Omenetto, Y. Huang, T. Coleman, J. A. Rogers, Epidermal Electronics, *Science* **2011**, 333 (6044), 838. [doi:10.1126/science.1206157]

54. R. Kim, D. Kim, J. Xiao, B. H. Kim, S. Park, B. Panilaitis, R. Ghaffari, J. Yao, M. Li, Z. Liu, V. Malyarchuk, D. G. Kim, A. Le, R. G. Nuzzo, D. L. Kaplan, F. G. Omenetto, Y. Huang, Z. Kang, J. A. Rogers, Waterproof AlInGaP optoelectronics on stretchable substrates with applications in biomedicine and robotics, *Nature Materials* **2010**, 9, 929. [doi:10.1038/nmat2879]

55. J. Yoon, S. Jo, I. S. Chun, I. Jung, H.-S. Kim, M. Meitl, E. Menard, Xiuling Li, J. J. Coleman, U. Paik, J. A. Rogers, GaAs photovoltaics and optoelectronics using releasable multilayer epitaxial assemblies, *Nature* **2010**, 465, 329. [doi:10.1038/nature09054]

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56. C. Landesberger, S. Scherbaum, K. Bock, Carrier techniques for thin wafer processing, CS MANTECH Conference, May 14-17, 2007, Austin, Texas, USA

57. T. Loher, M. Seckel, B. Pahl, L. Bottcher, A. Ostmann, H. Reichl, Highly integrated flexible electronic circuits and modules, 3rd International Microsystems, Packaging, Assembly & Circuits Technology Conference **2008**, 86. [doi: 10.1109/IMPACT.2008.4783814]

58. M. Bohr, The Evolution of Scaling from Homogeneous Era to the Heterogeneous Era, IEEE Int. Electron Device Meeting **2011**, 1.1, 1-6.

59. H.-J.Chung, T.-i. Kim, H.-S. Kim, S. A. Wells, S. Jo, N. Ahmed, Y. H. Jung, S. M. Won, C. A. Bower, J. A. Rogers, Fabrication of Releasable Single-Crystal Silicon–Metal Oxide Field-Effect Devices and Their Deterministic Assembly on Foreign Substrates. *Advanced Functional Materials* **2011**, 21, 3029, [doi:10.1002/adfm.201100124]

60. A. Baca, M. Meitl, H. Ko, S. Mack, H.-S. Kim, J. Dong, P. Ferreira, J. Rogers, Printable Single-Crystal Silicon Micro/Nanoscale Ribbons, Platelets and Bars Generated from Bulk Wafers, *Advanced Functional Materials* **2007**, 17, 3051. [doi:10.1002/adfm.200601161]

61. Y. Lee, H. Li, S. J. Fonash, High-performance poly-Si TFTs on plastic substrates using a nano-structured separation layer approach, *IEEE Electron Device Letters* **2003**, 24(1), 19. [doi:10.1109/LED.2002.807021]

62. Y. Zhai, L. Mathew, R. Rao, D. Xu, S. K. Banerjee, “High-Performance Flexible Thin-Film Transistors Exfoliated from Bulk Wafer”, Nano Lett., vol. 12, no. 11, pp. 5609–5615, Oct. 2012

63. L. Mathew, D. Jawarani, “Method of forming an electronic device using a separation technique,” U.S. Patent 8,076,215, December 13, 2011.

64. L. Mathew, D. Jawarani, “Method of forming an electronic device using a separation-enhancing species,” U.S. Patent 7,749,884, July 6, 2010.

65. D. Shahrjerdi, S. W. Bedell, A. Khakifirooz, K. Fogel, P. Lauro, K. Cheng, J. A. Ott, M. Gaynes, D. K. Sadana, “Advanced Flexible CMOS Integrated Circuits on Plastic Enabled by Controlled Spalling Technology”, in Proc. IEEE International Electron Devices Meeting (IEDM), San Francisco, 2012, pp. 5.1.1-5.1.4.

66. D. Shahrjerdi, S. W. Bedell, “Extremely flexible nanoscale ultrathin body silicon integrated circuits on plastic”, Nano Lett., dx.doi.org/10.1021/nl304310x

67. K.-S. Chen, X. Zhang, S.-Y. Lin, “Intrinsic stress generation and relaxation of plasma-enhanced chemical vapor deposited oxide during deposition and subsequent thermal cycling”, Thin Solid Films, vol. 434, pp. 190–202, Feb. 2003.

68. J. N. Burghartz, W. Appel, H. D. Rempp, M. Zimmermann, “A New Fabrication and Assembly Process for Ultrathin Chips”, IEEE Trans. Electron Dev., vol. 56, no. 2, pp. 321-327, Feb. 2009.

69. K. A. Shaw, Z. Zhang, N. C. MacDonald, SCREAM I: A single mask, single-crystal silicon, reactive ion etching process for microelectromechanical structures, *Sensors and Actuators A: Physical* **1994**, 40(1), 63. [doi:10.1016/0924-4247(94)85031-3]

70. M. J. de Boer, R. Willem Tjerkstra, J. W. (Erwin) Berenschot, H. V. Jansen, G. J. Burger, J. G. E. (Han) Gardeniers, M. Elwenspoek, A. van den Berg, Micromachining of buried micro channels in silicon, Journal of Microelectromechanical Systems 2000, 9(1), 94. [doi:10.1109/84.825783]

71. J. P. Rojas, A. Syed, M. M. Hussain, “Mechanically Flexible, Optically Transparent Porous Mono-crystalline Silicon Substrate”, IEEE 25th International Conference on Micro Electro Mechanical Systems (MEMS), 2012, Paris, France, Publication Year: 2012 , Page(s): 281 - 284

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72. Jhonathan P. Rojas, Muhammad M. Hussain, "Flexible Semi-transparent Silicon (100) Fabric with High-κ/Metal Gate Devices", Phys. Status Solidi RRL, 7, No. 3 (2013) [DOI 10.1002/pssr.201206490 (2013)] [Cover Page]

73. H. M. Fahad, M. M. Hussain, "High Performance Silicon Nanotube Tunneling FET for Ultra-Low Power Logic Applications", IEEE Trans. Elect. Dev. [DOI 10.1109/TED.2013.2243151]

74. Jhonathan P. Rojas, Galo Torres Sevilla, Muhammad M. Hussain, "Structural and Electrical Characteristics of High-k/Metal Gate MOSCAPs Fabricated on Flexible, Semi-transparent Silicon (100) Fabric", Appl. Phys. Lett. 102, 064102 (2013).

75. G. T. Sevilla, J. P. Rojas, S. Ahmed, A. Hussain, S. B. Inayat and M. M. Hussain, "Silicon Fabric for Multi-Functional Applications", Transducers 2013 & Eurosensors XXVII: The 17th International Conference on Solid-State Sensors, Actuators and Microsystems, Barcelona, Spain, 16th to 20th Jun 2013.

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