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Mechanism of Current Collapse Removal in Field-Plated Nitride HFETs

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***Abstract*—An experimental study of the mechanism of RF current collapse removal in high-power nitride-based HFETs is presented. The results show that the conductivity of the dielectric material under the field plate plays a crucial role in the current collapse removal. Identical geometry field plated HFETs differing only in the FP dielectric conductivity show varying degree of current collapse removal. Devices with semiconducting dielectric layers exhibit perfectly linear RF power – drain bias dependence with the output powers of 20 W/mm at 55 V drain bias with essentially no current collapse. A trapped charge discharging model is presented to explain the removal of current collapse in FPd devices.**

***Index Terms*—Current collapse, field-plate (FP), GaN-AlGaN, high-electron mobility transistors (HEMT), high field-effect transistors (HFET), metal–oxide–semiconductor heterojunction field-effect transistor MOSHFET, microwave power.**

I. Introduction

SINCE their first demonstration in 1991 [1] GaN-AlGaN heterostructure field-effect transistors (HFETs) have been extensively explored for solid-state high-power microwave devices. However, until recently, the experimentally demonstrated microwave powers were well below the values expected from their dc parameters. The output RF powers were found to be severely affected by the large signal RF dispersion, also referred to as current collapse. Recently, using a field-plated (FP) device design Ando *et al.* [2] demonstrated microwave powers of 10 W/mm at 2 GHz (gate-length 1 μm, source/drain opening 4.5 μm, and $V_{\rm ds} = 65$ V). Similar FP HFET devices were later reported by Thompson *et al.* [3] (16.5 W/mm at $V_{\rm ds} = 60$ V) and Wu *et al.* [4] (12.4 W/mm at 48 V and 30 W/mm at $V_{\rm ds} = 120$ V). The increased output powers for the FP HFETs in [2]–[4], were attributed to the higher breakdown voltage and reduced trapping due to the lower gate peak fields as suggested in [4]. However, to date no studies on the effect of FP dielectric material on the device performance have been reported. In this paper, we present the results of an experimental study showing that the leakage current through the FP dielectric plays a significant role in the current collapse removal. HFET devices with the "leaky" dielectric under the FP yielded output powers of ≈ 20 W/mm at 55-V drain bias. To the best of our knowledge, these are the highest reported power densities for this bias level.

II. Device Design and Fabrication

The device epilayer structures for this letter were grown by low-pressure metal–organic chemical vapor deposition on insulating 4H-SiC substrates. All AlGaN/GaN layers of the structures were deposited at 1000 °C and 76 torr. A 50-nm AlN buffer layer was first grown at a temperature of 1000 °C, followed by a 1.5 μm insulating GaN layer. The heterostructure was capped with a 25-nm $Al_{0.25}$ $Ga_{0.75}N$ barrier layer, δ-doped with silicon. The 2-D gas sheet resistance as measured by an on-wafer RF probing system was $\sim 310\,\Omega$ sq.

HFET devices were fabricated using standard optical lithography techniques. First a mesa structure was formed by using chlorine and an inductively coupled plasma (ICP). The ohmic contacts were then fabricated using Ti/Al/Ti/Afu. They were annealed in a forming gas ambient. Subsequent to that 1.1 $\times$200 μm Ni (100 Å)/Au (1000 Å) gates were fabricated. The source/drain spacing was 8 μm. The HFET devices from the same wafer were then used to process four different device types for our letter. For the first type, a 1000 Å thick silicon-oxynitride layer was deposited over the gate and the access region using a plasma-enhanced chemical vapor deposition (PECVD) process optimized to yield a highly insulating dielectric layer. These devices will be referred to as device type 1. For the second device type, the PECVD conditions were adjusted to yield a dielectric, whose isolation was significantly lower than that for the dielectric 1. The thickness for the dielectric 2 was kept identical to that for dielectric 1 (1000 A). The dielectric permittivity of dielectric 2 as confirmed by C–V measurements at 1 MHz and S-parameter testing in the 1 – 10 GHz range was also nearly the same as that for dielectric 1. These devices will be referred to as device type 2. For some of the devices of the type 1 and 2, 2.1-μm-long field-plates (FP) overlapping the gate with an overhang of 1 μm in the gate-drain opening were deposited on top of the dielectric. The gate and the field plates were connected at the gate-pad region. These field plated devices will be referred to as device type 1FP and 2FP respectively. These four device types 1, 2, 1FP, and 2FP formed the basis for the letter reported here.

III. Device Performance and Discussion

The fabricated HFETs exhibited peak currents of about 1.2 A/mm at zero gate bias, a threshold voltage of around -4.5 V and their gate-leakage current at $V_g = -4$ V was ~ 1 μA. The large signal RF powers were measured at 2 GHz using Maury automated tuning system. For device type 1 (highly insulating dielectric without FP), the maximum RF output powers quickly saturated as a function of the drain bias. The RF power/drain voltage plot for a representative Type 1 device is shown in Fig. 1 by open circle symbols. The maximum RF power was limited by a severe current collapse. The RF powers for FP devices with the dielectric 1 (devices type 1FP) are shown in Fig. 1 by open triangles. As seen, the deposition of the FP on top of the dielec-

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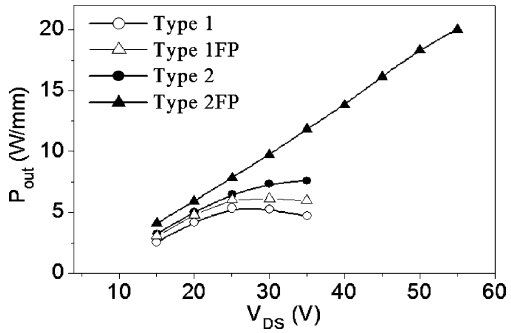

Fig. 1. RF power – drain bias dependencies for devices capped with different dielectric (highly insulating – type 1, and semiconducting -type 2, with and without FPs. Star symbols show the highest reported powers for different FP devices.

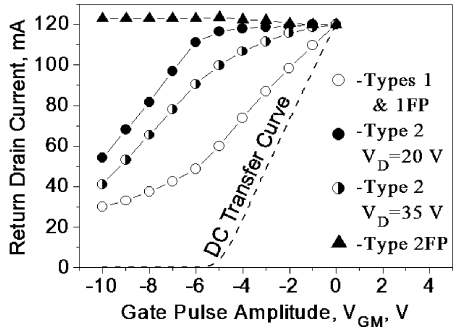

Fig. 2. Pulsed return current dependencies for different devices used in this letter. The device width is 100 mm. A decrease in return current as compared to the dc value at zero gate bias (120 mA for our devices) is indicative of the current collapse.

tric layer 1 has no significant effect on the RF powers, which remain relatively low.

For device type 2 ("semiconducting" dielectric 2), the output RF powers are slightly higher (as compared to device type 1 or 1 FP) and they also saturate at a higher drain bias. The corresponding RF power – drain bias dependence is shown in Fig. 1 by solid circles. The observed reduction in current collapse is due to the "surface passivation" [5], [6] from dielectric 2. Note that the dielectric type 1 does not provide the same effect although its' dielectric permittivity and composition are very close to those of the dielectric 2. For FP device type 2FP the RF output powers increase linearly with the drain bias reaching 20 W/mm at 55 V. The powers closely correspond to those expected from the dc characteristics. This behavior clearly indicates an absence of the RF-current collapse.

According to simulations, the deposition of FP reduces the peak fields at the gate edges by a factor of two or less depending on the FP design [7]–[9]. Since the FP definitely reduces the peak-fields in device type 1FP as compared to the same devices without FP, we can conclude that the peak field reduction does not lower the current collapse. The same conclusion follows from comparison of the RF performance of devices 2 and 2FP. The RF powers for HFET type 2 saturate at the drain biases of 25 V. Since the FP deposition reduces the gate peak fields twice at the most, one might expect the same RF power saturation in devices 2FP to occur at 50 V, as this voltage would reproduce the same peak fields in the FP devices. However, this does not seem to be the case for the type 2FP FP device. This further supports our assertion that field plates remove current collapse but not due to the reduction of peak fields. In order to rule out the contribution of possible surface modifications in the AlGaN/GaN heterostructures due to different dielectric deposition regimes, we also fabricated and tested the structures having a thin layer of dielectric type "1" sandwiched between the FP and the leaky dielectric type "2" (which was deposited directly on the AlGaN surface). The performance of this test device was nearly the same as that of the device type 1FP. Fig. 1 also shows that the RF powers for FP devices using dielectric type 1 are lower compared to those reported recently by other groups. However, for FP with the "semiconducting" dielectric (type 2), the RF powers achieved in this study to the best of our knowledge significantly exceed all the reported results at the corresponding drain biases.

To further investigate the current collapse removal mechanism in the devices of our study, their pulsed current–voltage (*C–V*) characteristics using a "return current" technique proposed earlier in [10] and [11] were also measured. For these measurements, the drain bias was kept constant, while the gate voltage was pulsed from a negative value $V_{\rm GM}$ up to zero volts. The current measured immediately after the gate voltage returns to zero is referred to as the "return current". In devices without the current collapse, the return current for any value of $V_{\rm GM}$ is equal to the steady state dc current at zero gate bias $I_{\rm DC0}$. The deviation of the "return-current" from $I_{\rm DC0}$ is a measure of the degree of current collapse. The return current dependencies on the gate pulse amplitude ($V_{\rm GM}$) for the devices used in this study are shown in Fig. 2. For devices type 1 and 1FP, a strong dispersion was observed. For devices of the type 2 (without FP), there was no current collapse at 20-V drain bias, however, at a higher drain bias of $V_D = 35$ V the collapse was significant. Field-plated devices type 2FP do not show any collapse at any drain bias. To summarize, the highly insulating dielectric (type 1) does not remove the current collapse. The "semiconducting" dielectric (type 2) without the field plate removes the collapse at relatively low but not at the higher drain biases. The "semiconducting" dielectric capped with the FP completely removes the current collapse for all drain biases used in this letter.

In the past, it has been reported that the deposition of FP on top of "semiconducting" dielectric significantly improves the performance of high-power Si devices by providing a leakage path that effectively discharges the surface state charges [12], [13]. The observed drastic difference in the performance of the HFET devices with dielectrics type 1 and 2 can be attributed to the following trapped charge discharging mechanism which is somewhat similar to that observed in Si devices. Under high bias and large-signal RF drive, surface and/or buffer trapped charges accumulate mostly in the gate-drain high-field region. Accumulated trapped charges prevent complete recovery of the 2-D gas density at zero or positive gate voltages thus causing the RF current collapse. Semiconducting dielectric provides a path to discharge the trapped charge. The high-field region width $X_{\rm D}$, at a high drain bias $V_{\rm D}$ can be estimated as [14]

$$X_{\rm D} = \frac{2\varepsilon\varepsilon_0 V_{\rm D}}{qN_S} \tag{1}$$

where N_S is the sheet electron density in the 2-D channel. Under large input drive, the peak drain voltage, $V_{\rm DM} \approx 2 \times V_B$, where V_B is a quiescent bias point (for the large drain bias, we ignore the contribution of knee voltage). Thus, $X_{\rm D}$ is a linear function of the peak drain voltage $V_{\rm DM}$. For typical values of $N_S \approx 10^{13}$ cm^{-2},

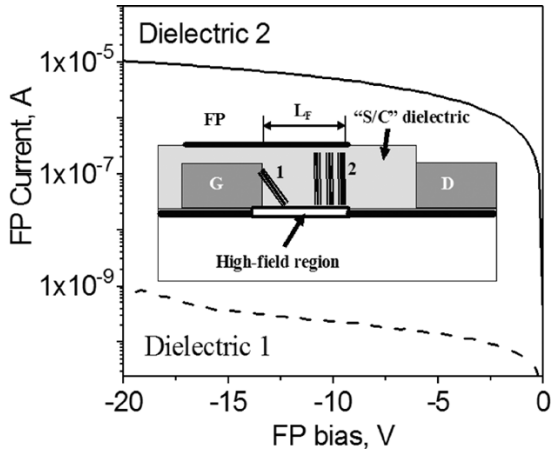

Fig. 3. I–V characteristics if the FP with different dielectrics. Inset: 1) Discharge path for passivated devices without FP. 2) Additional discharge path for devices with FP. Effective at high drain bias provided that $L_F \approx X_D$.

we find $X_{\rm D} \approx 0.5\,\mu$m for $V_{\rm DM} = 50$ V (~ 25 V drain bias) and $X_{\rm DM} \approx 1\,\mu$m for $V_{\rm DM} = 100$ V (~ 50 V drain bias).

The trapped surface charge concentration $N_{\rm TS}$ is a fraction of the 2-D electron sheet density,N_S: $N_{\rm TS} = \alpha N_S$, where α is the trapping factor [15]. Total trapped charge is $Q_T = q \times N_{\rm TS} \times X_D \times W$, where W is the device width. Using (1), the trapped charge can be rewritten as

$$Q_T = q\,\alpha N_S\,X_D\,W = 2\alpha\,\varepsilon\varepsilon_0\,V_{\rm D}\,W. \tag{2}$$

The trapped charge replenishes with the time constant τ_T that can vary in a wide range [16], typical values lying from milli- to micro-seconds. The current required to discharge the trapped charges can be found as

$$I_{\rm DC} = \frac{Q_T}{\tau_T} = 2\alpha\,\varepsilon\varepsilon_0\,V_{\rm D}\,\frac{W}{\tau_T}. \tag{3}$$

For typical values of $\tau_T \approx 10^{-3}$–10^{-6} s and maximal value $\alpha = 1$, the required discharging current $I_{\rm DC} \approx 10^{-8}$–$10^{-5}$ A/mm. For our test devices without gate electrodes, the I-V characteristics measured between the FP and ohmic contacts are shown in Fig. 3. For the dielectric 1, the current does not exceed 1 nA, which was not sufficient for the complete discharging of the trapped charges. For the dielectric 2, the current of $\sim 10^{-5}$ A was sufficient for the discharging and thus completely removes the current collapse in our devices.

At a relatively low drain bias, the width of high-field region is small and the trapped charge, being strongly field dependent, is relatively small too (α is low). For such a bias, a semiconducting dielectric can provide a path for the trapped charge discharging through the metal gate edges (shown as path #1 in Fig. 3). At higher drain bias however, the high-field region under the gate expands and the trapped charge density increases. The current through the gate edge is not sufficient to provide a discharge path. The field plate of an appropriate overhang, deposited on top of semiconducting dielectric significantly shortens the required path (path #2 in Fig. 3). However, if the conductivity of the dielectric under FP is too low, the current collapse is only partially removed. According to (1), the required FP overhanging for the discharging mechanism to work is around 1 μm for 50 V drain bias.

IV. Conclusion

The conductivity of the dielectric material under the filed plate plays a significant role in the current collapse removal. HFETs with a highly insulating dielectric under the FP show significant current collapse and premature RF power saturation. Identical HFETs with semiconducting dielectric layer under the FP exhibit perfectly linear RF power – drain bias dependence with the output powers of 20 W/mm at 55 V drain bias and essentially no current collapse. This improvement can be related to the trapped charge discharging to the FP through the leaky "semiconducting" dielectric.

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