

# **Megapixel CMOS Image Sensor Fabricated in Three-Dimensional Integrated Circuit Technology**

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**8 February, 2005**

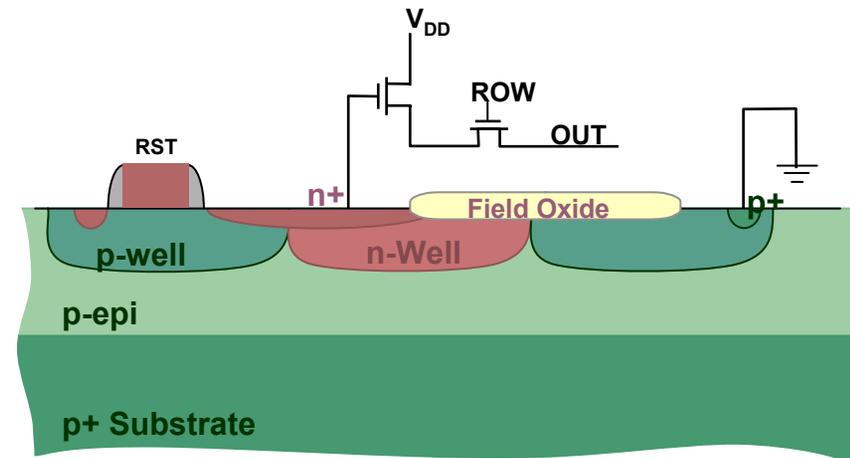
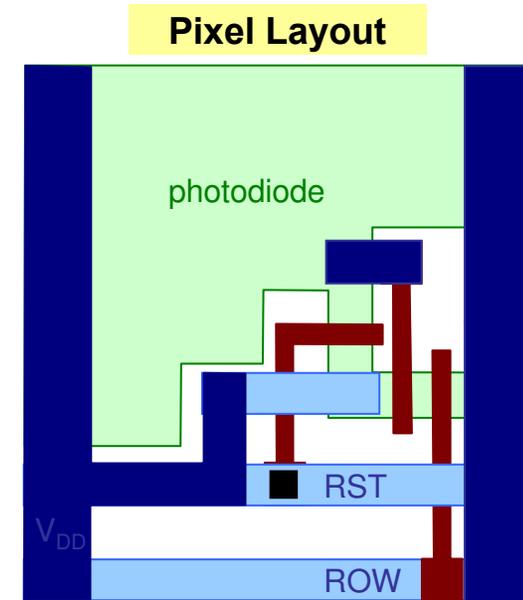
# Outline

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- **Advantages of 3-D for image sensors**
- **Megapixel 3-D imager array architecture**
- **Fabrication sequence**
- **Results**
- **Summary**

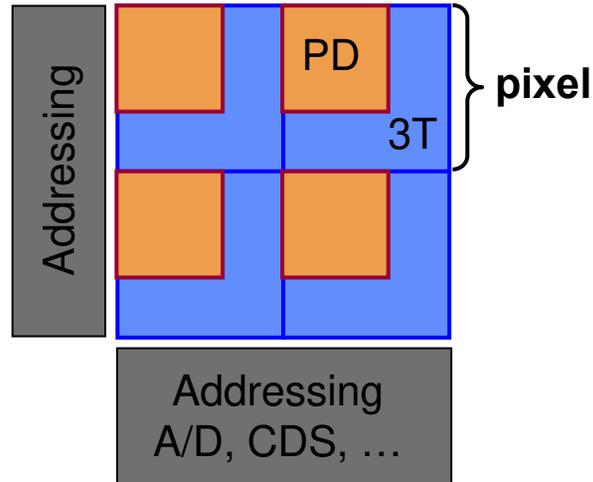
# Limitations – Standard Bulk CMOS APS

- **Fill factor compromised**
  - Photodetector and pixel transistors share same area
- **Low photoresponsivity**
  - Shallow junctions
  - High doping
  - Limited depletion depth
- **High leakage**
  - LOCOS/STI, salicide
  - Transistor short channel effects
- **Substrate bounce and transient coupling effects**



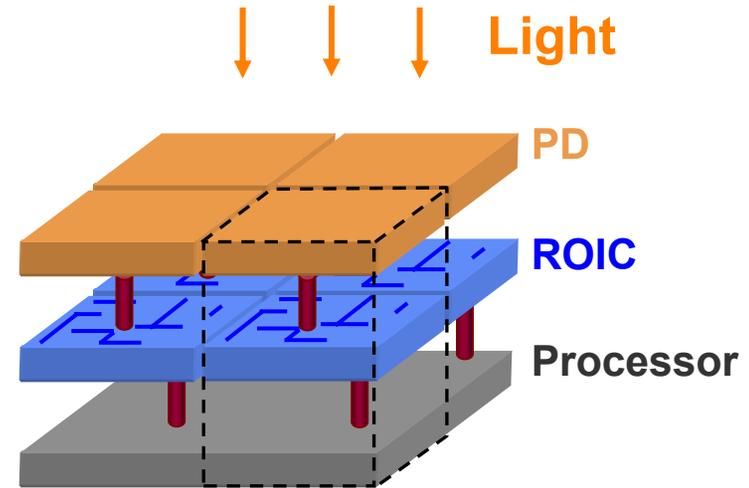
# Advantages of Vertical Integration

## Conventional Monolithic APS



- Pixel electronics and detectors share area
- Fill factor loss
- Co-optimized fabrication
- Control and support electronics placed outside of imaging area

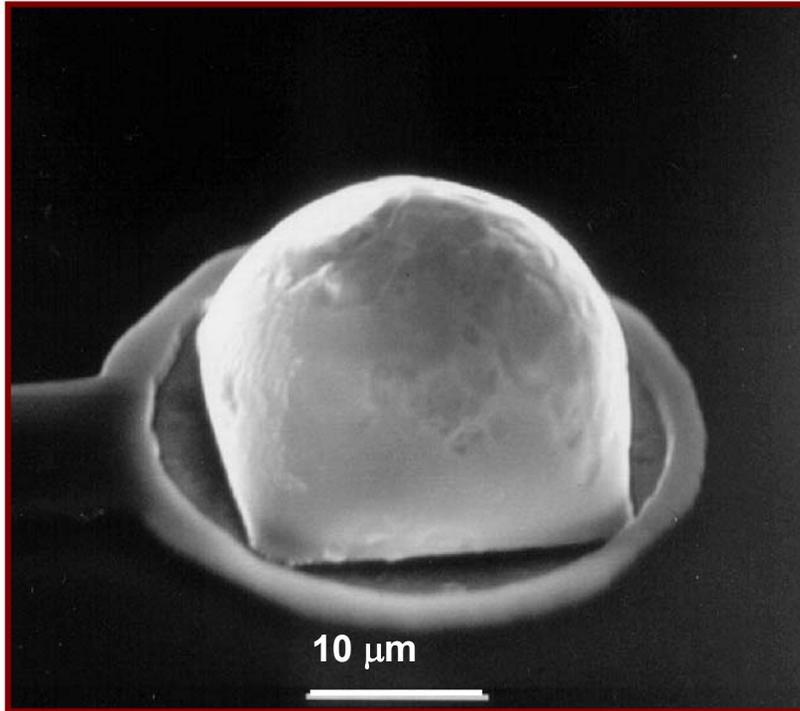
## 3-D Pixel



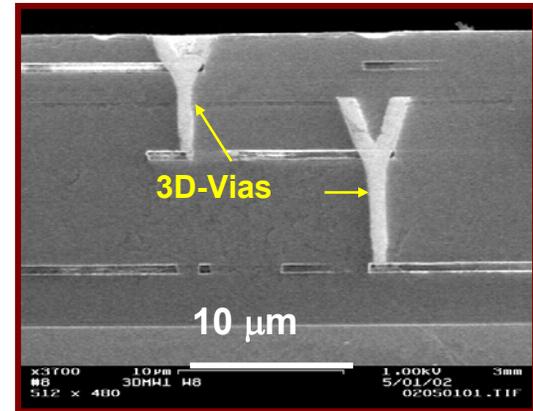
- 100% fill factor detector
- Fabrication optimized by layer function
- Local image processing
  - Power and noise management
- Scalable to large-area focal planes

# Approaches to 3D Integration

(To Scale)



**Bump Bond for  
Flip-Chip Interconnect  
Two circuit layers**



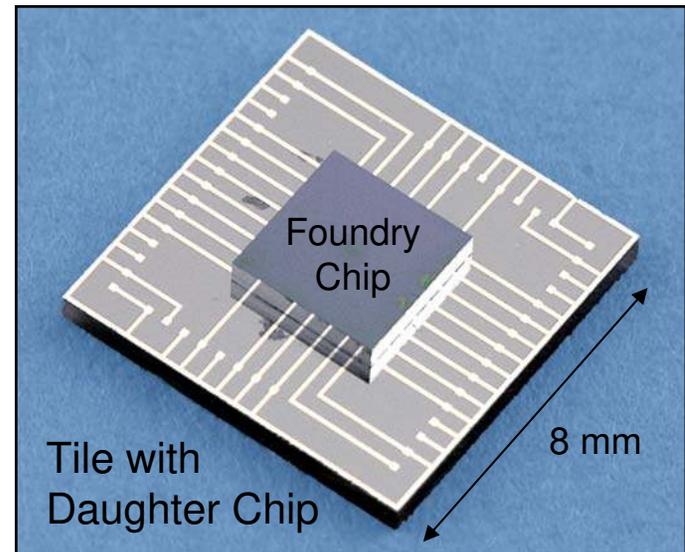
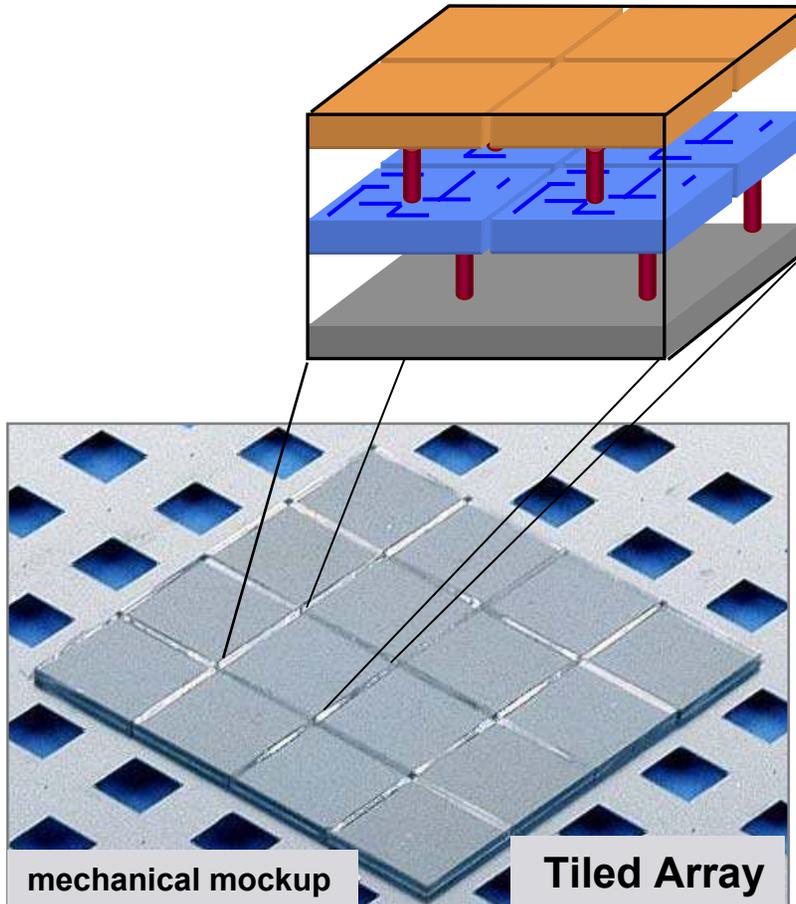
**Lincoln's SOI-based Vias  
3-D Interconnect  
Three circuit layers**

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# **Megapixel 3-D Imager Array Architecture**

# Four-Side Abutable Goal

- 3-D CMOS imagers tiled for large-area focal planes
- Foundry fabricated daughter chip bump bonded to non-imaging side

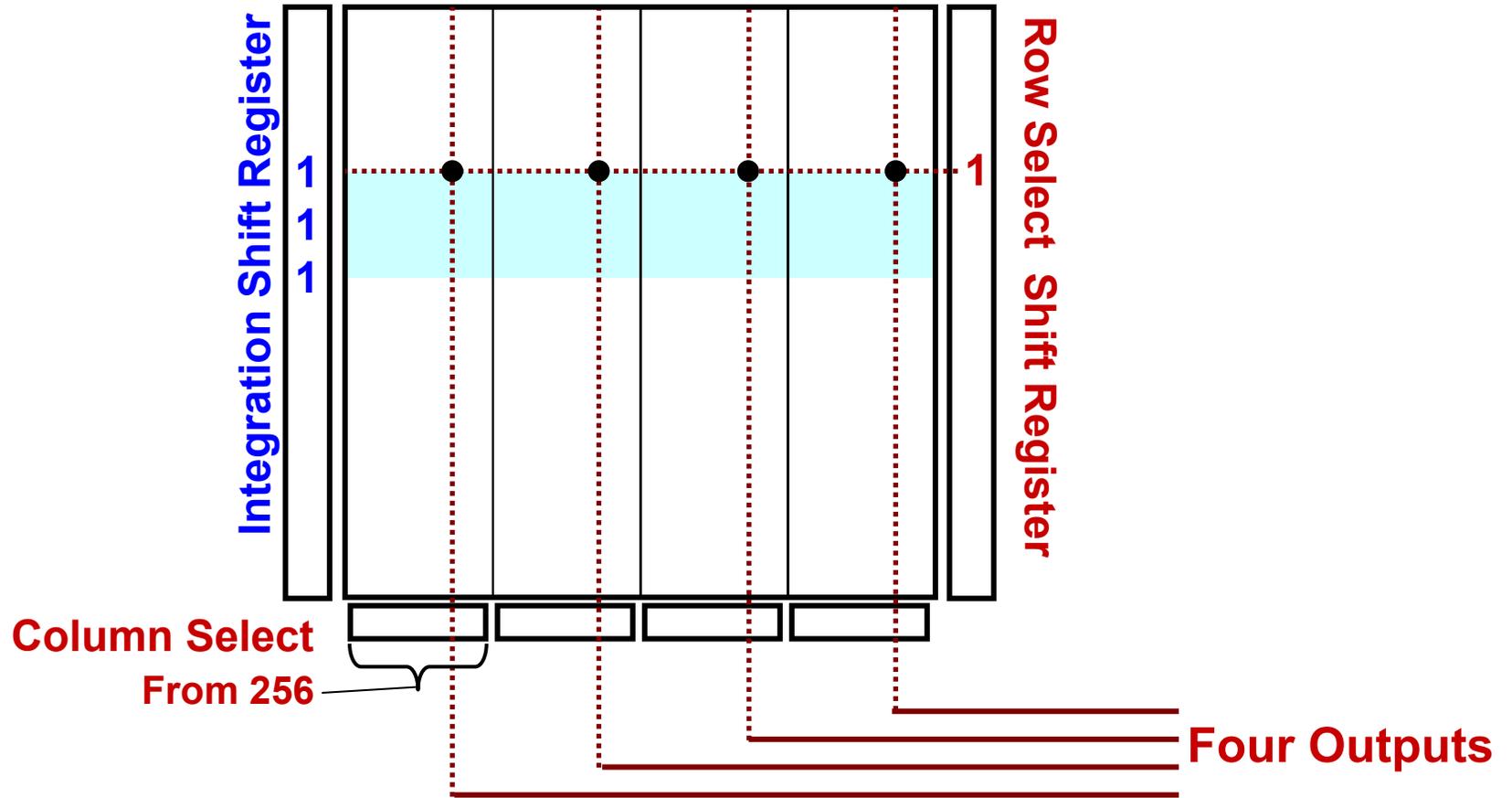


# Design Goals

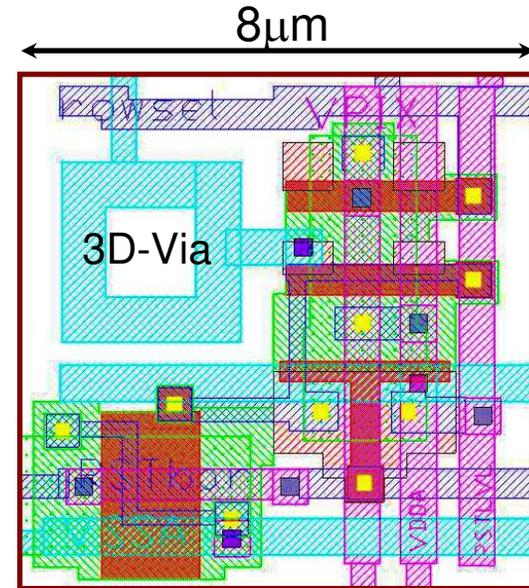
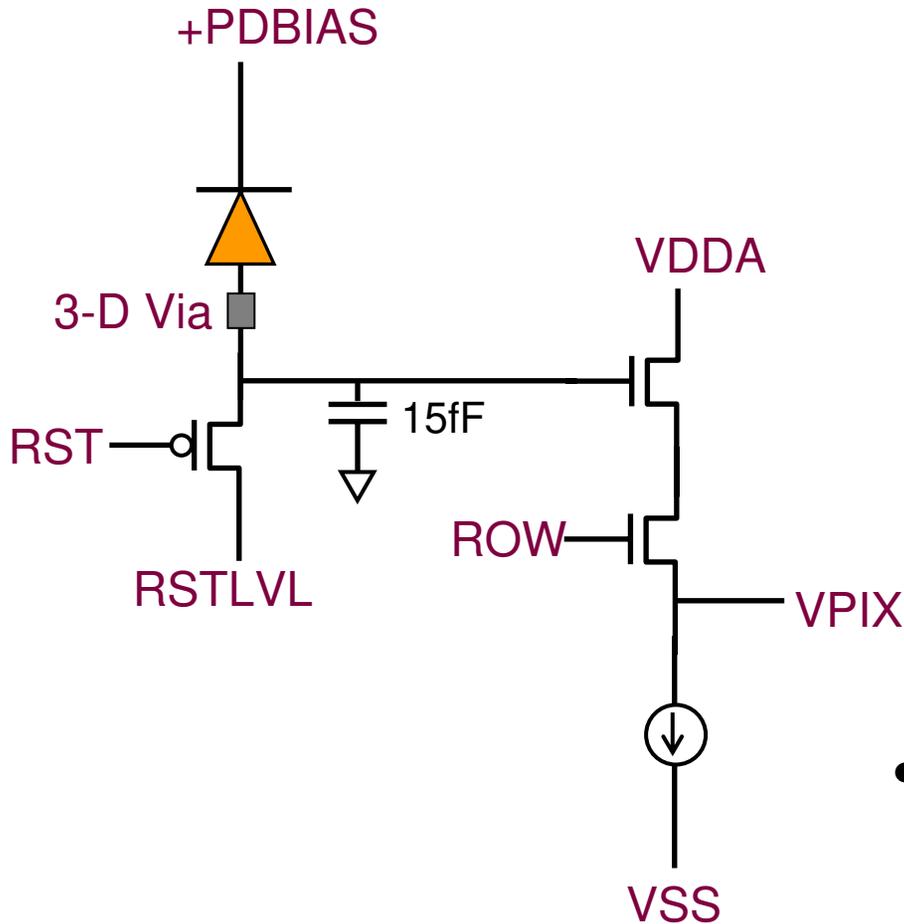
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- **Four-side abutable Active Pixel Sensor**
- **1024 x 1024 array of  $8\mu\text{m} \times 8\mu\text{m}$  pixels**
- **3-D interconnections per pixel**
- **3.3-V operating voltage**
- **Full digital control and readout at 10 fps**

# 1024 x 1024 Imager Array Architecture



# 3T Pixel Schematic and Layout



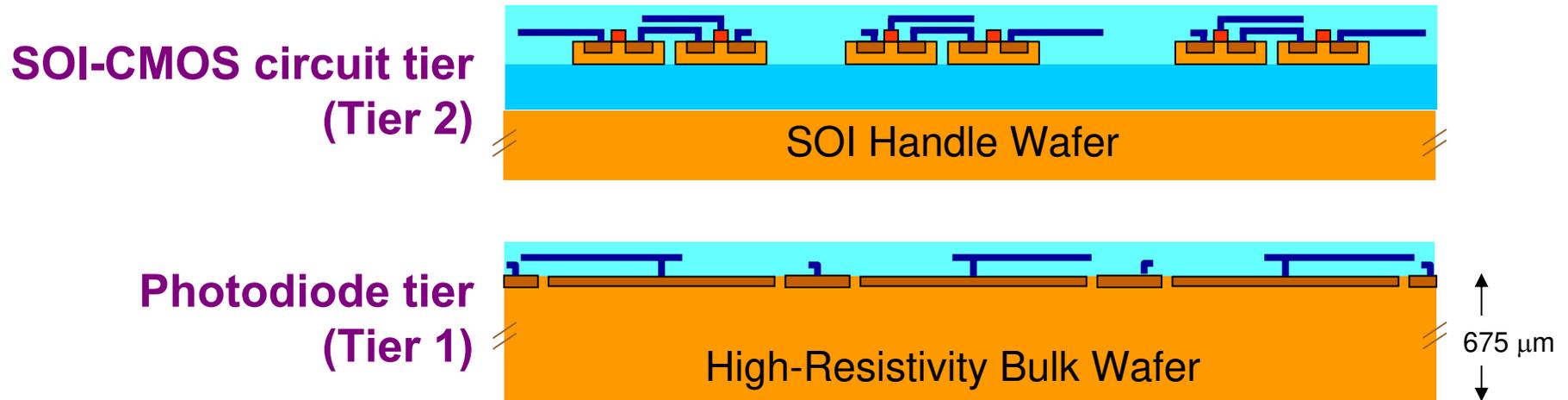
- **Design Variations**
  - pFET Reset with 15fF capacitor
  - nFET Reset with no capacitor

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# Fabrication Sequence

# Single Tier Circuit Fabrication

- **Photodiode and SOI circuit wafers fabricated separately**
  - 150-mm wafer processes
  - 350-nm gate length fully depleted SOI-CMOS technology
  - Low dark current, 100% fill factor photodiodes



# 3-D Circuit Integration Technology

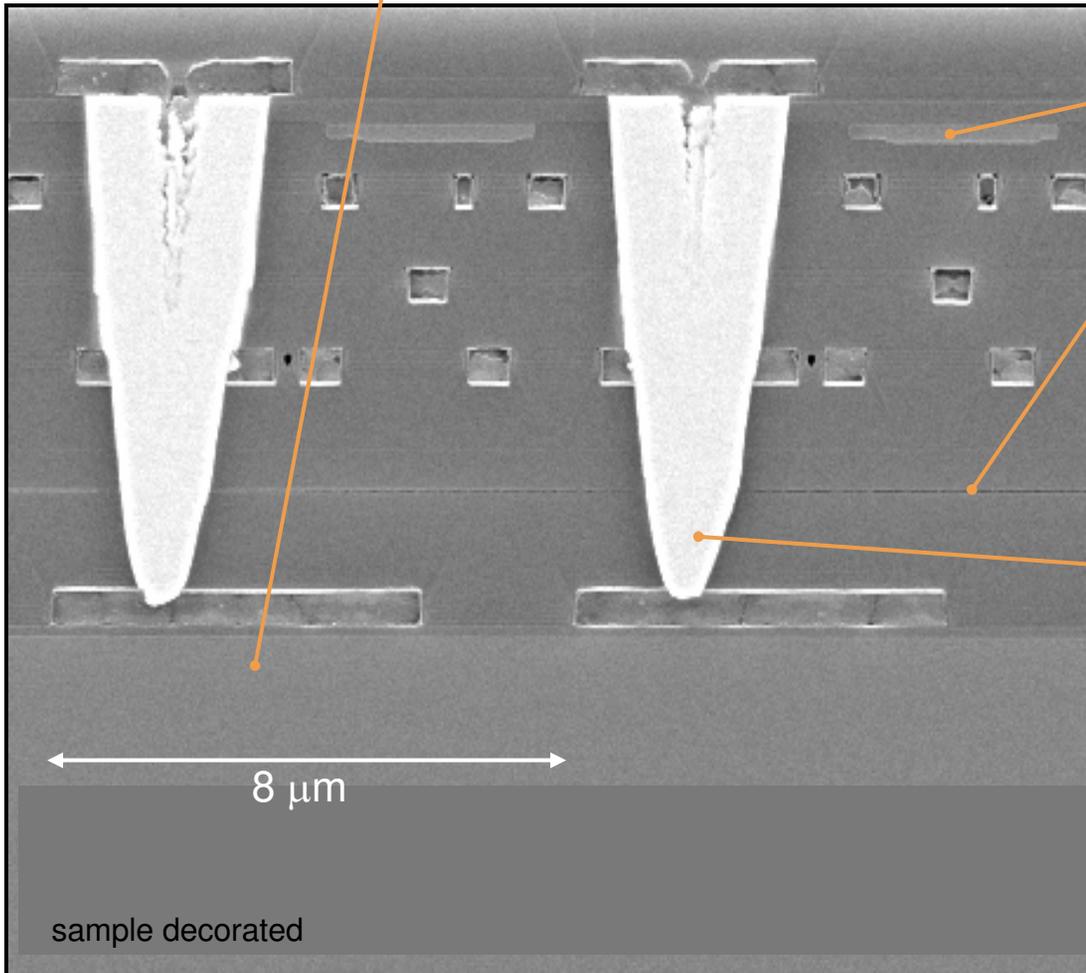
## Key Components

1. Low dark current photodiodes

2. SOI Circuits

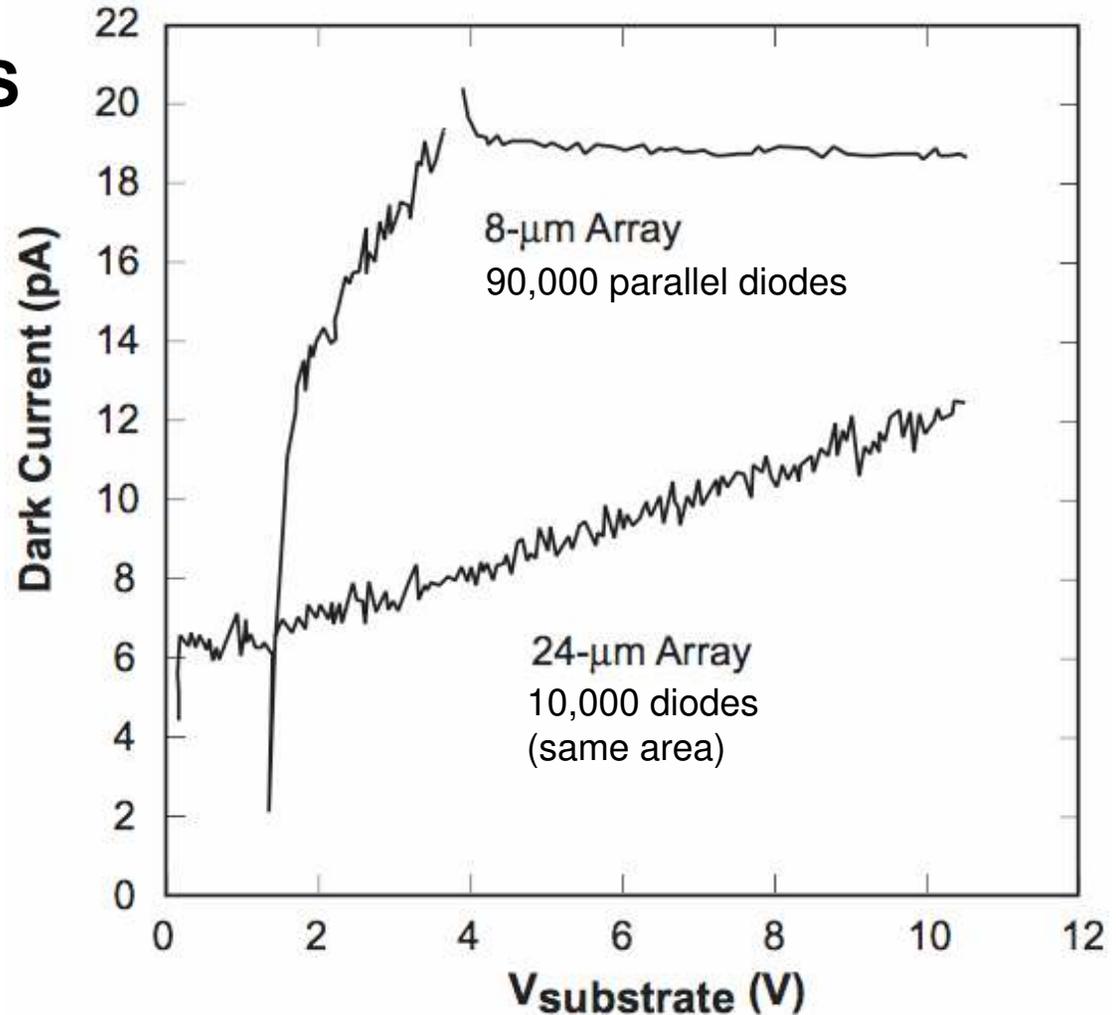
3. Low-temperature oxide-oxide bond

4. Vertical interconnect



# 1. Low Dark Current Photodiodes

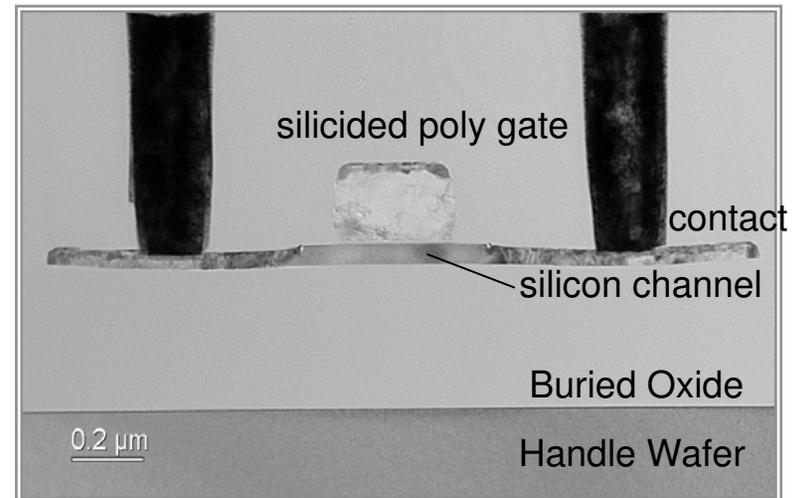
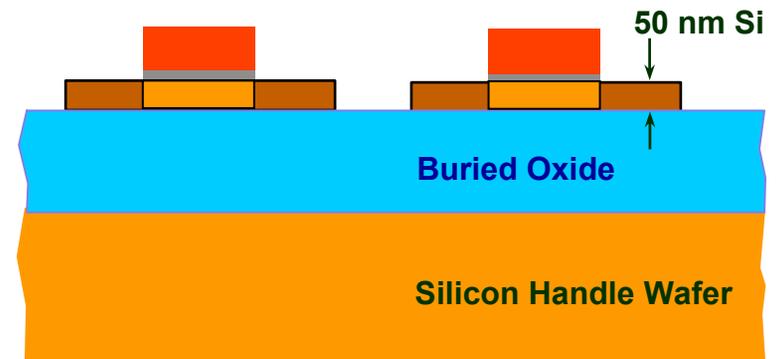
- Photodiode independent of CMOS
- High-resistivity substrates
- Back-illumination process
- Photodiode leakage  $< 0.2 \text{ nA/cm}^2 @ 25^\circ\text{C}$
- Similar results after 3D-stacking



Single tier test structure w/guard ring  
Full thickness wafer

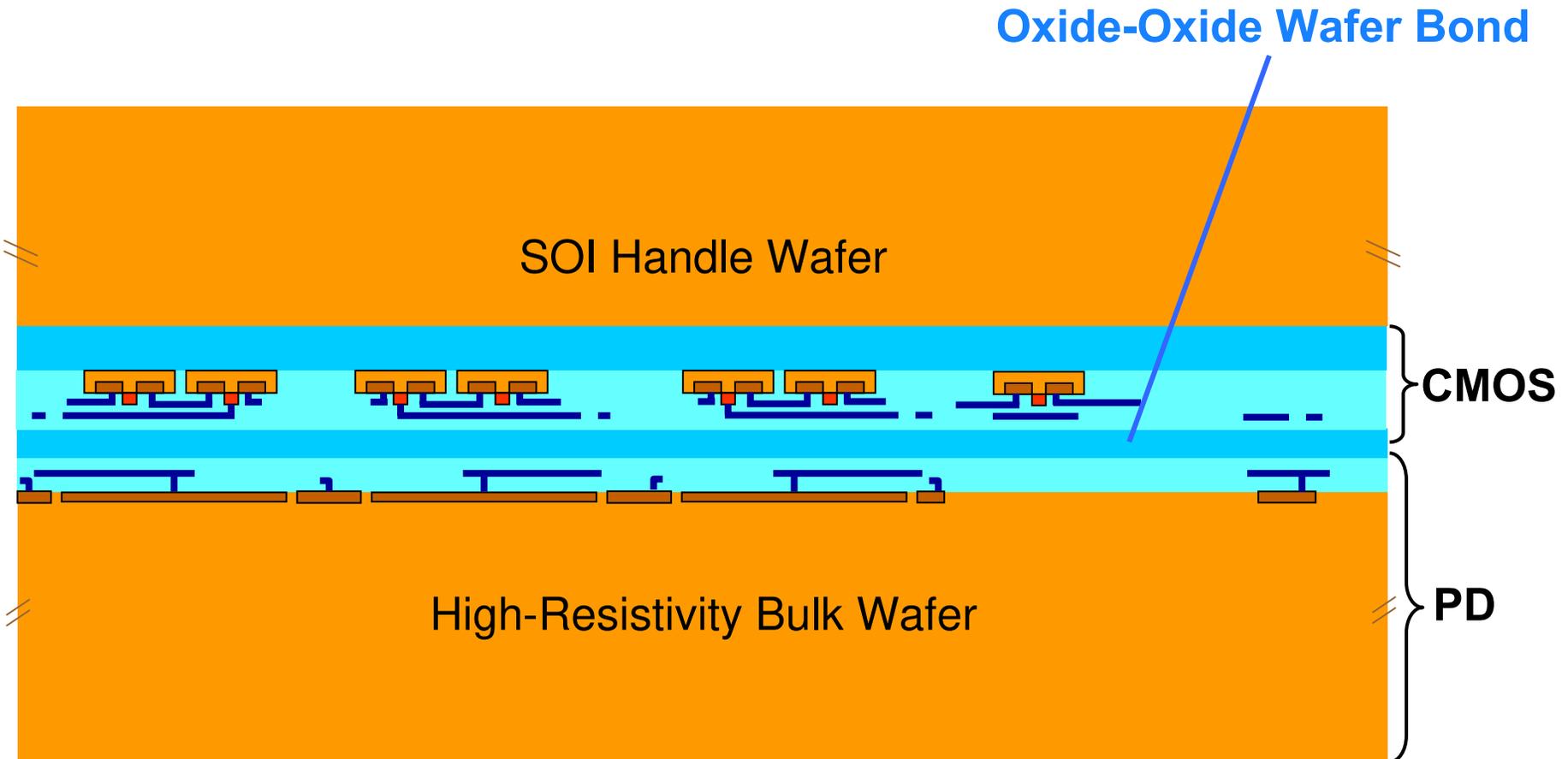
## 2. Silicon-On-Insulator Circuits

- 3.3-V, 350-nm gate length, fully depleted SOI CMOS
- Buried oxide
  - Dielectric isolation
  - Reduced parasitic capacitances
  - Enhanced radiation performance
  - Essential wafer-thinning etch stop



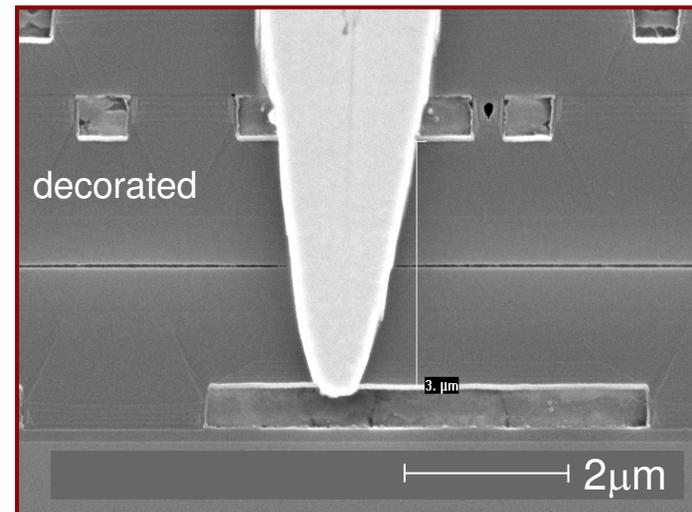
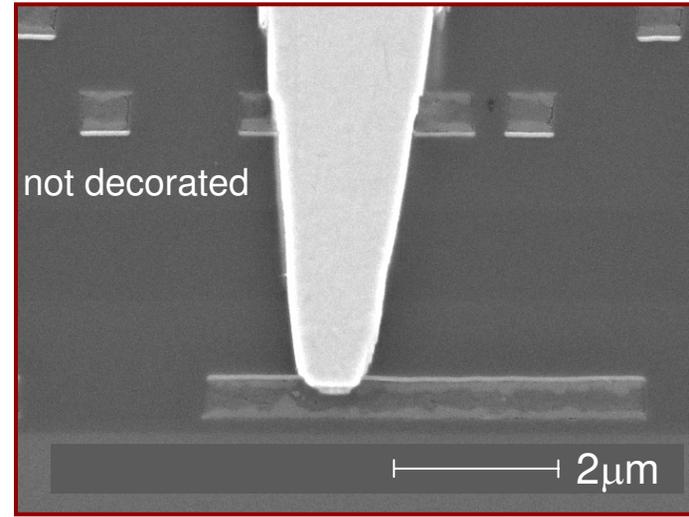
# 3-D Circuit Stacking

- Invert, align, and bond Tier 2 to Tier 1



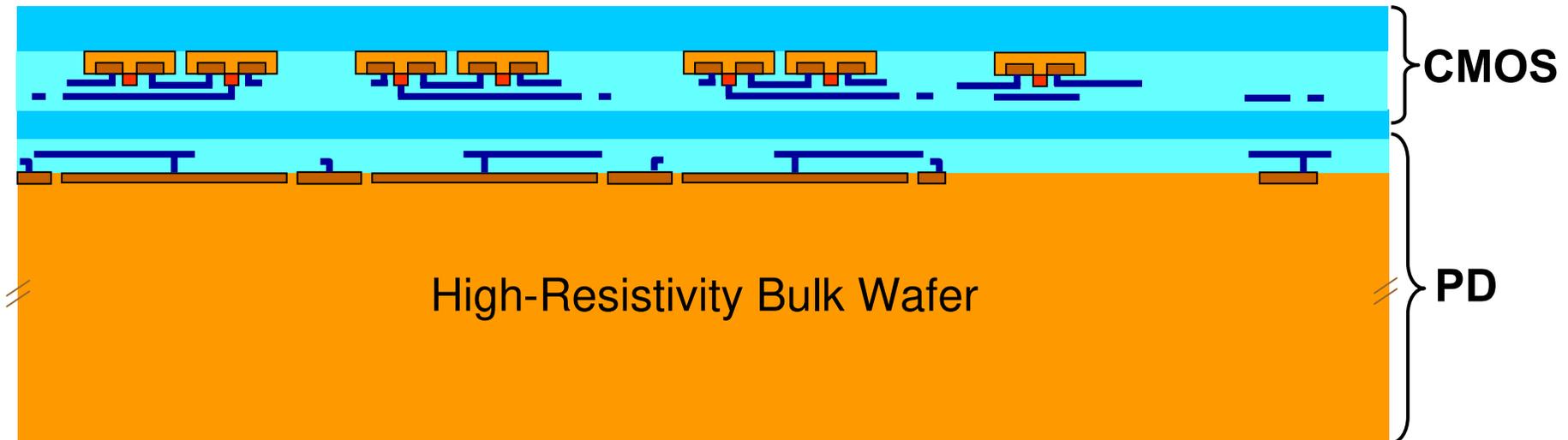
# 3. Low Temperature Oxide-Oxide Bond

- **Wafer-scale, CMOS-compatible oxide bond formed at 275°C**
  - Permits plugfill and metallization
  - Permits hydrogen passivation
  - Maintains CMOS channel engineering
- **SOI buried oxide etch stop**
- **Currently 2- $\mu\text{m}$  wafer-to-wafer alignment tolerances**
  - Next generation is 0.25 $\mu\text{m}$

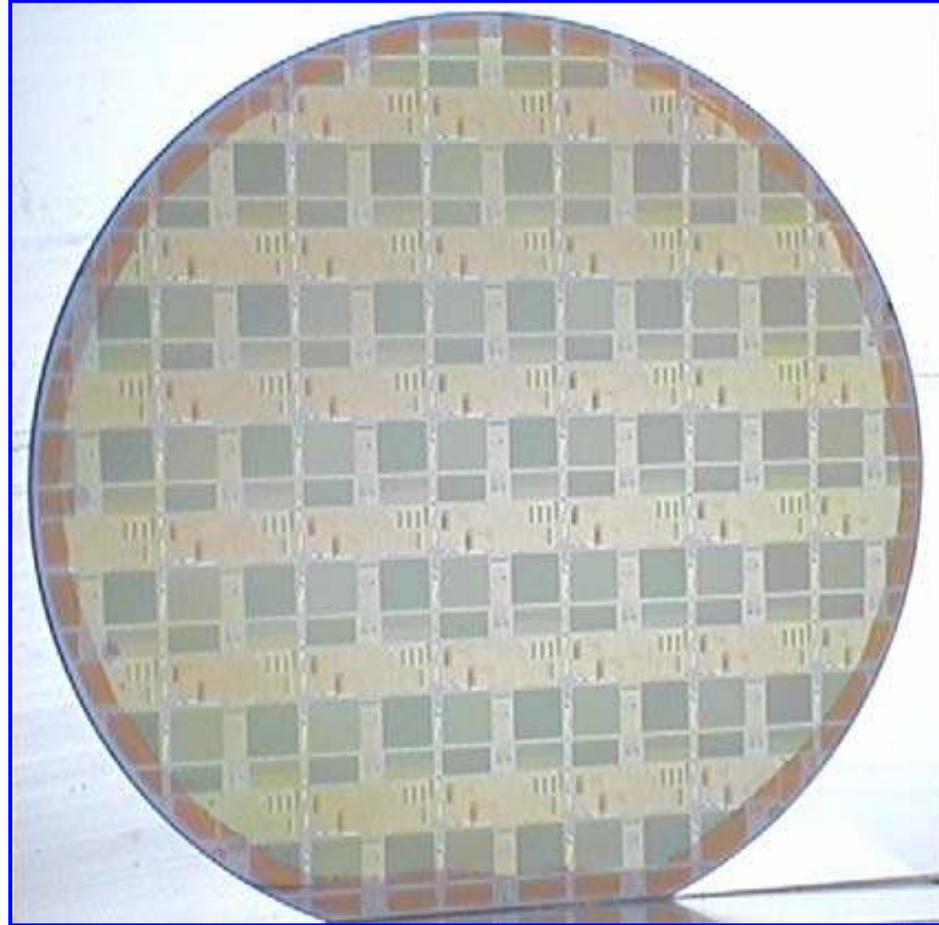


# 3-D Circuit Stacking

- Remove handle silicon from Tier-2



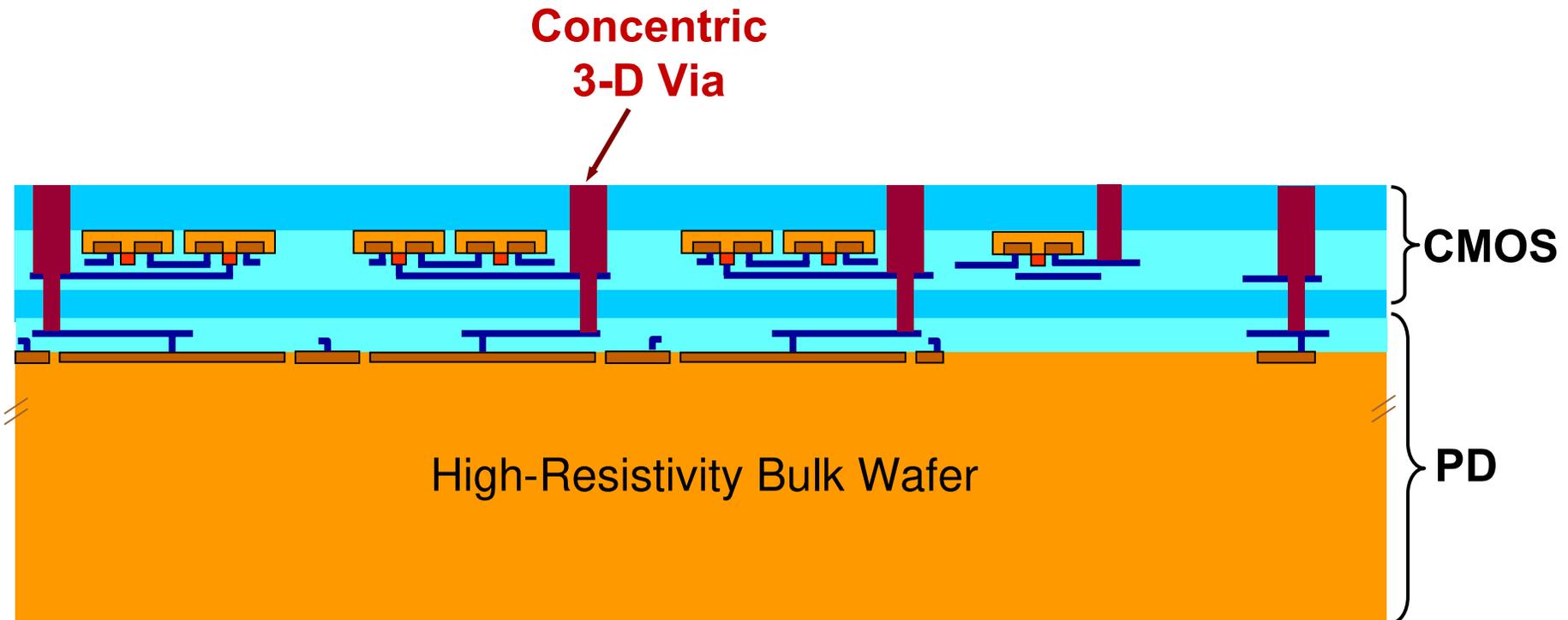
# Bonded Two Wafer Imager Stack



**150-mm Diameter Wafer Pair**

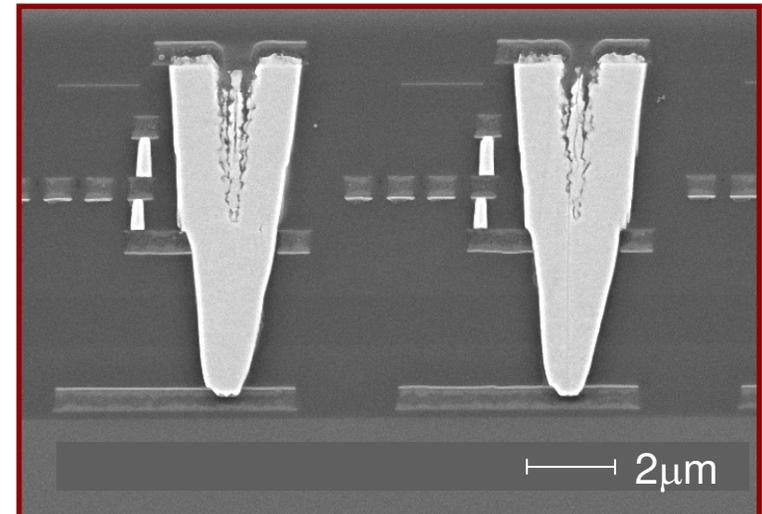
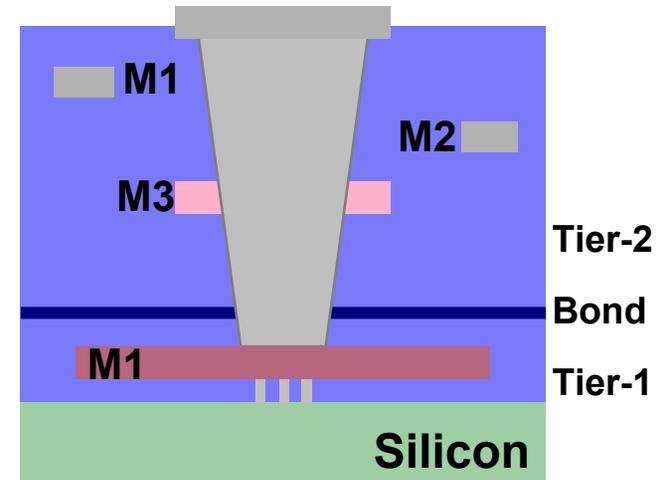
# Inter-Tier Via Connections

- Pattern, etch, and fill 3-D vias
- (Additional circuit tiers could be added)



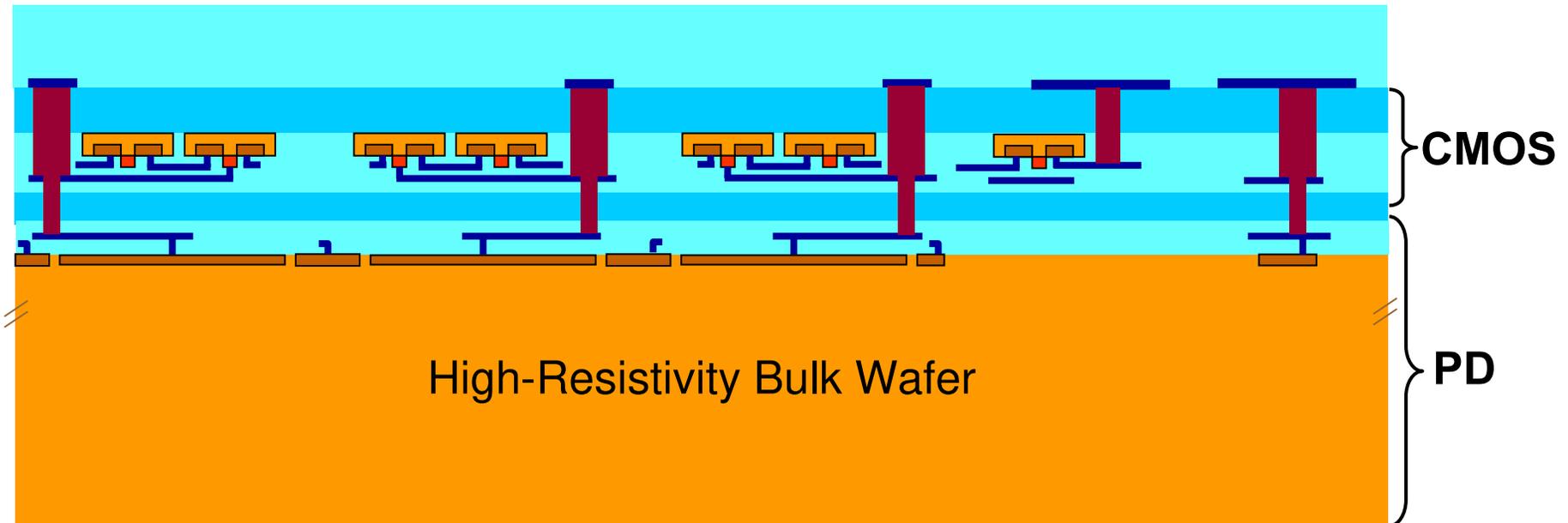
# 4. Micron-Scale Vertical Interconnect

- **Wafer-scale process**
  - Compact layout with concentric 3D via
  - > 1 million 3D vias in 1024x1024 imager
  - High aspect ratio (4:1) etch
  
- **3-D via yield  $\geq 99.999\%$  on functional imagers**



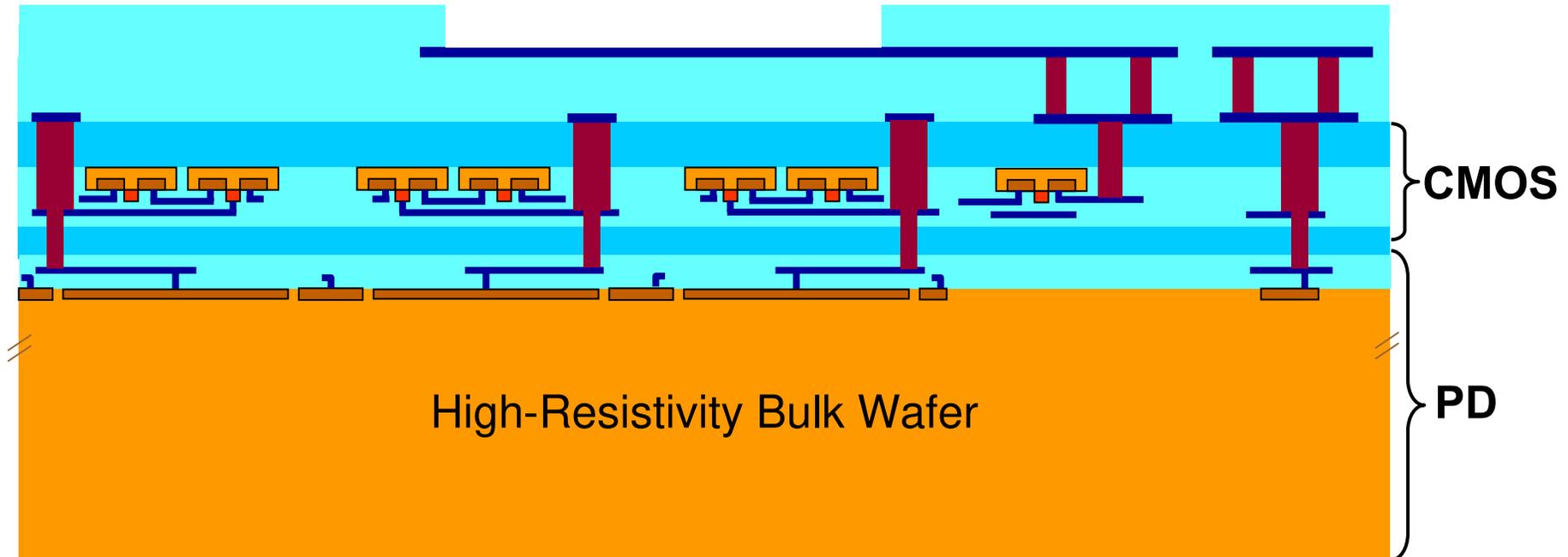
# Test Pad Metal-1

- Deposit and pattern Test Pad Metal-1



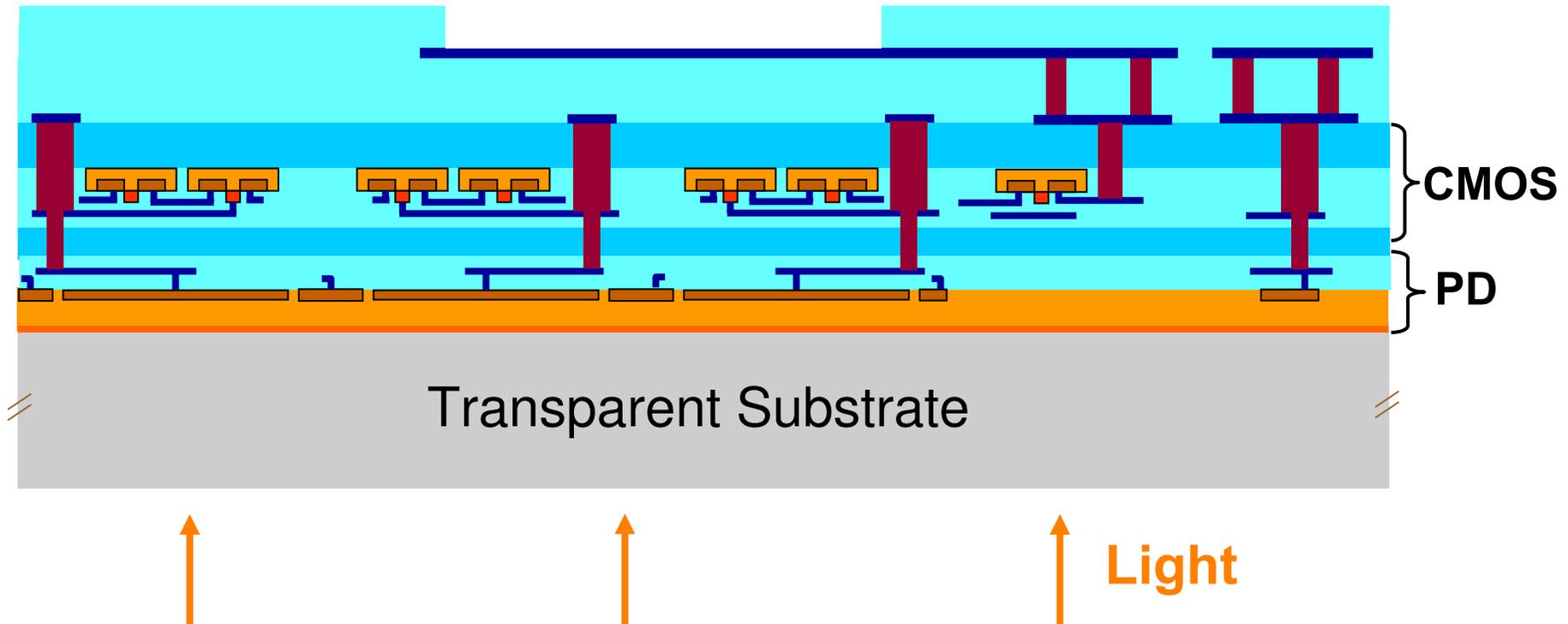
# Test Pad Metal-2

- Deposit and pattern Test Pad Metal-2
- Sinter



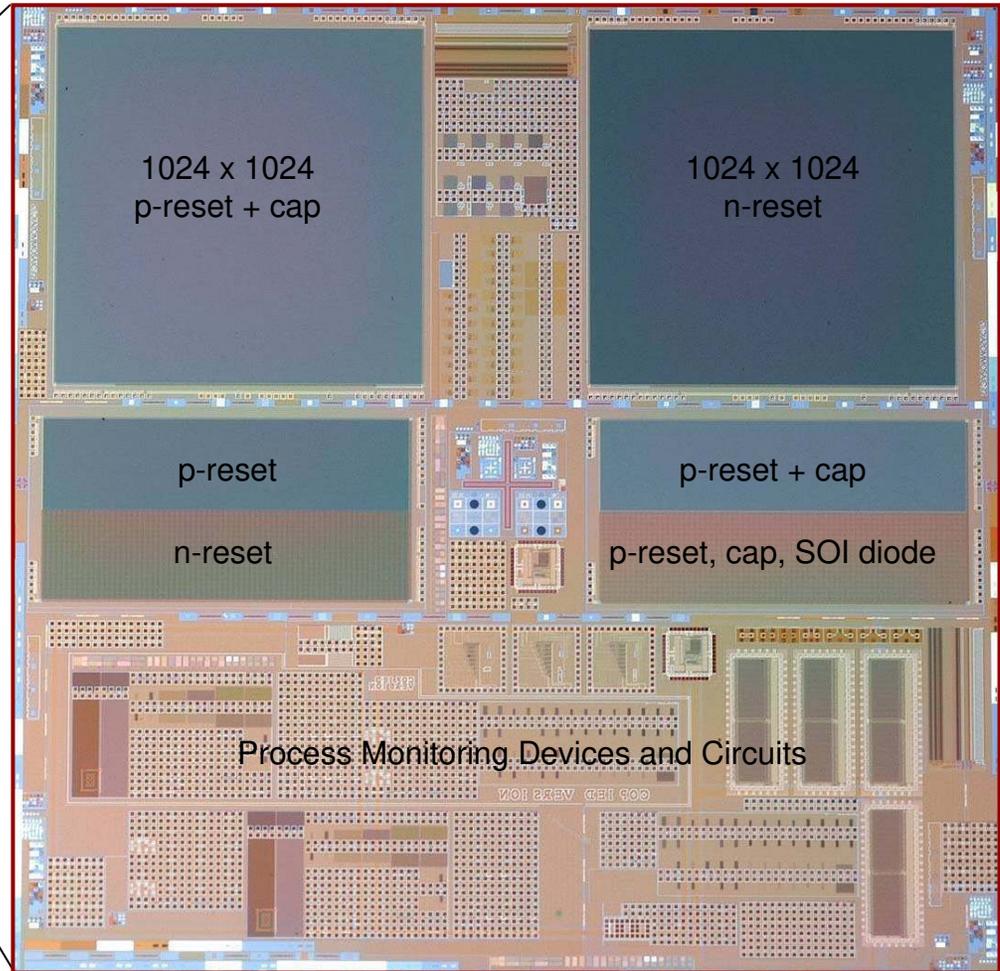
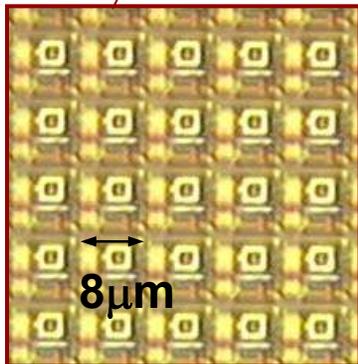
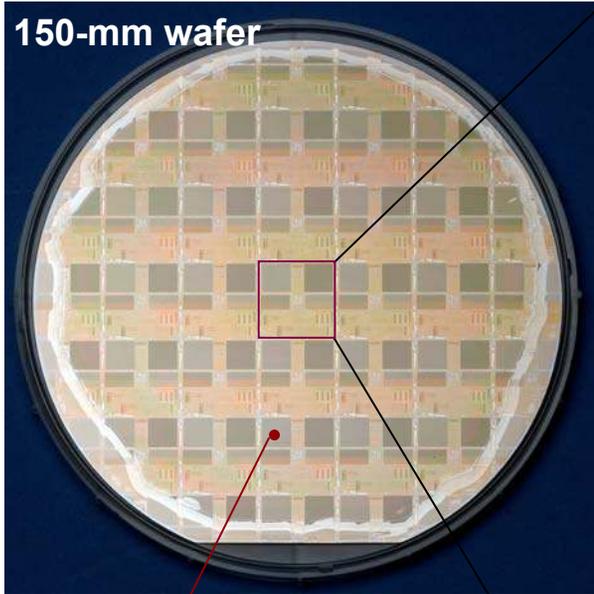
# Completed Back-Illuminated CMOS Imager

- Thin photodiode substrate to  $50\mu\text{m}$
- Epoxy bond to quartz



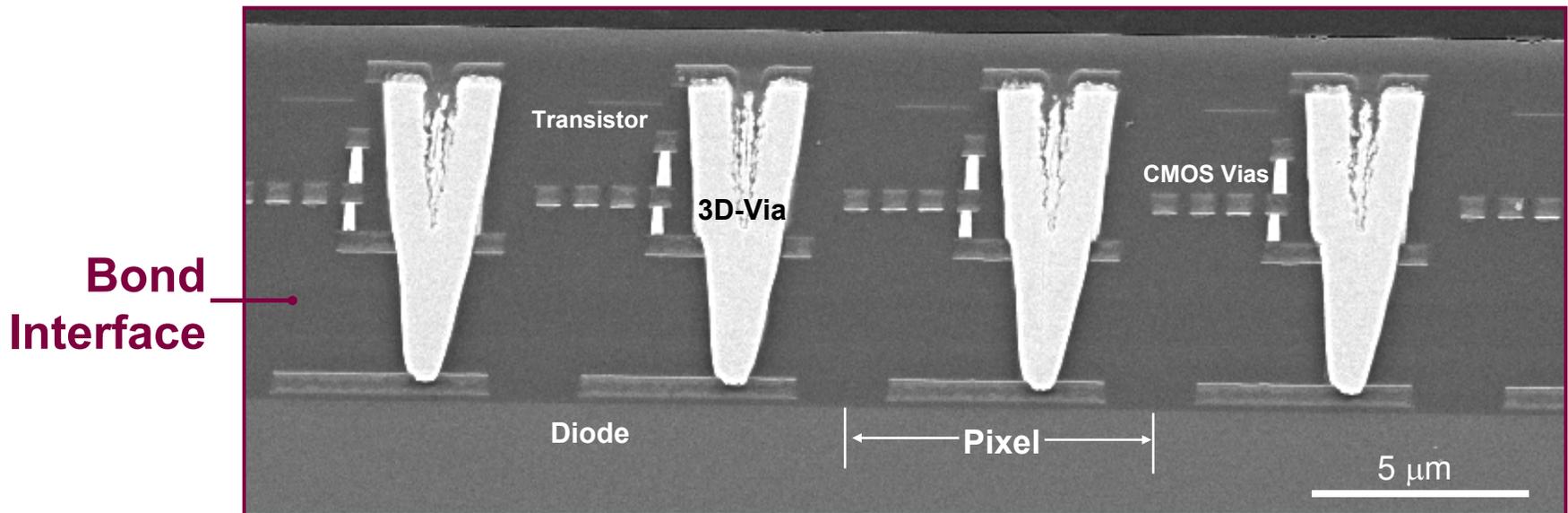
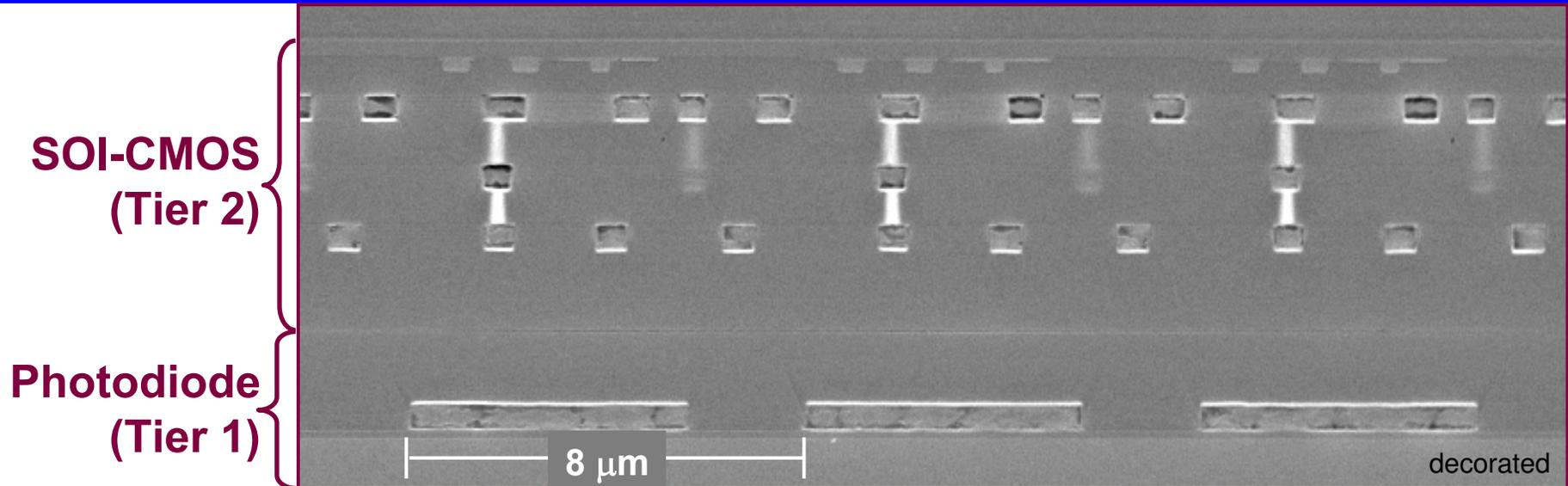
# Completed 3D-Stacked Imager Wafer and Die Layout

150-mm wafer



22 mm

# Cross Sections Through 3-D Imager

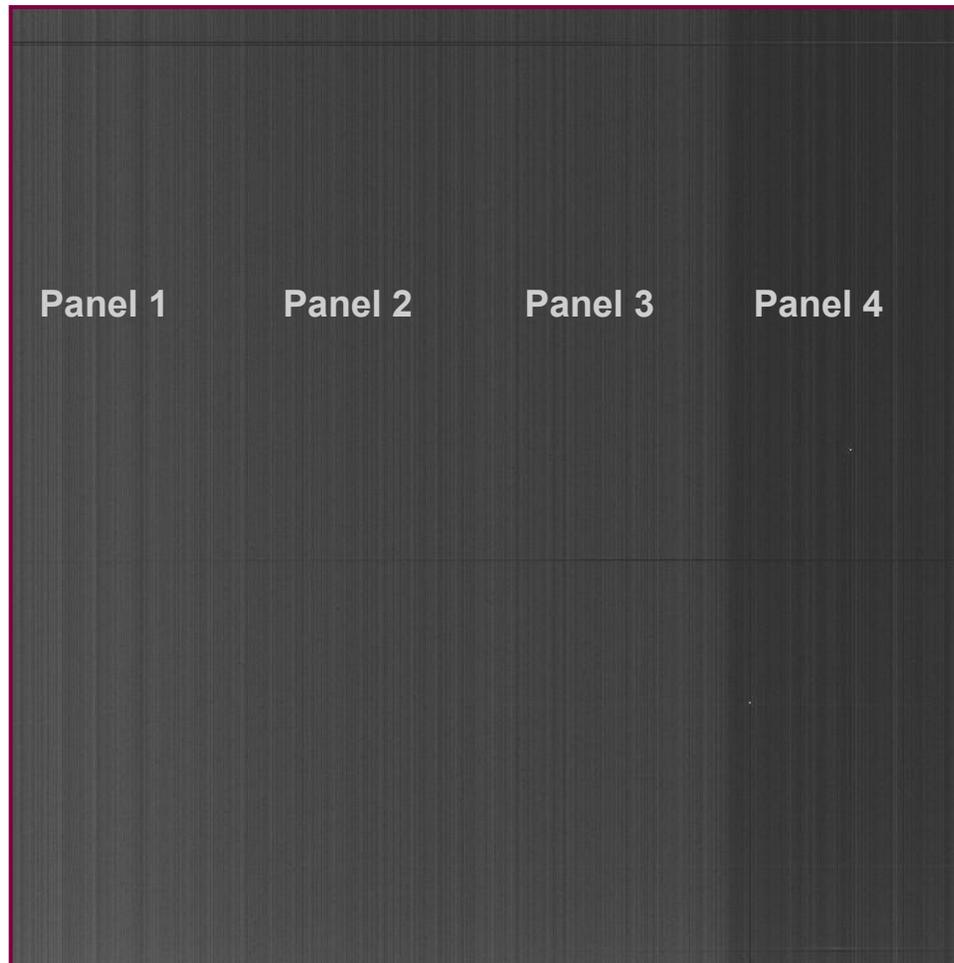


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# Results

# Sample Dark Background

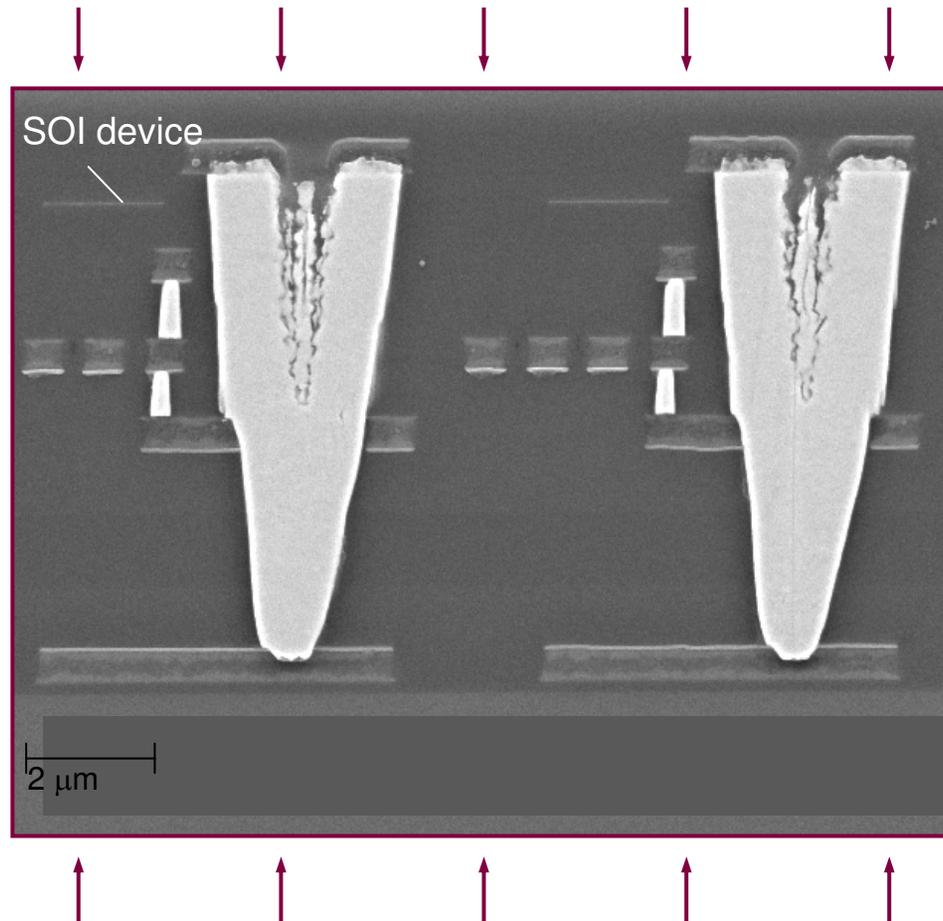
- Raw image without fixed pattern noise suppression
- Dominant yield detractor is row/column drop-outs



Four  
Analog  
Outputs

# Terminology

## Front Illumination

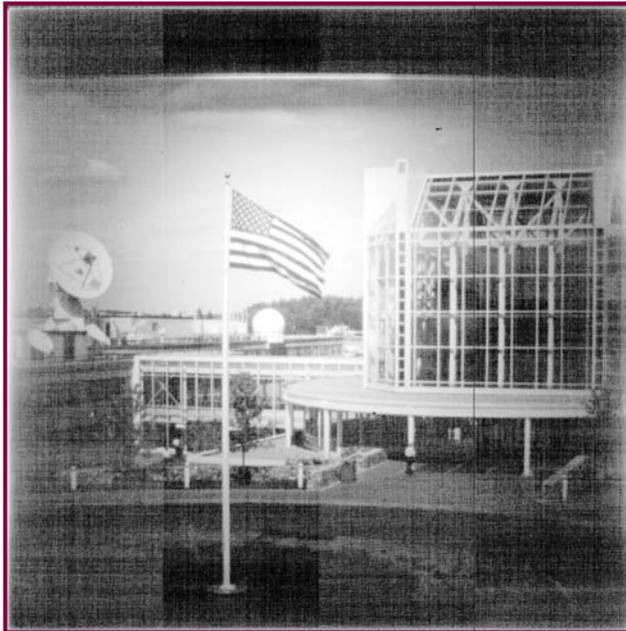


## Back Illumination

# Example Raw Imagery (Front Illuminated)

- Full thickness wafer
- Wafer probe-level test
- 10.5 frames/sec

pFET reset



nFET reset



# Packaged Device (Front Illuminated)

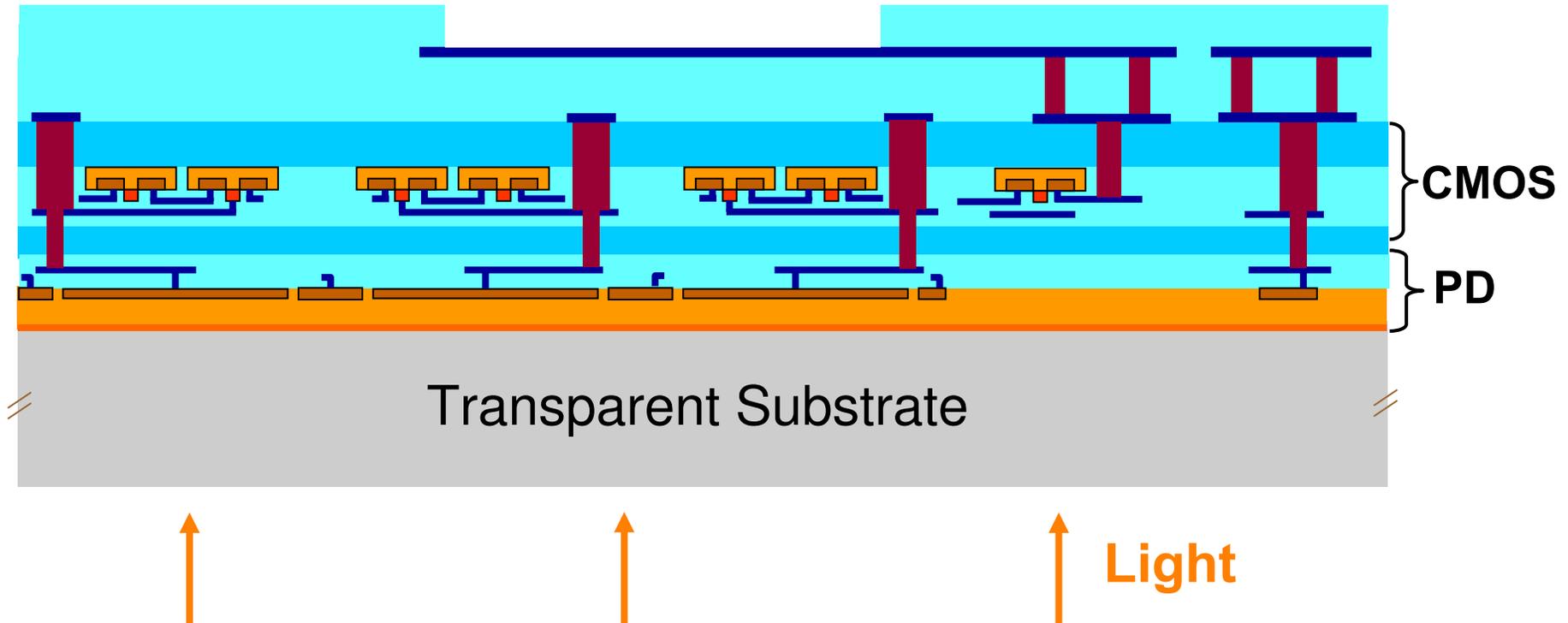
## Full Thickness Diode Wafer

1024 pixels

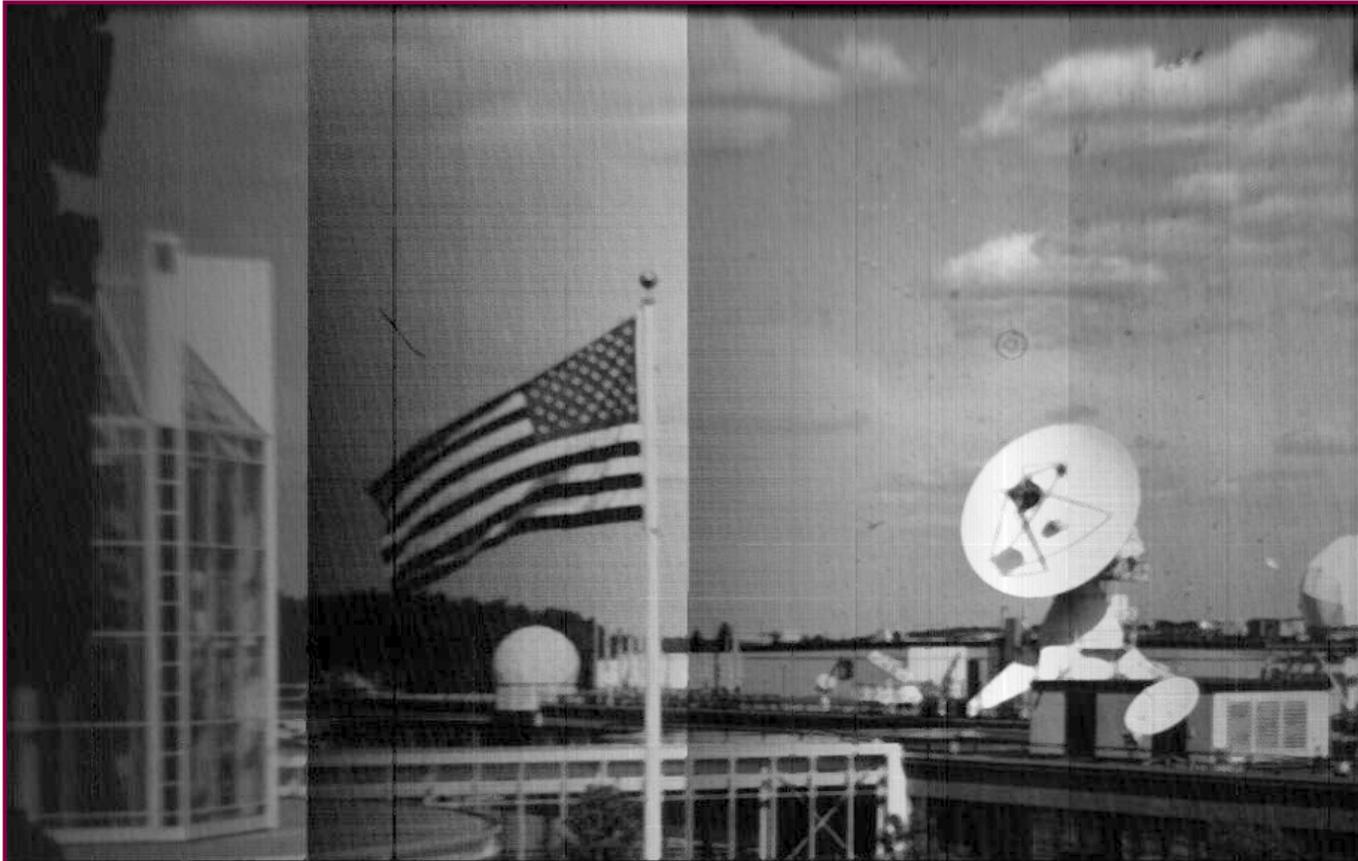


1024 pixels, ( $8\mu\text{m} \times 8\mu\text{m}$ )

# Back-Illuminated 3-D CMOS Imager



# Packaged Device (Back Illuminated)



(partial frame)

# Results Summary

<b>150-mm Wafer Technology</b>	<b>Bulk p+/n Photodiode 0.35<math>\mu</math>m FDSOI CMOS Per-pixel 3-D Integrated Backside Illumination</b>
<b>3-D Via Count</b>	<b>&gt; 1 million</b>
<b>3-D Via Yield</b>	<b>&gt; 99.999%</b>
<b>Transistor Count</b>	<b>&gt; 3.8 million</b>
<b>Photodiode Dark Current</b>	<b>&lt; 0.2 nA/cm<sup>2</sup></b>
<b>Imager Dark Current</b>	<b>1-3 nA/cm<sup>2</sup></b>
<b>Responsivity</b>	<b>w/Cap: 2.7<math>\mu</math>V/e-    No Cap: 9.4<math>\mu</math>V/e-</b>
<b>Well Capacity</b>	<b>w/Cap: 350ke-    No Cap: 85ke-</b>

# Summary

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- **Extendable focal plane fabricated in SOI-based 3-D circuit stacking technology**
  - 1024x1024 array of 8 $\mu$ m x 8 $\mu$ m pixels
  - Per-pixel 3D interconnections
  - 100% fill factor, deep-depletion, back-illuminated photodiodes
- **Two imager designs demonstrated**
  - Operational at >10 fps
  - 3-D via yield > 99.999%
- **All imager circuits operate after 50- $\mu$ m wafer thinning for Back Illumination**