INVITED PAPER

Memristive Device Fundamentals and Modeling: Applications to Circuits and Systems Simulation

This paper presents SPICE ready circuit models that system designers can use to accurately measure the behavior of memristor-based large systems.

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ABSTRACT | The nonvolatile memory property of a memristor enables the realization of new methods for a variety of computational engines ranging from innovative memristive-based neuromorphic circuitry through to advanced memory applications. The nanometer-scale feature of the device creates a new opportunity for realization of innovative circuits that in some cases are not possible or have inefficient realization in the present and established design domain. The nature of the boundary, the complexity of the ionic transport and tunneling mechanism, and the nanoscale feature of the memristor introduces challenges in modeling, characterization, and simulation of future circuits and systems. Here, a deeper insight is gained in understanding the device operation, leading to the development of practical models that can be implemented in current computer-aided design (CAD) tools.

KEYWORDS | Conductance modulation index; content addressable memory (CAM); memory; memristor; memristor-based content addressable memory (MCAM); SPICE modeling

I. INTRODUCTION

Traditionally, there are only three fundamental passive circuit elements: capacitors, resistors, and inductors, discovered in 1745, 1827, and 1831, respectively. However, one can set up five different mathematical relations between the four fundamental circuit variables: electric current i, voltage V, electric charge q, and magnetic flux Φ. For *linear* elements, $f(V,i)=0$, $f(V,q)=0$, where $i=dq/dt$ $(q=CV)$, and $f(i,\Phi)=0$, where $V=d\Phi/dt$ $(\Phi=Li)$, indicate linear resistors, capacitors, and inductors, respectively.

In 1971, Chua proposed that there should be a fourth fundamental passive circuit element to set up a mathematical relationship between $q(\int_t i)$ and $\Phi(\int_t V)$, which he named the *memristor* (a portmanteau of *memory* and *resistor*) [1]. Chua predicted that a class of memristors might be realizable in the form of a pure solid-state device without an internal power supply.

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In 2008, Strukov *et al.* [2], at Hewlett-Packard (HP), announced the first physical realization of a memristor device based on a TiO_2 thin film doped with oxygen vacancies. The doping process entails removing the negatively charged oxygen atom from its substitutional site in TiO_2, which creates a positively charged oxygen vacancy. These vacancies are formed at the time of crystallization. By applying an electric field, ions move in the direction of current flow. The nonlinearity that characterizes a memristor implies that the charge that flows through a memristor dynamically changes its internal state.

The new location of the ions can be read out as a change in the resistance (state) of the material thus permitting the realization of a new class of low-power ultradense devices [3]. A resistor with memory is not a new concept. For example, a memristive device, due to Choi *et al.* [4], exploited a TiO_2 thin layer, and predated the HP work. Nonvolatile memory dates back to 1960 when Bernard Widrow introduced a new circuit element named the *memistor* [5]. The rationale for choosing the name "memistor" is the same as the memristor, a resistor with memory. However, the memistor has three terminals and its resistance is controlled by the time integral of a current signal, which implies that the resistance of the memistor is controlled by charge. Widrow devised the memistor as an electrolytic memory element to form a basic structure for a neural circuit architecture referred to as ADAptive LInear NEuron (ADALINE) [5]. In the 1960s, Simmons [6] published the very first report on metal–insulator–metal (MIM) I–V curve, illustrating the hysteresis effect associated with a MIM structure, that characterized tunneling current behavior.

This paper has the following structure. Section II is an introduction that highlights the periodic table of circuit elements and how it provides a better insight into the family of fundamental elements with memory. In Section III, we briefly review available memristor models, with regard to their suitability for SPICE implementation. Here, we describe our new SPICE model based on a modified Simmons tunneling relation and illustrate the significance of the *conductance modulation index* σ_M for better understanding of memristor dynamics. Building upon the presented fundamentals, Section IV provides a circuit case study for the realization of a memristor-based content addressable memory (MCAM).

II. MEMRISTOR AND MEMRISTIVE DEVICES WITHIN CHUA'S PERIODIC TABLE

In 2003, Chua [7] introduced a "periodic table" of the fundamental passive circuit elements. The table is based on differentials and integrals of the two basic circuit variables i and V, which can be extended to higher orders as desired. An interesting property of this periodic table is that vertically it is cyclic with period four. We can see this intuitively, if using sinusoidal functions of time for q or V, in that after four differentials we return to the original function. We present an alternative simplified view of the periodic table in Fig. 1.

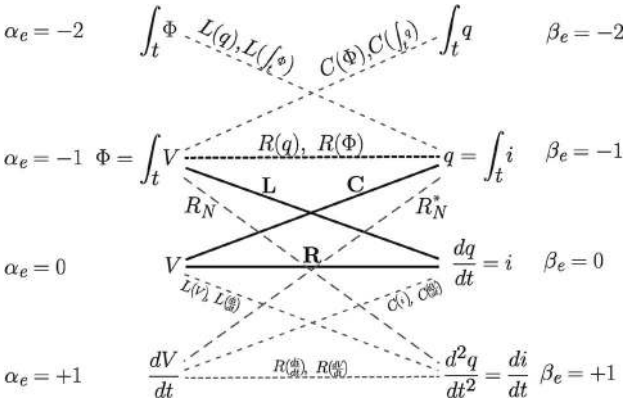


Fig. 1. ***Classification of circuit elements. The two circuit variables, current i and potential V, are placed in a sequence of differentials as shown above. The three basic circuit elements C, L, and R that link the four circuit variables V, i, Φ, and q are shown in bold. The memristor $(R(q), R(\Phi))$ links flux and charge. The meminductor and the memcapacitor also link the higher order integrals $\int_t \Phi$ and $\int_t q$ [8]. The α_e and β_e are used for element identification using Chua's periodic table of circuit elements from [7]. According to the periodic table, there are two types of negative resistances: R_N, directly proportional to frequency, and R_N^* has an inverse relationship with frequency.***

If we display the memristor behavior on an I–V graph, a hysteresis loop is obtained, as opposed to a 1 : 1 relationship between the variables produced by a Φ–q graph. Similar arguments regarding their memory behavior and a unique link between two circuit variables indicates that the meminductor and the memcapacitor can also be considered fundamental elements. Hence, it may be argued that the memristor begins a subclass of memristive systems [9] based on the integrals of the appropriate circuit variables. Basically, as shown in Fig. 1, $\int_t i$–$\int_t V$, $\int_t i$–$\int_t \Phi$, and $\int_t V$–$\int_t q$ relationships can be considered as second generation of circuit elements.

The reader is referred to Appendixes A–D for further detail on understanding how a fourth fundamental element can be seen from the quasi-static expansion of Maxwell's equations. For the first time, we show how this insight can be gained in a clearer way by exploiting a unified form of Maxwell's equations based on geometric algebra (GA) in Appendix D-2.

III. MEMRISTOR MODELING AND CHARACTERIZATION

In this section, we are primarily concerned with the development of simple models that will assist us in the understanding of circuits and system behavior providing the basis whereby system performance, in terms of signal

delays and power dissipation, can be estimated. Here, we develop analytic and empirical models that describe the switching characteristics of a memristor.

Strukov *et al.* [2] introduced a physical model whereby the memristor is characterized by an equivalent time-dependent resistor whose value at a time t is linearly proportional to the quantity of charge q that has passed through it. This proof-of-concept implementation, which consists of a thin nanolayer (2 nm) of TiO_2 and a second oxygen deficient nanolayer of TiO_{2-x} (3 nm) sandwiched between two Pt nanowires, is shown schematically in Fig. 2. The oxygen vacancies are positively charged mobile carriers. A change in distribution of the vacancies within the nanolayer changes the resistance by a tunneling mechanism through the TiO_2 layer to Pt [10].

The device conductance then will change by applying either a positive or negative voltage. As shown in Fig. 2, by considering tunneling as the dominant physical mechanism [11], l introduces the initial tunneling barrier width, which is bounded with two maximum $(x_{\max})$ and minimum $(x_{\min})$ possible positions, while x indicates the position of the tunnel barrier. The initial barrier width $l = x_{\max} - x_{\min}$, where $x_{\max}$ and $x_{\min}$ are the maximum and minimum of the state index position. As an example, based on the HP measurement [10], when $x_{\max} = 19$ Å and $x_{\min} = 11$ Å, the initial tunneling barrier width in the TiO_2 layer is 8 Å. In order to promote consistency between the first description of the fabricated memristor and the tunneling concept we assign the memristor state as a normalized variable. The approach results in a normalized parameter that indicates the internal memristor state $w = (x_{\max} - x)/l$. The barrier position can move from $x_{\text{off}} = 18$ Å ("OFF" state) down to $x_{\text{on}} = 12$ Å ("ON" state). This results in 0.12 and 0.88 boundaries of the normalized state variable w for "OFF" and "ON" switchings, respectively. Interestingly, this piece of the puzzle confers a physical interpretation upon the position of the normalized state variable published in [12], leading to the expected current limits for a 10-nm-thin $SrTiO_3$/Pt device.

Application of Ohm's law to Fig. 2(c) results in $V = (R_S + R_V)i$. If θ is the resistivity of the TiO_2 region and A is the contact area, then $R_V = (\theta/A)(x_{max} - x)$, from which we obtain $dx/dt = -(A/\theta)(dR_V/dt)$. Thus, $dx/dt = (A/\theta G_V^2)(dG_V/dt)$, where G_V illustrates the variable conductance. In other words, the rate of change in the device conductance is a strong function of the rate of change in the position of the barrier and initial conductance. Therefore, a memristor can be treated as a finite state machine. If a uniform distribution of particles and applied electric field (uniform applied force on each particle) is assumed, a factor called the *conductance modulation index* [13] can be shown to follow from the very first HP memristor model.

The very first step is to prepare a SPICE-like model that can mimic the behavior of a memristive device. A memristor structure is created by forming a Pt/TiO_2–TiO_{2-x}/Pt layers. Each layer and the boundary display a particular behavior that is fundamental in estimating the performance of a circuits or a system. There are a number of approaches that aim to model the memristor behavior.

Kavehei *et al.* [13] introduced a *resistance modulation index* (ρ_M) term, which is based on the memristor OFF and ON resistance ratio $r = R_{\text{off}}/R_{\text{on}}$ and the integral of applied voltage $\phi(t) = \int V(t)dt$. The ρ_M factor can be described as

$$\rho_M = \sqrt{1 - \frac{2c(t)}{r}} \tag{1}$$

where $c(t) = \Phi(t)/\kappa$, $\Phi(t)$ is the magnetic flux, $\kappa = D^2/\mu_D$ having the dimensions of magnetic flux $\Phi(t)$, μ_D is the average drift mobility with unit of $m^2s^{-1}V^{-1}$ and D is the film thickness. Fig. 3 illustrates the response of a memristive device model using ρ_M to characterize the modulation mechanism, where the current/voltage relationship is described by $i_M = V_M/(\rho_M R_{\text{off}})$. This definition is derived from HP's experimental data [2], which is based on geometrical and physical parameters. Therefore, it can be inferred that there is a strong relationship between the

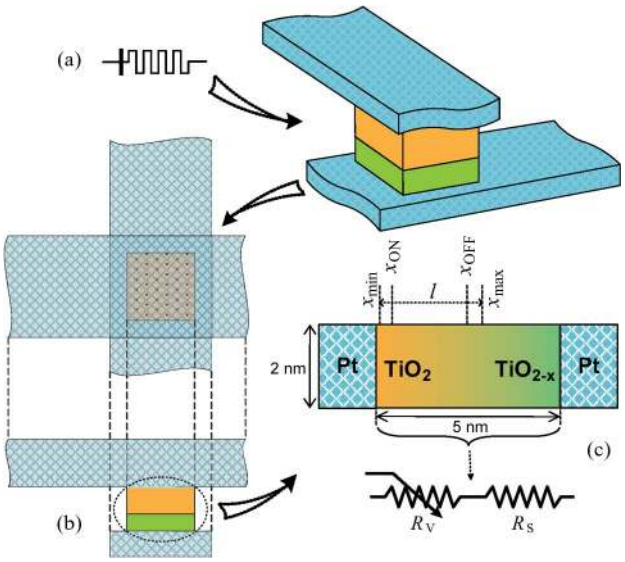


Fig. 2. ***Physical representation of memristor switching. (a) Memristor symbol and a 3-D view of the Pt/TiO_2/Pt structure. (b) Top and side cross sections of the structure. (c) Switching behavior of the memristor, whereby "doped" and "undoped" regions correspond to R_{on} and R_{off}, respectively, being the two extreme states for the variable resistance R_V. Here, R_S is a series resistor around 200 Ω [10]. The dopant consists of mobile charges. Assuming the tunneling [11], l introduces the initial (maximum) tunneling barrier width, bounded by two extremes $(x_{\max})$ and minimum $(x_{\min})$ possible positions, x indicates the position of the tunneling barrier. As an example, with $x_{\max} = 19$ Å and $x_{\min} = 11$ Å, we have $l = 8$ Å. At the same time, x_{off} and x_{on} are 18 Å and 12 Å, respectively.***

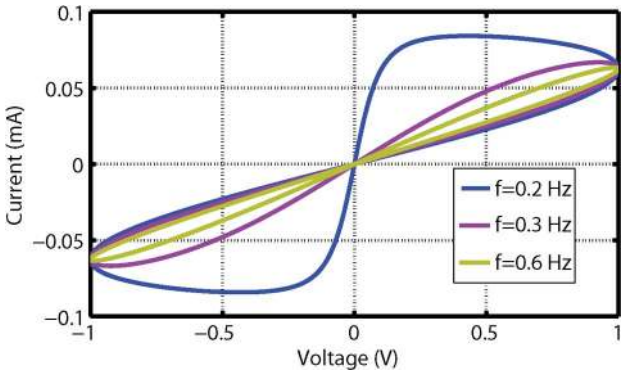


Fig. 3. *The I–V characteristic of an ideal memristor based on the HP modeling approach and using the resistance modulation index ρ_M. Three curves show the hysteresis behavior at three different frequencies: 0.2, 0.3, and 0.6 Hz [2]. The change in the device conductance σ_M can be expressed as $\sigma_M = 1/\rho_M$, which corresponds to the conduction modulation factor. The rate of this change is usually described as the rate of change in an internal (normalized/unnormalized) state variable w.*

resistance/conductance modulation factor ($\propto \sqrt{V}$) and the memristor dynamics.

A. Progression of Memristor Modeling

Available memristor or memristive device models attempt to characterize both current/voltage behavior and the device dynamics. A number of memristor models have been introduced [10], [14]–[18]. However, only a few address the highly nonlinear nature of the device. It would be useful to review the more successful models thus far. The "normalized" dynamics of a memristive device can be described as the rate of change in the position of state variable w, which over time can be written as

$$\frac{dw}{dt} = h(w, X_M) \tag{2}$$

where $h(\cdot)$ is a function of the state variable. Either memristor current (i_M) or voltage (V_M) facilitates rate of change in the device resistance/conductance (memristance/memductance) [1], [9]. A simplified and practical example of a memristor model is $h(w, i_M) = \alpha \cdot i_M$, where α is a constant that depends on device parameters such as the device thickness, carrier mobility, and initial resistance [2], hence, the memristor device dynamic is linearly related to i_M.

Available models apply a number of techniques to describe the nonlinear dynamics of the memristor device. These approaches can be simplified in the form of

$$\frac{dw}{dt} = \alpha \cdot f(w) \cdot i_M \tag{3}$$

where $f(w)$ is a normalized nonlinear function of the form $1 - (2w - 1)^{2p}$, commonly referred to as a *window function*, where p is a positive constant [14].

The limitation in adopting the window function is its boundary conditions [19] whereby one has to ensure that there is little or no change in the memristance when w approaches the boundaries (0, 1 states for normalized w), $f(w \rightarrow \text{boundaries}) \approx 0$. This condition implies an infinite state at the boundaries, identified as a *hard switching* condition in [2] and [15]. The second problem with using such a window function is that highly nonlinear behavior obtained at high values of p changes the exponential nature of the reported relationship [10], [20], with the direct relation that exists between the dw/dt and $f(w)$. It deploys the same behavior pattern for both $0 \rightleftharpoons 1$ transitions, which may not be the case based on recent experimental results for ON and OFF switchings [21]. The nonlinearity created by the window function does not appear to comply with presently known physical phenomena. These asymmetries between ON and OFF switching speeds and also the rate of the state variable change toward ON and OFF imply an exponential relationship between initial conductance level and the rate of conductance change [21]. These limitations are identified with other types of window functions, such as $1 - (w - \text{stp}(-i_M))^{2p}$ [15], where the $\text{stp}(\cdot)$ function can be either 0 or 1 depending on the current signature $\text{stp}(z) = 1$ if $z \geq 0$, otherwise $\text{stp}(z) = 0$. As a consequence, these models continue to have some limitations in modeling the device as they do not allow for a consistent prediction of the memristor behavior when compared with experimental results. Additionally, a $\sinh(\sqrt{V})$-like behavior has been observed between the rate of change differential conductance and the applied voltage at low electric field relative to the tunneling barrier width [21].

Generally, the common problem in these models is that there is no threshold consideration, so there is a gap in knowledge base for design characterization. Nonetheless, the models [2], [14], and [15] confirm the behavior of HP's memristor. However, Lehtonen and Laiho [17] introduced a new model using the window function of (3). The main advantage of this model is that it provides a programming threshold by using a nonlinear function $g(\cdot)$, which is a function of the applied voltage V. The model is described by

$$\frac{dw}{dt} = \alpha \cdot f(w) \cdot g(V). \tag{4}$$

They concluded that to mimic the behavior of the memristor reported in [22], the $g(\cdot)$ term must be a nonlinear, odd, and monotonically increasing function. Considering the basic memristor properties discussed in [1] and [9], the memristor experimental data, and some of the mathematical approaches from the literature [23], [24],

these features must be met in any memristive device modeling.

Several options are possible, such as $g(V) = V^{2j-1}$, where j is a positive constant, and $g(V) = c_a \cdot \sinh(c_b \cdot V)$, where c_a and c_b are two constants that depend on device characteristics and experimental results, comparable to that in [22]. Applying a highly nonlinear $g(\cdot)$ automatically yields a programming threshold voltage. However, applying this nonlinearity has never been linked to a physical phenomenon in the modeling context. It is important to note that the models show similar speed for ON and OFF switchings, which seems to be not the case based on experiments reported in [10].

Another model introduced by Linares-Barranco and Serrano-Gotarredona [24] is

$$h(w, V_M) = \begin{cases} A \cdot \text{sign}(V_M)\left(e^{\frac{|V_M|}{V_0}} - e^{\frac{V_t}{V_0}}\right), & |V_M| > V_t \\ 0, & \text{otherwise} \end{cases} \quad (5)$$

where $\text{sign}(\cdot)$ is the signum function and the A and V_0 parameters can be dependent on, or independent of the normalized state variable w. This model describes the ideal behavior of a memristor in its OFF mode by taking $dw/dt = 0$ for an applied voltage that is less than the threshold V_t. This, however, is not a realistic condition as the memristor state can change, if $V_M \leq V_t$ is retained for sufficient time [21].

A piecewise modeling approach was reported in [23]. The reported function is interesting because it is directly a strong function of the rate of change in memristor's resistance (memristance M) dM/dt, which is the approach that we have taken in introducing our proposed model.

B. Proposed Model for Memristor Dynamic Behavior

The conduction mechanism of MIM structures is based on tunneling [22], [25]–[27]. Simmons [6] introduced a model that describes the I–V characteristics of MIM structures, based on the Simmons tunneling theory. In the modeled device, depicted in Fig. 4, the conductance G is shown as a function of the barrier width based on the Simmons theory that is in agreement with the experimental results reported by [25]. The conductance model is described by

$$G = \frac{q^2}{4\pi h}\frac{A}{L^2}(\rho\varphi_0 - 2)e^{(-\rho\varphi_0)} \quad (6)$$

where q is the electron charge, h is Planck's constant, φ_0 is the equilibrium ($V \equiv 0$) barrier height in eV, ρ is the equilibrium shape factor in eV^{-1}, A is the contact area in μm^2, and L is the energy barrier width [28]. The barrier width L can be taken as a function of the state variable x,

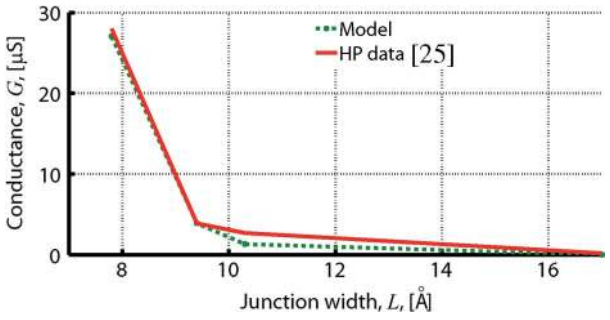


Fig. 4. *Device conductance G in μSiemens (μmho), as a function of junction width L in Angstroms. A highly nonlinear change in conductance of the device can be observed based on the Simmons theory of tunneling [see (6)], which confirms the experimental results shown in [25].*

$L = x - x_{\min}$, where $x \in [x_{\text{on}}, x_{\text{off}}]$, or as a function of the normalized state variable w, $L = l(1 - w)$, where $w \in (0, 1)$. The shape factor parameter can be related to L using $\rho \equiv \beta_0 L/\varphi_0$, where β_0 is the tunneling constant (decay parameter) in Å^{-1}, which presents in the form of normalized state variable $w = 1 - (x - x_{\min})/l$. The resistance of such devices as a function of w illustrates an exponential behavior as depicted by $R \propto e^{(1-w)}$ [29].

This approach leads to a more in-depth understanding of the underlying mechanism of the memristor dynamics. Furthermore, the $\sinh(\sqrt{V})$-like behavior and the complexity of the available model, in [10], motivates us to explore different possibilities. The exponential form of the conductance in (6) is consistent with the behavior of characteristics of a modified Simmons relation in [28]. Therefore, we apply a new $g(\cdot)$ function as follows:

$$\begin{aligned} &g(V, \rho(w), \varphi_0) \\ &= \left(1 - \frac{V}{2\varphi_0}\right)\exp\left(\rho(w)\varphi_0\left(1 - \sqrt{1 - \frac{V}{2\varphi_0}}\right)\right) \\ &\quad - \left(1 + \frac{V}{2\varphi_0}\right)\exp\left(\rho(w)\varphi_0\left(1 - \sqrt{1 + \frac{V}{2\varphi_0}}\right)\right). \end{aligned} \quad (7)$$

The core part[1] of (7) is based on the assumption that in an asymmetric trapezoidal barrier, the averaged potential $\bar{\psi}(V) = (\psi_{\text{left}} + \psi_{\text{right}})/2 = \psi_0 + V/2$, there is an asymmetry between the barrier heights at the left and right ends of the barrier. However, such asymmetry can be ignored when the applied bias is less than the maximum barrier heights [28]. Equation (7) describes the behavior based on two exponentials for ON and OFF switchings similar to that reported by HP in [10]. From (6), we have that the effective barrier width L is proportional to $1 - w$. Therefore,

[1]Similarity of the term $\sqrt{1 - (V/2\varphi_0)}$ when compared with (1) highlights the relationship of modulation index in characterization of the memristor dynamics.

Table 1 SPICE Subcircuit of a Memristor

```
.SUBCKT memristor Pos Neg PARAM:
* Parameters:
n=4 a1=9 a2=0.01 b1=2 b2=4 l=10n
wmin=0.05 wmax=0.95 p0=1.2 fon=40E-3 foff=40E-3
* Shape factor, sf, can be a function of tunneling barrier width (normalized state variable)
sfo=4 sfm=20 p=5 *** sf(w)=sfo+sfm(1-(2w-1)**2p)
*State variable:
Gvon 0 w value = signm(wmax-V(w))*signm(V(Pos,Neg))*gon(V(Pos,Neg),sf(V(w)),p0)
Gvoff 0 w value = signm(V(w)-wmin)*signm(V(Neg,Pos))*goff(V(Pos,Neg),sf(V(w)),p0)
* Initial (internal) state:
.IC V(w) 0.5
*Integration:
Cw w 0 8e-5
Rw w 0 0.01T
*Current equation:
Gmem Pos Neg value = l*((V(w)**n)*a1*sinh(b1*V(Pos,Neg))+a2*(exp(b2*V(Pos,Neg))-1))
* Series resistor, RS, can be implemented here, between two Neg1 and Neg2 nodes.
*Functions:
.func signm(v) = (sgn(v)+1)/2
.func gon(v1,v2,v3) = fon*((1-v1/(2*v3))*exp(v2*v3*(1-sqrt((1-v1/(2*v3))))))
.func goff(v1,v2,v3) = foff*(-((1+v1/(2*v3))*exp(v2*v3*(1-sqrt((1+v1/(2*v3)))))))
.func sf(v1)=sfo+sfm(1-(2*(v1)-1)**2p)
.ENDS memristor
```

if $w \to 0$, an OFF device results, whereas if $w \to 1$, an ON switch results. Thus, the two exponential parts charge and discharge a capacitor C in the SPICE model. This capacitor carries out integration process to achieve w. According to Kirchhoff's circuit laws

$$\frac{dw}{dt} = \frac{i_{\text{charge}} - i_{\text{discharge}}}{C} \tag{8}$$

where i_{charge} and $i_{\text{discharge}}$ are the two exponential forms in (7) and in the forms of $G_{V,\text{ON}}$ and $G_{V,\text{OFF}}$ in Table 1.

In this case, there is no need for using a window function $f(w)$ and the rate of change of the state variable dw/dt will be linearly related to the tunneling phenomenon, which appears to be the case for a memristor.[2] Therefore, (4) can be rewritten as

$$\frac{dw}{dt} = \nu \cdot g(V, \rho(w), \varphi_0) \tag{9}$$

where ν is a constant value to identify ON and OFF switching speeds in a normalized distance $(w \in (0,1))$ based on experimental results [10], [20]. It has been observed that ON switching is much faster than OFF switching in a memristive device. The most interesting part of the model is that several thresholds can be programmed by tuning the shape factor, which can also be tuned for a certain range of voltages. It is instructive to note that the $g(V, \rho(w), \varphi_0)$ contains two exponential parts that can be used in symmetric or asymmetric fashion for negative and positive voltages. Fig. 5 illustrates the proposed model response to a 1-MHz sinusoid. The normalized state variable w is limited to a maximum of 0.95 and a minimum of 0.05 and an initial state of 0.95 is assumed. These limits can be modified based on experimental results, where the ON and OFF state limits can be extracted as $w_{\text{on}} = 0.88$ and $w_{\text{off}} = 0.12$, respectively. These limits guarantee that the model operation is always within the memristive regions [18]. Furthermore, there is a threshold around $V_t \equiv \pm 1.7$ V.

Based on the definition, the shape factor parameter ρ linearly depends on the tunneling junction width L. This relationship causes a high nonlinearity in one of the boundaries and low nonlinearity in the other and also the function can be unnormalized. To address this issue and formulate a more robust model, we introduced $\rho(w)$ as a new shape factor function defined as

$$\rho(w) = \delta + \eta\left(1 - (2w-1)^{2p}\right) \tag{10}$$

where δ is an offset (positive) constant and it should be adjusted to retain the monotonically increasing condition

[2]The window function can be used to control the exponential nonlinearities at the boundaries by applying lower values to the shape factor $\rho(w)$ at the boundaries. In fact, the double exponential relationship between the tunneling barrier width and device dynamics equation in [10] can be modeled as a highly nonlinear polynomial equation, introduced by (10).

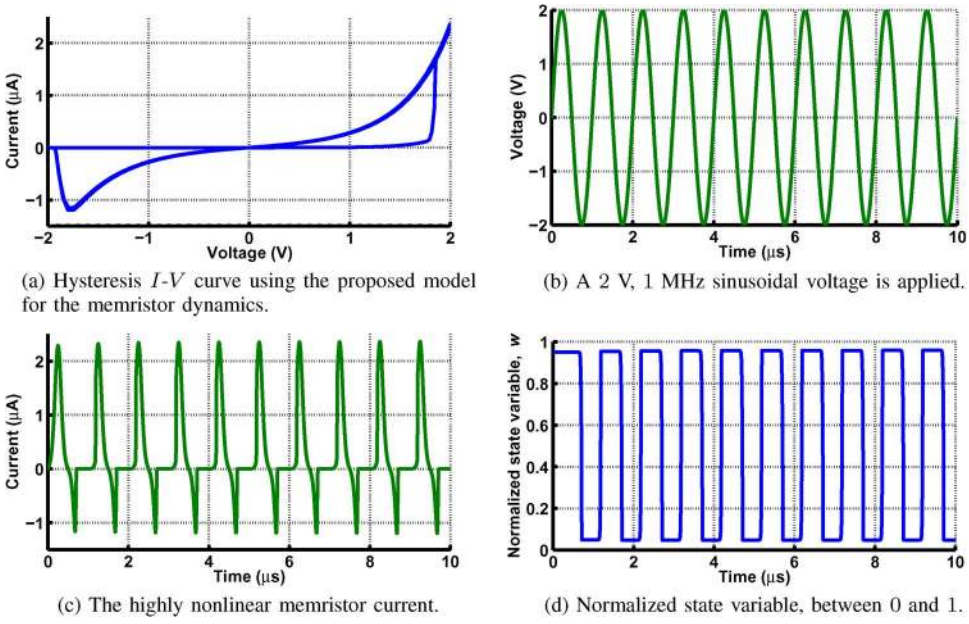


Fig. 5. ***Memristor compact model response to a 1-MHz sinusoid applied voltage. (a) The current/voltage characteristic shows the existence of a threshold voltage around 1.7 V for an applied voltage of 2 V. The plots in (b) and (c) illustrate the applied voltage and memristor current as a function of time. (d) The normalized state variable shows switching between 0 and 1 states. Lower values are closer to the OFF state and higher values indicate a more conductive device. Basically, a memristor in its digital (binary) regime acts as a two-state device with high and low regions for ON and OFF states, respectively.***

for (9), and η is a positive coefficient to control the $\rho(w)$ nonlinearity. The $1-(2w-1)^{2p}$ part is a normalized-nonlinear function, which describes the nonlinear conditions at the boundaries. Introducing this polynomial form in (7) approximates the double exponential form of the velocity equation in [10] though its SPICE implementation is not a robust model and contains convergence and current overflow problems even for simulation of a small-scale array. The SPICE (Mentor Graphics Eldo, PSPICE, or LTSpice) implementation of our model as a subcircuit is shown in Table 1.

The current/voltage relationship, using the model introduced by Yang *et al.* [22], can now be described by

$$i_M = w^n \sinh(\vartheta V_M) + \chi\left(e^{(\gamma V_M)} - 1\right) \tag{11}$$

where and ϑ are fitting parameters for characterizing the ON state, which is essentially based on electron tunneling through a barrier (supplementary information [22]). In the second term, χ and γ are used as fitting parameters to characterize net electronic barrier for the OFF state. Using the proposed model for the state variable it confirms that w is proportional to the history of applied voltage, which is equivalent to the magnetic flux from Faraday's law. The first term of (11) is controlled by the exponent n. Therefore, the nonlinearity between the drift velocity and the ON switching current can be controlled by applying n as a fitting parameter. It can be concluded that the first modeling approach introduced by Strukov *et al.* [2] is a special case of this particular relationship where $n = 1$. Fig. 6 demonstrates the difference between the two current curvatures, for $n = 1$ (linear HP model) and $n = 4$ (used for this work).

A possible way of characterizing a memristive I–V curve is to plot the relationship on a log–log scale. Using this approach, the curve will yield two functional (fitting)

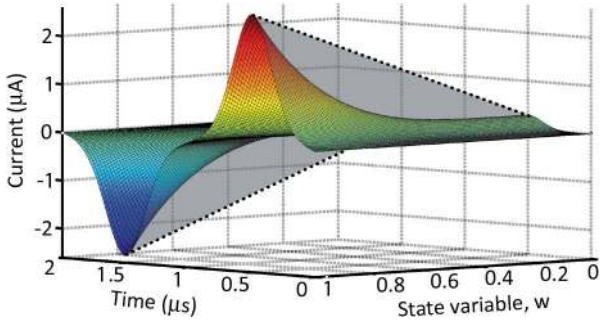


Fig. 6. ***The memristor current i_M in (11) as a function of time and normalized state variable w in response to a sine input voltage. The grayscale curve, which curvature is highlighted by a dashed line, shows how (11) can mimic the linearity of the model proposed in [2] by applying $n = 1$. The colored curve, however, illustrates a highly nonlinear behavior of this current when $n = 4$.***

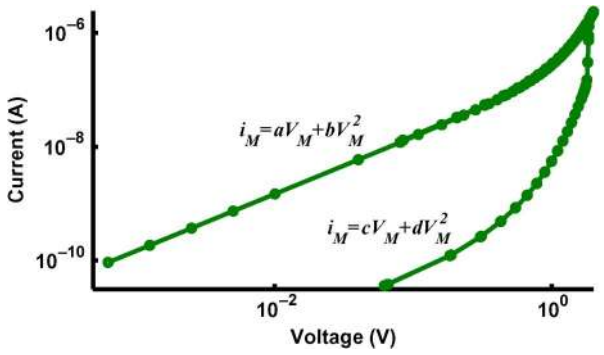


Fig. 7. ***The memristor I–V curve on a log–log scale linearizes the current as a function of applied voltage. The current/voltage relationship can be rewritten as a polynomial function*** $i_M = k_1 V_M + k_2 V_M^2$, ***where*** x_1 ***and*** x_2 ***are fitting parameters. Switching occurs when the memristor current is highly nonlinear, i.e., at the boundaries highly nonlinear behavior is observed [14].***

parameters a (c) and b (d). Basically, this can be considered as another signature of high nonlinearity at the boundaries and one way to characterize different implementations of memristors. Fig. 7 depicts an I–V curve on its log–log scale [30].

1) Comparison of Models: Table 2 summarizes the comparison between different available models. These models, which provide the threshold programming and/or SPICE-like model, are [10] (with SPICE implementation in [31]), [13], [17], [18], [33], and this work. Our proposed model is the only approach that addresses the issue of programming threshold, SPICE-friendly approach, adaptation of Simmons theory of tunneling, and the memristive operation regime limits. SPICE implementation of model [10] in [31] needs extensive and detail adjustments for the applied signal, including detailed rise time tuning; otherwise, the model does not provide convergence in simulation and practically fails when running a large-scale simulation. Thus, the model in [31] mainly suffers from convergence and current overflow problems in SPICE implementation form. Our approach, therefore, significantly improves simulation robustness in terms of convergence and overflows for i_{charge} and $i_{\text{discharge}}$. Note that the modeling approach herein can be extended to memcapacitor and meminductor [8] modeling along similar lines to Biolek *et al.* [32].

IV. CIRCUITS AND SYSTEMS APPLICATION

One of the key applications of a *digital memristor* is memory. Combining this capability with its two-state resistance for ON (low resistance) and OFF states (high resistance) may enable future associative memory/processor architectures.

Table 2 Progression in the Development of Memristive Device Modeling

Models	State variable	$f(\cdot)$	I-V	Ⓥ	Ⓢ	Ⓣ
Strukov et al. [2]	$\alpha \cdot i_{\text{M}}$ and $\alpha \cdot f_H(w) \cdot i_{\text{M}}$	$w(1-w)$	$V_{\text{M}}/M(q_{\text{M}})$	-	-	-
Kavehei et al. [13]	$\alpha \cdot f_{\text{H}}(w) \cdot i_{\text{M}}$			-	+	-
Joglekar and Wolf [14]	$\alpha \cdot f_{\text{J}}(w) \cdot i_{\text{M}}$	$1-(2w-1)^{2p}$		-	-	-
Biolek et al. [33]	$\alpha \cdot f_{\text{B}}(w) \cdot i_{\text{M}}$	$1-(w-\text{stp}(-i_{\text{M}}))^{2p}$		-	+	-
Shin et al. [18]	$\alpha \cdot i_{\text{M}}$ and $\alpha \cdot f_S(w_q) \cdot i_{\text{M}}$	$\delta + 1-(2w_q-1)^{2p}$		-	+	-
Strukov and Williams [20]	$\mu_v E_0 \cdot \sinh(\frac{E}{E_0})$	-	-	+	-	-
Pickett et al. [10]	$\upsilon \cdot \sinh(\zeta) \cdot e^{-e^{(\pm\omega_a-\zeta_b)}-\omega_c}$	-	Supplementary material in [10]	+	+	+
Linares-Barranco and Serrano-Gotarredona [24]	$A \cdot \text{sign}(V_{\text{M}})\left(e^{\frac{\lvert V_{\text{M}}\rvert}{V_0}} - e^{\frac{V_t}{V_0}}\right)$: $\lvert V_{\text{M}}\rvert > V_t$ 0 : otherwise	-	$V_{\text{M}}/M(q_{\text{M}})$	+	-	-
Lehtonen and Laiho [17]	$\alpha \cdot f_{\text{J}}(w) \cdot V^{2j-1}$ $\alpha \cdot f_{\text{J}}(w) \cdot \sinh(c_b V)$	$1-(2w-1)^{2p}$	$i_M = w^n \delta \sinh(\vartheta V_M) + \chi(e^{(\gamma V_M)}-1)$	+	+	-
This work	$\nu \cdot g(V, \rho(w), \varphi_0)$	-		+	+	+

Key: Ⓥ Programming threshold Ⓢ SPICE-like Ⓣ Adaptation of tunneling phenomena

Comments: (1) Trimming is another important factor in comparing the models. Basically, a model without limits for the state variable may introduce complexity with convergence in SPICE-like simulators and furthermore the modeled device most likely will violate the boundary conditions [18]. Only four of the models, [10, 17, 18], and this work address this issue. (2) The state variable memristor equation [20] is equal to $\vartheta \cdot \exp(-\frac{U_A}{qV_0}) \cdot \sinh(\frac{gE}{2V_0})$, where ϑ is velocity, U_A is activation energy, V_0 is thermal voltage, and E is electric field. The E_0 in the equation indicates a point between linear and nonlinear electric field and μ_v shows the mobility. This nonlinearity can be large, it is stated that a 20 orders of magnitude of change in the drift velocity for a small change in the applied electric field [20]. In [10] two equations in the form of $\upsilon \cdot \sinh(\zeta) \cdot \exp(-\exp(\pm\omega_a - \zeta_b) - \omega_c)$ is defined to separately explain the OFF and ON switching behavior. In these equations, υ is ON or OFF switching velocity, ζ and ζ_b are dimensionless parameters depends on i_{M}, and ω_a and ω_c are dimensionless parameters based on the device state variable, x, and ON and OFF limits, x_{on} and x_{off}. Its SPICE implementation can be found in [31], which is very sensitive to the applied voltage in terms of convergence and current overflow errors. (3) In the Shin et al. [18] model, δ is a positive constant ($\delta \ll 1$), and w_q is a normalized memristive charge. (4) The $\sinh(\cdot)$ part of the equation cannot be found in [17]; however, it is published online and appears to be an improvement over the use of V^{13}.

Low-power and nonvolatile content addressable memories (CAMs) are also promising applications. Note that CAM-based search engines are well known for their speed advantage over their software counterparts. The significance of CAMs is in search-intensive applications such as translation lookaside buffers (TLB), image coding [34], artificial neural networks, and classifiers to forward Internet protocol (IP) packets in network routers [35]. The energy requirement, however, is a major challenge in present-day high capacity CAMs and many other ultrahigh capacity memories including flash memory structures [36]. Many techniques have been used to reduce power dissipation, but despite all the efforts power consumption is still high [37].

1) MCAM Implementation: Here, we introduce a new (nonvolatile) memristor-based CAM structure, in order to improve the area-power-speed tradeoff. The benchmark CAM architecture is designed and simulated based on an $N\times$ 144-bit structure [35], where N is the number of rows shown in Fig. 9(a), which shows a modified version of a conventional CAM architecture with N rows and 144 cells per match line (ML). For simplicity, the search line (SS) and the word line (WS) are not shown in the figure. The control line (V_L) is an additional interconnection shared between columns. The addition of this interconnection is compensated by the use of the shared search and data lines $(D/\overline{D})$. The MCAM cell, shown in Fig. 9(b), is based on the memristor-MOS (M^2) approach. The implementation consists of seven transistors and two memristors (7T2M) that facilitate a complete set of write and search operations, in a 25-μm^2 area, since the design consists of only n-type transistors, and there is no supply voltage (V_{DD}) connection.

The SPICE-like model illustrated by Table 1 is used to simulate a row of 144 cells for both the "match" and "miss" conditions. Fig. 9(a) shows the circuit for match-line sense amplifier (MLSA). Simulations are based on 0.13-μm technology mixed signal device model (Dongbu HiTek) with 1.2 V as nominal supply voltage. Methods of READ and WRITE in an array of memristive devices and related information can be found in [38].

A basic MCAM cell is introduced in Fig. 9(b). The cell implements an exclusive-OR function implying that, if data (D) and the stored bit in the left-hand side memristor (W_L) are matched, the ML is not discharged from its precharged state. Therefore, if there is a mismatch between the applied bit stream and stored data in a row, the output of the match-line sense amplifier (MLSA) returns to "0" state, otherwise, the input bit stream and stored data are matched.

2) Write Operation: To carry out the write process, first the input bit stream is applied to D and $\overline{D}$. Then, the write enable line (WS) and the common memristors bias line (V_L) are enabled [19]. The main problem is that the write operation is slower within the context of high-speed

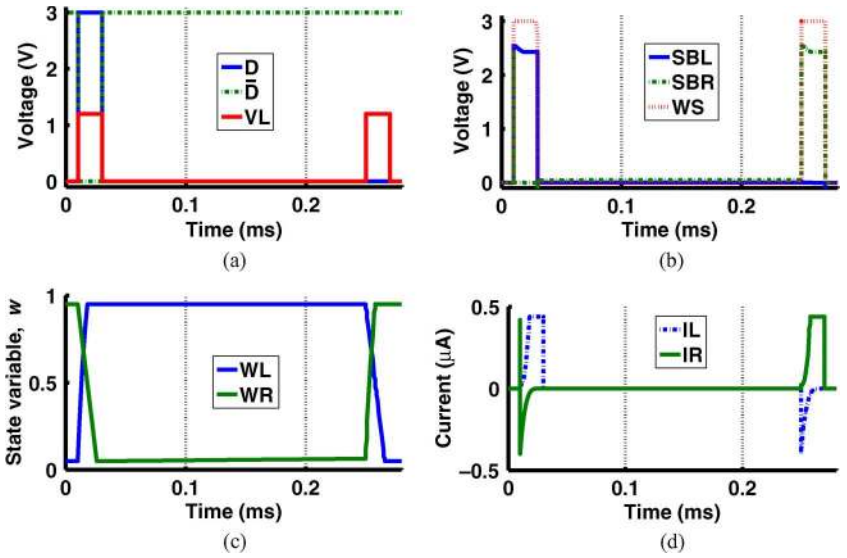


Fig. 8. *Write operation signaling. To carry out a write operation, first the data should be available on the data lines. Then, we apply V_L signal to control the bias across the memristors. Obviously, a voltage threshold drop on either of the write select transistors $N_{WSL/R}$, in Fig. 9(b), reduces the effective applied voltage across either of the memristors, depending on the applied data. For example, considering a threshold voltage around 0.27 V for nMOS transistors from the transistor model used for simulations, a $V_L \approx 1.2$ V can guarantee almost similar voltage difference for ON and OFF switchings [10]. Note that the V_L signal value can also be adjusted for different ON and OFF switching speeds. The red V_L signal in (a) indicates writing attempts. Here two successive write operations are happening. A significant delay of 20 μs can be observed, which is frequently reported as one of the problems in using these devices instead of conventional SRAMs or flash memories. (a) Write data D and its complement $\overline{D}$ and the memristor bias control signal V_L. (b) Write select (WS) and the intermediate node voltages (SBL and SBR). (c) Memristor state variables. (d) Current passing through the left (IL) and right (IR) memristors.*

applications. Using high programming voltages/currents it becomes possible to speed up the write process. Here, we apply a 3.0-V bias to the D and $\overline{D}$ lines for writing "1" and "0," respectively. The common bias line, however, has almost half the programming voltage to create enough positive and negative bias across both memristors to write either "1" or "0" logic. Fig. 8(a) and (b) illustrates the control voltages for writing "1" and "0." The reason that we apply $V_L = 1.2$ V is for writing "1" ("0") as there is an nMOS threshold voltage drop of $N_{\mathrm{WSL}}(N_{\mathrm{WSR}})$ transistor on $\mathrm{SB}_L(\mathrm{SB}_R)$ node. Fig. 8(b) shows the SB_L and SB_R node voltages. The first step is to write a "1" in the left-hand side memristor (W_L). Fig. 8(c) shows that the sequence successfully writes "1" in W_L and "0" in W_R. The second part of this process is to write "0" in W_L, as illustrated in the figure. In this case, we assume that writing "1" and "0" can be carried out with similar speeds. Thus, ν in (9) is equal for ON and OFF switchings. Fig. 8(d) illustrates the current passed through each memristor I_L for W_L and I_R for W_R. The energy consumption analysis of the refreshing process for a row of 144 cells shows an average of 90.6 fJ/b/refresh cycle. Considering a 125-MHz search frequency, which results from a worst case access time analysis, the refresh operation can be carried out after 125 access events and the energy consumption of a refresh operation is 0.73 fJ/b/search.

3) Search: In contrast to the write operation, the search is fast. Since the read from a memristor or memristive device will change the position of the state variable (tunneling barrier width), which depends on the magnitude of the applied voltage/current and time. It is reasonable to apply a positive voltage to carry out the read operation and then continue with application of a negative pulse with the same amplitude and pulse width. The entire cycle can be achieved within time frame of the order of nanoseconds. The worst case access time analysis for an ML [Fig. 9(b)] transition from a precharged status to lower level voltages is to have only one mismatched bit in a row. This means there is only one of the N_{ML} transistors in its ON state to discharge the load capacitor (C_{Load}). Here the search process offers an acceptable speed of 8 ns in comparison to available conventional CAM designs [37] or its magnetoresistive counterpart [39]. The access time will increase by connecting more bit line (D) (adding more rows).

The worst case power analysis needs to be carried out by assuming a worst case match. In this case, all the 144 cells are mismatched. The energy consumption is 0.7 fJ/b/search considering MLSA and bit/data-line drivers. Worst case sensing current through a memristive device is 0.58 μA. Fig. 9(c) illustrates a simplified MCAM cell with a search configuration. If we assume that $W_R(W_L)$ has been already programmed to its low (high) resistance value, $R_{\mathrm{on}}(R_{\mathrm{off}})$. Therefore, the time constant for charging the gate capacitance of the N_{SBL} transistor is almost r times more than the time constant for the N_{SBR} where $r = R_{\mathrm{off}}/R_{\mathrm{on}}$. Consequently, applying a voltage for a

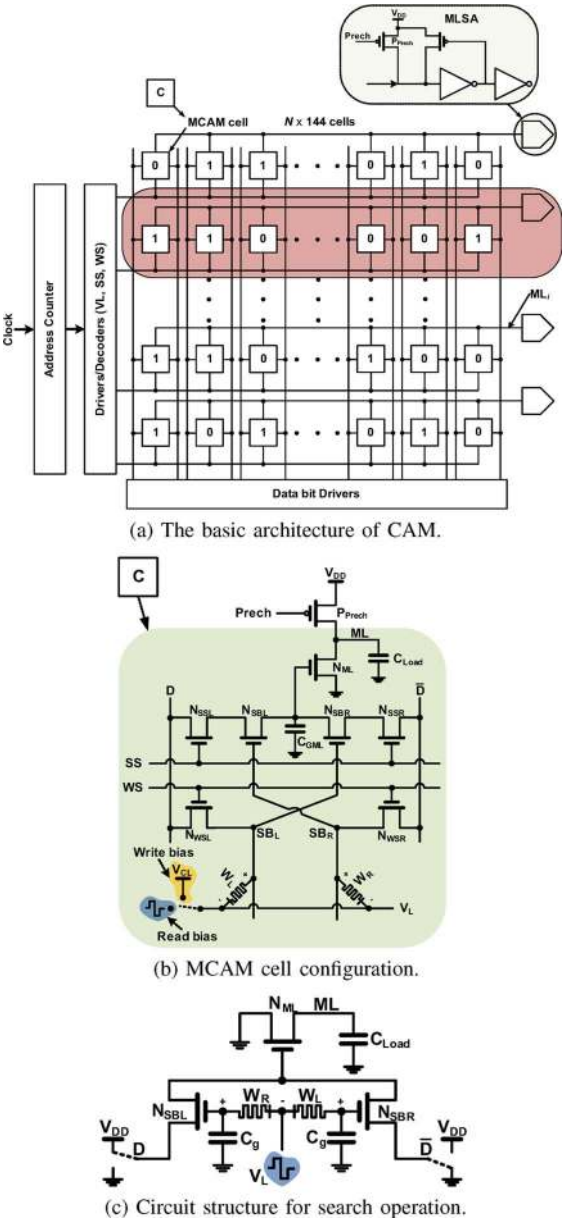
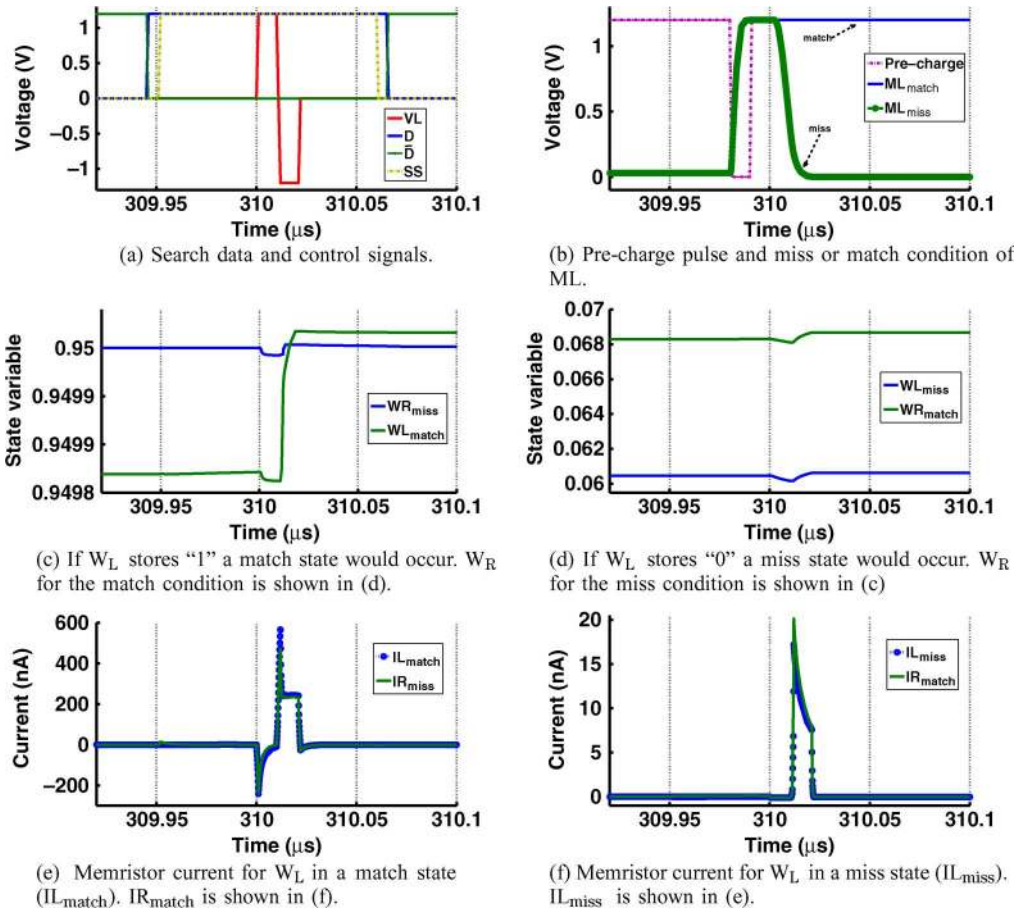


Fig. 9. ***The MCAM architecture and cell configuration. The CAM architecture in (a) illustrates a simplified CAM structure. Each MCAM cell contains seven transistors and two memristors. Memristors store complementary bits. The left memristor W_L stores data and W_R contains complementary data. The write and search operations are controlled by WS and SS signals, respectively. For simplification, these two signals are not shown in the CAM architecture (a). The write bias voltage V_{CL} and read bias are connected to the negative pole of the memristors. The parasitic load capacitor C_{Load} and the parasitic gate capacitor of the ML transistor (N_{ML}), C_{GML}, as well as the precharge transistor P_{Prech} help to understand the basic operation of the MCAM cell. The simplified structure in (c) describes an exclusive-OR behavior between the stored data W_L and the search data D. Basically, the time constant in charging the gate capacitors (C_g) of the N_{SBL} and N_{SBR} transistors changes by the change in the conductance (memductance) of the W_L and W_R, respectively. (a) The basic architecture of CAM. (b) MCAM cell configuration. (c) Circuit structure for search operation.***



(a) Search data and control signals.

(b) Pre-charge pulse and miss or match condition of ML.

(c) If W_L stores "1" a match state would occur. W_R for the match condition is shown in (d).

(d) If W_L stores "0" a miss state would occur. W_R for the miss condition is shown in (c)

(e) Memristor current for W_L in a match state (IL_{match}). IR_{match} is shown in (f).

(f) Memristor current for W_L in a miss state (IL_{miss}). IL_{miss} is shown in (e).

Fig. 10. ***Search operation signaling. The V_L signal in (a) shows a pulse shape that is applied to the negative poles of the memristors. The reason for using the negative side is to retain the memristor state. Plots (c) and (d) demonstrate that the memristor states are almost stable during the search operation. Another reason that helps this operation to keep the memristors state is a short time process (8 ns) and relatively low applied bias (1.2 V). The simulations are carried out for a 1 × 144 MCAM cells and under the condition that one cell creates the miss or match situation. The power analysis, however, has to be carried out considering all 144 misses in a row. (a) Search data and control signals. (b) Precharge pulse and miss or match condition of ML. (c) If W_L stores "1" a match state would occur. W_R for the match condition is shown in (d). (d) If W_L stores "0" a miss state would occur. W_R for the miss condition is shown in (c). (e) Memristor current for W_L in a match state (I_{match}). IR_{match} is shown in (f). (f) Memristor current for W_L in a miss state (IL_{miss}). IL_{miss} is shown in (e).***

short period of time (τ), which is $\tau \ll \tau_{off}$, where $\tau_{off} = R_{off}C_g$, and $\tau \geq \tau_{on}$, where $\tau_{on} = R_{on}C_g$, can turn the N_{SBL} transistor on. Thus, if the D line is connected to V_{DD} implying a miss condition, since W_R stores the complementary of stored data, the ML will be discharged through N_{ML} transistor, else ML stays in the high state. Fig. 10(a) shows the control signals and data bits. The ML_{match} and ML_{miss} signals in Fig. 10(b) highlight the MLSA output. Fig. 10(c) and (d) illustrates the rate of change in W_L and W_R for both miss and match conditions. Finally, Fig. 10(e) and (f) demonstrates memristive current for both conditions.

A. Analog Characterization

The function of biological synapses in the brain can be likened to the behavior of memristors. This implies that memristor-based systems have the potential to form basic building blocks for neuromorphic analog processors. This implies that developed models must be able to adequately simulate analog behavior. Initialization is the first step in programming an analog memory. The next step is to apply a series of successive positive voltages/current. The shape of the applied signal is not important as far as there is a reasonably good control on the time integral of the applied voltage/current. One of the very basic applications of such an analog memory would be in pattern recognition. In other words, image features, for example, enhanced edge information, can be encoded into a matrix of memristive states as analog data. The analog nature of the state variable helps to implement a fully analog pattern recognition structure. Basically, by using a front-end memristive convolution with analog storage layers, a back-end analog winner-takes all (WTA) layer can be achieved [40]. In this part of the paper, we illustrate the application of the proposed model by mimicking the analog behavior of the memristors.

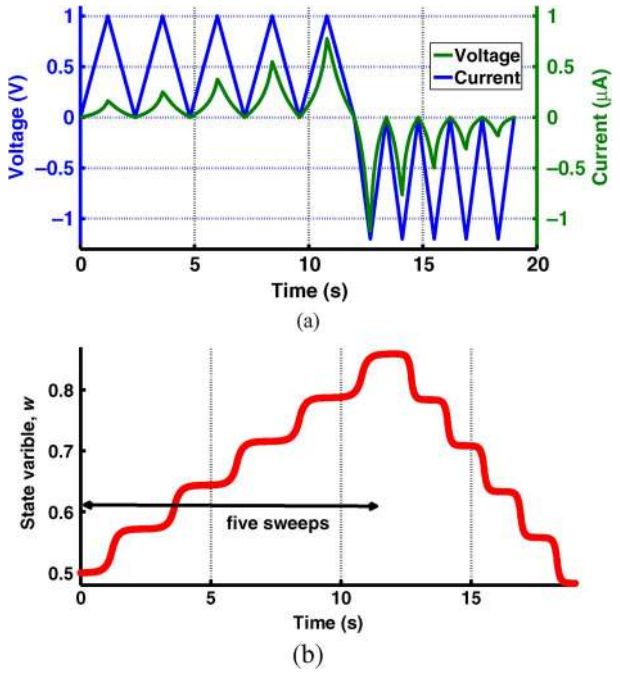


Fig. 11. *Memristor analog response to a number of successive positive and negative triangular voltage pulses. The magnitude of the negative applied voltage is 1.2 V, while the positive voltage is 1 V; this is to adjust the memristor's state to be in the same position as it was before the test. Due to the different speeds and current for* ON *and* OFF *switchings, different voltage values to adjust the memristor state are expected. It is found that due to the nanostructure of the memristor and existence of a high electric field by applying a few hundred millivolts, a large uncertainty in adjusting the memristor's state is expected. The memristor mathematical expression allows us to assume that the connection of two memristors in series can help to minimize the process variation side effects. (a) The current and voltage versus time. (b) Normalized state variable* w *position during the sweeps.*

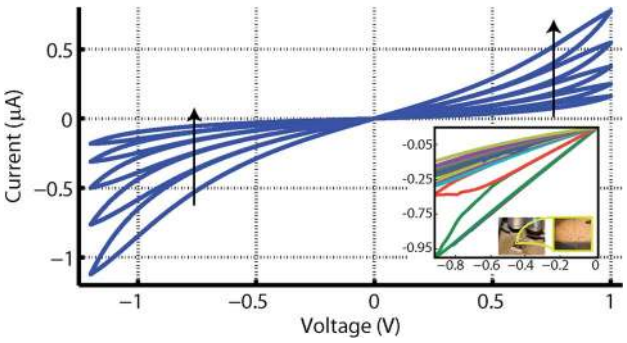


Fig. 12. *The memristor* I–V *curve in its analog regime of operation. Positive hysteresis loops start from* $w = 0.5$ *and by applying a 1-V triangular voltage pulse,* w *changes to 0.58. Successive pulses then change* w *to different values. Here the change in* w *for each positive step is similar. To adjust* w *around 0.5, both applied voltage and the time are different from the positive region. When the last positive voltage pulse is applied, maximum current can be observed since* w *is close to the* ON *state. Negative hysteresis then starts with a high current, which gradually decreases by further application of successive pulses. The existence of multistable memory states is experimentally observed and is shown in the inset figure. The* x*- and* y*-axes in the inset are voltage and normalized current (to a maximum of 35* μ*A), respectively. It clearly shows that the rate of change in the conductance is related to the initial conductance in a nonlinear manner. This is the result measured using a Keithly 4200-SCS and a silver/titanium dioxide/indium tin oxide (Ag/*TiO_2*/ITO) memristor.*

Fig. 11(a) highlights the change in the amount of current that can pass through the memristor after a succession of ten positive and negative voltage sweeps (five each). The magnitude of current can be tuned for a range of microamperes up to a few hundred milliamperes [41]. Fig. 11(b) demonstrates the internal states of a memristive device after applying a couple of positive and negative signals. This characterizes the behavior of *analog memristor*, which can be synonymous with an *analog memory*.

Fig. 12 illustrates the current/voltage behavior of a memristive device in analog regime. A careful characteristic of applied voltage and time, which can be viewed as the time integral of the applied voltage signal, encapsulates information on the memritor/memristive state rather than signal phase, frequency, amplitude, or width. Another advantage of encoding information into the position of the state variable(s) is state variable changes via the integral of the applied signal over time.

V. CONCLUSION

In this paper, we provide a brief insight into memristor fundamentals and physical behavior from which we addressed an overview of modeling approaches being pursued by the design community. We compared features of these models using HP's published TiO_2 platform as the basis of such comparisons. We briefly reviewed options that have been published over the past three decades to motivate reconciliation of some of the unexpected behaviors of MIM thin films such as those encountered in a memristor. We introduced a modeling approach based on tunneling, which includes the concept of programming threshold and SPICE-friendly adaptation. Finally, we presented a system-based case study showing the advantage the memristor confers for MCAM architectures. ■

APPENDIX

A. The Link to Maxwell's Equations

Regarding the very first memristor argument [1], using the quasi-static expansion of Maxwell's equations, proposing a link between the first-order terms in the expansion $\mathbf{D_1}$ and $\mathbf{B_1}$, which are the first-order electric and magnetic flux densities, respectively, we can now identify these elements as connecting dV/dt and di/dt, as shown in Fig. 1. For linear systems, the memristor becomes equivalent to a resistor, and

Table 3 Fundamental Circuit Elements

Physical level	Variables	Element	Field	Property	Relation
1. Electrostatic	q, V	$q = CV$	$\mathbf{E} = -\nabla V$	Capacitance	$V = \frac{1}{C}q$
2. Accelerating charge	$\frac{d^2q}{dt^2} = \frac{di}{dt}$	$\Phi = Li$	$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{dt}$	Inductance	$V = L\frac{d^2q}{dt^2}$
3. Diffusion	$\frac{dq}{dt}$	$V = Ri$	$\mathbf{J} = \frac{i}{A_x} = \sigma \mathbf{E}$	Resistance	$V = R\frac{dq}{dt}$

hence the memristor can be seen as a special case that relates $\mathbf{D_1}$ to $\mathbf{B_1}$.

Beginning from the electrostatic field in conjunction with the relativity principle and Maxwell's equations, we show how the fundamental circuit elements can be derived. Table 3, in fact, can be seen as an underlying motivation to Fig. 1. It was first shown by Einstein that an electrostatic field will register magnetic fields, when viewed by an observer from a relatively moving frame. Hence, the most fundamental aspect of Maxwell's equations is the electrostatic field, defined by the single parameter charge q, creating an electrostatic potential V. However, this is sufficient to define capacitance with the relation $q = CV$. The field can then be found from $\mathbf{E} = -\nabla V$, or we can calculate the field directly from the charge distribution ρ, according to Maxwell's first equation $\nabla \cdot \mathbf{E} = \rho/\epsilon$. We can thus view capacitance as the first fundamental circuit element, shown in Table 3.

For the nonelectrostatic case, we have the magnetic field, which is described by the flux calculated from the inductance L, given by $\Phi = Li$ (Ampère's law, Maxwell's third equation). We have $\Phi = \int V dt = Li = L(dq/dt)$, and hence, differentiating with respect to time, $V = L(d^2q/\,dt^2)$. Thus, α_e and β_e in Fig. 1 increase one unit by the differentiation and this relation therefore presents inductance as the second generation of fundamental circuit element, as shown in Table 3. During steady currents, inductors have no reactance, but alternating current (ac) produces a fluctuating magnetic field in the inductor that according to Faraday's law (Maxwell's second equation) will produce a back emf proportional to $\partial_t B$, as given by $\nabla \times \mathbf{E} = -\partial_t B$, which is shown in the third line of Table 3.

B. Resistance in the Maxwell Picture

Based on Maxwell's equations, the first two fundamental circuit components are lossless. In order to identify the third fundamental element we need to allow energy dissipation. We might expect from the Lorentz force law that charges will accelerate in an electric field because of the relation $\mathbf{F} = q(\mathbf{E} + \mathbf{v} \times \mathbf{B})$. In a dielectric the electrons soon hit terminal velocity, and will drift at a constant velocity v_d. Here, due to the relatively low velocities, we can neglect the magnetic force in circuits. The new law is simply Ohm's law $V = Ri$, where the steady current $i = A_x \sigma \mathbf{E}$, σ is the conductance of the material, and A_x is the cross-sectional area of the element. Hence, we have $V = R(dq/dt)$, linking potential with the first time derivative of charge. Hence, we can consider R as the third fundamental element. Even though resistance depends on Ohm's law and not Maxwell's electromagnetic equations, a steady current can be simulated with a moving reference frame past a static charge and hence from this perspective resistance can be considered fundamental.

C. Questions Surrounding the Fourth Element

From Fig. 1, it can be seen that the memristor completes the square of circuit variables Φ, V, i, q, with a link between Φ and q. Moreover, it may be argued that the concept of memristive systems developed later, which include meminductors and memcapacitors, leads us to classify the memristor as the first new element in a second generation of circuit elements based on the integrals of the circuit variables q, V, i, and Φ.

It appears that there are two threads to Chua's original argument for a memristor: 1) memristor as a basic two-terminal circuit element that establishes a link between charge q and magnetic flux Φ, and 2) a circuit theory perspective, along the line that a memristor in fact links the quantities $\mathbf{D_1}$ and $\mathbf{B_1}$ in the quasi-static expansion of Maxwell's equations. A natural question would be then how these two seemingly distinct approaches to the basic physical principles of a memristor are related to each other. In particular, how can the link between q and Φ be reexpressed in terms of $\mathbf{D_1}$ and $\mathbf{B_1}$ and *vice versa*? Fano *et al.* [42] stated "Quasi-static fields involving both first-order fields fall outside the scope of circuit theory." However, Chua was expecting an element linking the first-order electric and magnetic fields. A possible answer to this conflict is the $\mathbf{D_1}$ and $\mathbf{B_1}$ relation points to a resistive-type component, but lying between the variable pairs $dV/dt, di/dt$ as opposed to the variable pairs Φ, q for HP's memristor. Alternatively, there is also perhaps scope for a new circuit element using Ampère's law (Maxwell's third equation) using the property of a changing electric field related to changing the magnetic field given by $\nabla \times \mathbf{H} - (\partial \mathbf{D}/\partial t) = \mathbf{J}$.

D. Quasi-Static Expansion of Maxwell's Equations

Circuit theory can be treated as a special case of electromagnetic field theory, using the quasi-static expansion of Maxwell's equations [1], [13]. However, in order for the expansion to converge, we require the dimensions of the circuit elements to be smaller than the wavelength of the highest frequency being applied [42]. In the presence of

dielectrics, Maxwell's equations are typically written, in SI units, as

$$\begin{aligned}\nabla \cdot \mathbf{D} &= \rho \quad \text{(Gauss's law)}\\ \nabla \times \mathbf{E} + \frac{\partial \mathbf{B}}{\partial t} &= 0 \quad \text{(Faraday's law)}\\ \nabla \times \mathbf{H} - \frac{\partial \mathbf{D}}{\partial t} &= \mathbf{J} \quad \text{(Ampere's law)}\\ \nabla \cdot \mathbf{B} &= 0 \quad \text{(Gauss's law of magnetism)}\end{aligned}$$

where we use the constitutive relations to allow for the polarization $\mathbf{P}$ and magnetization $\mathbf{M}$ of dielectrics

$$\begin{aligned}\mathbf{D} &= \epsilon_0 \mathbf{E} + \mathbf{P} = \mathcal{D}(\mathbf{E})\\ \mathbf{B} &= \mu_0(\mathbf{H} + \mathbf{M}) = \mathcal{B}(\mathbf{H})\end{aligned}$$

so that ρ and $\mathbf{J}$ refer to free charges and currents, respectively, and $\mathbf{E}, \mathbf{B}$ are the vector fields with ∇ the vector gradient.

Maxwell's four equations along with the Lorentz force law

$$\mathbf{F} = q(\mathbf{E} + \mathbf{v} \times \mathbf{B})$$

completely summarize classical electrodynamics [43]. The charge continuity equation $\nabla \cdot \mathbf{J} = -(\partial \rho / \partial t)$ is contained within Ampère's law. If we assume the behavior of charges in a dielectric is governed by Ohm's law, then we also have $\mathbf{J} = \sigma \mathbf{E}$, where we have ignored the magnetic component of the Lorentz force.

If we include a time rate parameter α, then we define the family time $\tau = \alpha t$, and then Maxwell's equations, which include a time derivative, become [13], [42]

$$\begin{aligned}\nabla \times \mathbf{E} + \alpha \partial_\tau \mathbf{B} &= 0,\\ \nabla \times \mathbf{H} - \alpha \partial_\tau \mathbf{D} &= \mathbf{J}.\end{aligned}$$

We can define the vector fields, as a power series in α, for example, using the electric field we have

$$\begin{aligned}\mathbf{E} &= \mathbf{E}_{\alpha=0} + \alpha \frac{\partial \mathbf{E}}{\partial \alpha}\Big|_{\alpha=0} + \frac{\alpha^2}{2}\frac{\partial^2 \mathbf{E}}{\partial \alpha^2}\Big|_{\alpha=0} + \ldots\\ &\quad + \frac{\alpha^k}{k!}\frac{\partial^k \mathbf{E}}{\partial \alpha^k}\Big|_{\alpha=0} + \ldots\\ &= \mathbf{E}_0 + \alpha \mathbf{E}_1 + \alpha^2 \mathbf{E}_2 + \ldots + \alpha^k \mathbf{E}_k + \ldots \qquad (12)\end{aligned}$$

where

$$\mathbf{E}_k = \frac{1}{k!}\frac{\partial^k \mathbf{E}}{\partial \alpha^k}\Big|_{\alpha=0}.$$

Therefore, the relevant Maxwell's equations become

$$\begin{aligned}&\nabla \times \mathbf{E_0} + \alpha(\nabla \times \mathbf{E_1} + \partial_\tau \mathbf{B}_0) + \alpha^2(\nabla \times \mathbf{E_2} + \partial_\tau \mathbf{B}_1)\\ &\quad + \ldots = 0\\ &\nabla \times \mathbf{H_0} + \alpha(\nabla \times \mathbf{H_1} - \partial_\tau \mathbf{D}_0) + \alpha^2(\nabla \times \mathbf{H_2} - \partial_\tau \mathbf{D}_1)\\ &\quad = \mathbf{J_0} + \alpha \mathbf{J}_1 + \alpha^2 \mathbf{J}_2 + \ldots\\ &\mathbf{J}_0 + \alpha \mathbf{J}_1 + \alpha^2 \mathbf{J}_2 + \ldots = \sigma(\mathbf{E}_0 + \alpha \mathbf{E_1} + \alpha^2 \mathbf{E_2} + \ldots).\end{aligned}$$

Equating orders we find first the zeroth-order Maxwell's equations

$$\begin{aligned}\nabla \times \mathbf{E_0} &= 0\\ \nabla \times \mathbf{H_0} &= \mathbf{J_0}\end{aligned}$$

and the first-order Maxwell's equations

$$\begin{aligned}\nabla \times \mathbf{E_1} + \partial_\tau \mathbf{B_0} &= 0\\ \nabla \times \mathbf{H_1} - \partial_\tau \mathbf{D_0} &= \mathbf{J_1}. \qquad (13)\end{aligned}$$

In the standard approach, we would start with the zeroth-order fields, solving in the static case and by substituting these results into the first-order equations we can then solve these equations and so on, up to as many orders as required to converge to the exact solution. These are then substituted into equations of the form (12) to find an approximation to the full time varying field.

Chua [1] argued for a new electrical component that established a link between $\mathbf{D}_1$ and $\mathbf{B}_1$, which are the first-order fields in the quasi-static expansion, and that these quantities are evaluated instantaneously. From Ohm's law and constitutive relations, Chua writes the relationships between the first-order fields as

$$\mathbf{J}_1 = \mathcal{J}(\mathbf{E}_1) \quad \mathbf{B}_1 = \mathcal{B}(\mathbf{H}_1) \quad \mathbf{D}_1 = \mathcal{D}(\mathbf{E}_1)$$

where $\mathcal{J}$, $\mathcal{B}$, and $\mathcal{D}$ are one-to-one continuous functions defined over space coordinates only. When $\mathbf{E}_0$, $\mathbf{D}_0$, $\mathbf{B}_0$, and $\mathbf{J}_0$ are negligible in the quasi-static expansion of Maxwell's equations, using (13), we are then led to a relationship between $\mathbf{D}_1$ and $\mathbf{B}_1$, which Chua used as a basis to postulate the memristor.

1) Derivation of Memristor Category: From the relation $\mathbf{D_1} = \mathcal{F}(\mathbf{B_1})$, we find in terms of the scalar magnitudes

$$\epsilon \frac{\partial E}{\partial \alpha} = \frac{\partial f(B)}{\partial \alpha} = f(w)\frac{\partial B}{\partial \alpha}$$

where $f(w)$, dependent on a state variable w, must not be a function of B or the time scale α. Hence, $\epsilon dE = f(w)dB$ or for a circuit element assuming $E = V/D$, we have

$$\frac{\epsilon}{D}V = f(w)f(s)\frac{\mu i}{2\pi}$$

where $f(s,z) \approx 1/s$ gives the spatial distribution of B, where s is the radius in cylindrical coordinates. Hence, we find

$$V = R(w)\frac{dq}{dt}.$$

Chua's relationship between $\mathbf{D_1}$ and $\mathbf{B_1}$ implies a memristor-type element depending on a state variable w. The HP memristor, for example, has w proportional to q.

2) Quasi-Static Expansion of Maxwell's Equations Using Geometric Algebra: The quasi-static expansion of Maxwell's equations was used by Chua in order to justify the existence of a new circuit element he called the memristor. GA [44] is known to produce a very efficient representation of Maxwell's four equations, requiring just a single equation, and so by producing the quasi-static expansion in GA, clearer insights may be forthcoming. It should be noted that the expansion series is not guaranteed to converge and so perhaps not too much should be read into different components of a perturbation series, however it does provide insights into possible field and current relationships.

In GA, Maxwell's equations can be written in a single equation in linear isotropic media [45] as

$$\left(\frac{1}{c}\partial_t + \nabla\right)F = J$$

where $F = c\mathbf{D} + i\mathbf{H}$, $J = c\rho - \mathbf{J}$, and c is the speed of light. Geometric algebra typically represents multivector variables such as F and J, in plain type, as opposed to pure vectors which are identified with bold type. Using the expansion given in (12), we can write

$$\left(\frac{\alpha}{c}\partial_\tau + \nabla\right)(F_0 + \alpha F_1 + \alpha^2 F_2 + \ldots) = (J_0 + \alpha J_1 + \alpha^2 J_2 + \ldots).$$

Thus, it can be seen that the orders of the quasi-static expansion become

$$\begin{aligned} \nabla F_0 &= J_0 \\ \partial_\tau F_0 + \nabla F_1 &= J_1 \\ \partial_\tau F_1 + \nabla F_2 &= J_2 \\ \ldots &= \ldots \end{aligned}$$

The process of solution is now very clear in GA. From the zeroth-order fields we calculate F_0, which is substituted into the first-order fields to find F_1, and so on. Chua also states that $\mathbf{D_0} = \mathbf{H_0} = 0$ and hence $F_0 = 0$. Therefore, we have the relation

$$\nabla F_1 = J_1.$$

This equation fixes the value of F_1, and hence there must be a relationship between $\mathbf{D_1}$ and $\mathbf{H_1}$, or equivalently, $\mathbf{D_1}$ and $\mathbf{B_1}$, as deduced by [1], which again is the memristor element.

3) Confirm Equivalence of GA With Vector Calculus Form: The geometric product between two vectors is given by [44]

$$\mathbf{uv} = \mathbf{u}\cdot\mathbf{v} + i\mathbf{u}\times\mathbf{v}.$$

Expanding and equating scalars, vectors, bivectors, and trivectors parts in the zeroth-order case, we find

$$\begin{aligned} \nabla\cdot D_0 &= \rho_0 \quad \text{(scalar)} \\ -\nabla\times H_0 &= -\mathbf{J_0} \quad \text{(vector)} \\ \nabla\times D_0 &= 0 \quad \text{(bivector)} \\ \nabla\cdot H_0 &= 0 \quad \text{(trivector)} \end{aligned}$$

the expected zeroth-order equations. The magnetic component of force is much smaller than the electric component, and hence we can write $\mathbf{J} = \sigma\mathbf{E}$. Hence, for the case with steady currents, inspecting the vector equation, we form a link between H_0 and E_0. The first-order equations are

$$\begin{aligned} \nabla\cdot D_1 &= \rho_1 \quad \text{(scalar)} \\ \frac{\partial \mathbf{D_0}}{dt} - \nabla\times H_1 &= -\mathbf{J_1} \quad \text{(vector)} \\ \frac{\partial \mathbf{H_0}}{cdt} + \nabla\times D_1 &= 0 \quad \text{(bivector)} \\ i\nabla\cdot H_1 &= 0 \quad \text{(trivector)} \end{aligned}$$

in agreement with the quasi-static expansion in [1].

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