Memristor MOS Content Addressable Memory (MCAM): Hybrid Architecture for Future High Performance Search Engines

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***Abstract*—Large-capacity content addressable memory (CAM) is a key element in a wide variety of applications. The inevitable complexities of scaling MOS transistors introduce a major challenge in the realization of such systems. Convergence of disparate technologies, which are compatible with CMOS processing, may allow extension of Moore's Law for a few more years. This paper provides a new approach towards the design and modeling of Memory resistor (Memristor)-based CAM (MCAM) using a combination of memristor MOS devices to form the core of a memory/compare logic cell that forms the building block of the CAM architecture. The non-volatile characteristic and the nanoscale geometry together with compatibility of the memristor with CMOS processing technology increases the packing density, provides for new approaches towards power management through disabling CAM blocks without loss of stored data, reduces power dissipation, and has scope for speed improvement as the technology matures.**

***Index Terms*—Content addressable memory (CAM), memory, memory resistor-based CAM (MCAM), memory resistor (memristor)-MOS hybrid architecture, modeling.**

I. Introduction

THE QUEST for a new hardware paradigm that will attain processing speeds in the order of an exaflop (10^{18} floating point operations per second) and further into the zetaflop regime (10^{21} flops) is a major challenge for both circuit designers and system architects. The evolutionary progress of networks such as the Internet also brings about the need for realization of new components and related circuits that are compatible with CMOS process technology as CMOS scaling begins to slow down [1]. As Moore's Law becomes more difficult to fulfill, integration of significantly different technologies such as spintronics [1], carbon nano tube field effect transistors (CNFET) [2], optical nanocircuits based on metamaterials [3], and more recently the memristor [4], are gaining more focus thus creating new possibilities towards realization of innovative circuits and systems within the *system on system* (SoS) domain.

In this paper we explore conceptualization, design, and modeling of the memory/compare cell as part of a memristor-based content addressable memory (MCAM) architecture using a combination of memristor and n-type MOS devices. A typical content addressable memory (CAM) cell forms a SRAM cell that has two n-type and two p-type MOS transistors, which requires both V_{DD} and GND connections as well as well-plugs within each cell. Construction of a SRAM cell that exploits memristor technology, which has a non-volatile memory (NVM) behavior and can be fabricated as an extension to a CMOS process technology with nanoscale geometry, addresses the main thread of current CAM research towards reduction of power consumption.

The design of the CAM cell is based on the fourth passive circuit element, the memristor (M) predicted by Chua in 1971 [5] and generalized by Kang [6], [7]. Chua postulated that a new circuit element defined by the single-valued relationship $d\phi = Mdq$ must exist, whereby current moving through the memristor is proportional to the flux of the magnetic field that flows through the material. In another words, the magnetic flux between the terminals is a function of the amount of charge, q, that has passed through the device. This follows from Lenz's law whereby the single-valued relationship $d\phi = Mdq$ has the equivalence $v = M(q)i$, where v and i are memristor voltage and current, respectively.

The memristor behaves as a switch, much like a transistor. However, unlike the transistor, it is a two-terminal rather than a three-terminal device and does not require power to retain either of its two states. Note that a memristor changes its resistance between two values and this is achieved via the movement of mobile ionic charge within an oxide layer, furthermore, these resistive states are non-volatile. This behavior is an important property that influences the architecture of CAM systems, where the power supply of CAM blocks can be disabled without loss of stored data. Therefore, memristor-based CAM cells have the potential for significant saving in power dissipation.

This paper has the following structure. Section II is an introductory section and reviews the properties of the memristor and then explores various options available in the modeling of this

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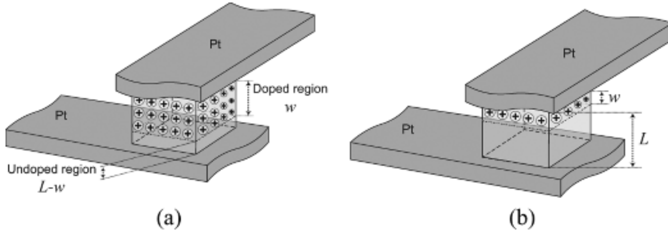


Fig. 1. Memristor switching behavior. (a) "ON" state, low resistance, (b) "OFF" state, high resistance. The key feature of memristor is it can remember the resistance once the voltage is disconnected. In (a) "doped" and "undoped" regions are related to R_{ON} and R_{OFF}, respectively. The dopant consists of mobile charges. In (b), L and w are the thin-film thickness and doped region thickness, respectively.

device. In Section III, circuit options for realization of MCAM is investigated whereby the two disparate technologies converge to create a new CMOS-based design platform. Section IV provides simulation results of a basic MCAM cell to be implemented as part of a future search engine. The details of our proposed layout and preliminary CMOS overlay fabrication approach are also presented in Section V. The concluding comments are provided in Section VI.

II. Characterization and Modeling Behavior of Memristor

Strukov *et al.* [4] presented a physical model whereby the memristor is characterized by an equivalent time-dependent resistor whose value at a time t is linearly proportional to the quantity of charge q that has passed through it. They realized a proof-of-concept memristor, which consists of a thin nano layer (2 nm) of $\mathrm{TiO_2}$ and a second oxygen deficient nano layer of TiO_{2-x} (8 nm) sandwiched between two Pt nanowires ($\sim$ 50 nm), shown in Fig. 1 [4]. Oxygen (O^{2-}) vacancies are $+2$ mobile carriers and are positively charged. A change in distribution of O^{2-} within the $\mathrm{TiO_2}$ nano layer changes the resistance. By applying a positive voltage, to the top platinum nanowire, oxygen vacancies drift from the TiO_{2-x} layer to the $\mathrm{TiO_2}$ undoped layer, thus changing the boundary between the TiO_{2-x} and $\mathrm{TiO_2}$ layers. As a consequence, the overall resistance of the layer is reduced corresponding to an "ON" state. When enough charge passes through the memristor that ions can no longer move, the device enters a hysteresis region and keeps q at an upper bound with fixed memristance, M (memristor resistance). By reversing the process, the oxygen defects diffuse back into the TiO_{2-x} nano layer. The resistance returns to its original state, which corresponds to an "OFF" state. The significant aspect to be noted here is that only ionic charges, namely oxygen vacancies (O^{2-}) through the cell, change memristance. The resistance change is non-volatile hence the cell acts as a memory element that remembers past history of ionic charge flow through the cell.

A. Simplified Memristor Model

The memristor can be modeled in terms of two resistors in series, namely the doped region and undoped region each having vertical width of w and $L-w$, respectively, as shown in Fig. 1, where L is the $\mathrm{TiO_2}$ film thickness [4]. The voltage-current relationship defined as $M(q)$, can be modeled as [5]

$$v(t)=\left(R_{\mathrm{ON}}\frac{w(t)}{L}+R_{\mathrm{OFF}}\left(1-\frac{w(t)}{L}\right)\right)i(t) \quad (1)$$

where R_{ON} is the resistance for completely doped memristor, while R_{OFF} is the resistance for the undoped region. The width of the doped region $w(t)$ is given by

$$\frac{dw(t)}{dt}=\mu_v\frac{R_{\mathrm{ON}}}{L}i(t) \quad (2)$$

where μ_v represents the average dopant mobility $\sim 10^{-10}$ $\mathrm{cm^2/s/V}$. Taking a normalized variable, $x(t)=w(t)/L$, instead of $w(t)$ assists in tracking memristance, $M(q)=d\phi/dq$, or memductance, $W(\phi)=dq/d\phi$. The new normalized relation is

$$\frac{dx(t)}{dt}=\mu_v\frac{R_{\mathrm{ON}}}{L^2}i(t) \quad (3)$$

where L^2/μ_v has the dimensions of magnetic flux (ϕ). Following the calculation steps from Kavehei *et al.* [8], a simple memristance model can be defined as

$$M(t)=R_{\mathrm{OFF}}\left(\sqrt{1-\frac{2c(t)}{r}}\right) \quad (4)$$

where $c(t)=\mu_v\phi(t)/L^2$, and r is a ratio of $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ and $\sqrt{1-2c(t)/r}$ is the *resistance modulation index*. Here, $x(t)$ can now be rewritten as

$$x(t)=1-\left(\sqrt{1-\frac{2\phi(t)}{r\beta}}\right) \quad (5)$$

which highlights that the $r\beta$ term (where $\beta=L^2/\mu_v$) must be made sufficiently large to maintain $2\phi(t)/r\beta$ between the range 0 and 1. The simplified linear ionic drift model facilitates the understanding of the operational characteristics of the memristor. However, for a highly nonlinear [9] relationship between electric field and drift velocity that exists at the boundaries, the ratio cannot be maintained. Thus this function is unable to model large nonlinearities close to the boundaries of the memristor characteristics. At the boundaries, i.e., when x approaches 0 or 1, there is a nonlinearity associated with the memristor behavior that is discussed in Section II-B.

B. Modelling the Nonlinear Behavior of Memristor

The electrical behavior of the memristor as a switch/memory element is determined by the boundary between the two regions in response to an applied voltage. To model this nonlinearity, the memristor state (3) is augmented with a *window function*, $F(w,i)$[4], [10]–[12], where w and i are the memristor's state variable and current, respectively.

Thus, (3) can be rewritten as

$$\frac{dx(t)}{dt}=\frac{R_{\mathrm{ON}}}{\beta}i(t)F(x(t),p) \quad (6)$$

TABLE I
COMPARISON BETWEEN DIFFERENT MEMRISTOR MODELS. FOR A-II, B-I, AND B-II $x = w/L$

Model	Ref	Window Function $F(\cdot)$	Boundaries $(x \to 0, x \to 1)$	Problem(s)
A-I	[4]	$w(1-w)/L^2$	(0,∼ 0)	Linear approximation, $x \in [0, 1]$ Stuck at the terminal states $F(w \to L) \neq 0$
A-II	[12]	$x(1-x)$	(0, 0)	Linear approximation, $x \in [0, 1]$ Stuck at the terminal states
B-I	[13]	$1-(2x-1)^{2p}$	(0, 0)	Stuck at the terminal states
B-II*	[11]	$1-(x-\text{sgn}(-i))^{2p}$	(0, 0)	Discontinuity at the boundaries

* This model is adopted for the simulations.

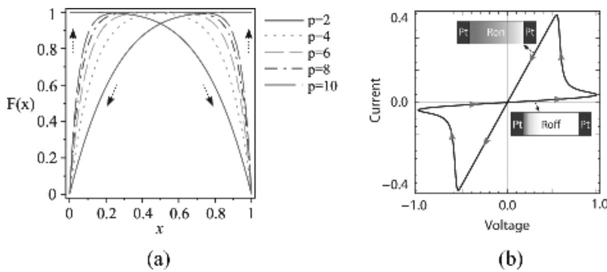


Fig. 2. Nonlinear behavior of the memristor. (a) Window function: $F(x) = 1 - (x - \text{sgn}(-i))^{2p}$, where $\text{sgn}(I)$ gives the sign of the input signal I. (b) The hysteresis characteristics using the nonlinear drift assumption. This hysteresis shows a highly nonlinear relationship between current and voltage at the boundaries.

where p is its *control parameter*. The nonlinearity at the boundaries can now be controlled with parameter p. The influence of a window function described by (6) is illustrated in Fig. 2(a) for $2 \leq p \leq 10$.

Joglekar and Wolf [13] proposed a modified window function to approximately address linear ionic drift and the nonlinear behaviour at the boundaries when $0 < x < 1$. For the window function $F(x) = 1 - (2x - 1)^{2p}$, p is a positive integer and $x = w/L$. This model considers a simple boundary condition, $F(0) = F(1) = 0$, when $p \geq 4$, the state variable equation is an approximation of the linear drift assumption, $F(0 < x < 1) \approx 1$. This model is denoted by B-I in Table I.

Based on this model, when a memristor is at the terminal states, no external stimulus can change its state. Biolek *et al.* [11] addressed this problem with a new window function, $F(x) = 1 - (x - \text{sgn}(-i))^{2p}$, where i is the memristor current, $\text{sgn}(i) = 1$ when $i \geq 0$, and $\text{sgn}(i) = 0$ when $i < 0$. When current is positive, the doped region length, w, is expanding. This model is denoted by B-II in Table I and is adopted for the simulations that follow.

The hysteresis characteristic using the nonlinear drift assumption is illustrated in Fig. 2(b). This hysteresis shows a highly nonlinear relationship between current and voltage at the boundaries as is derived using similar parameters reported by Strukov *et al.* [4]

To conclude this section Table I shows a brief comparison between different behavioral memristor models. It is also important to emphasis that the modeling approach in this paper is based on the behavioral characteristics of the solid-state thin film memristor device [4]. Shin *et al.* [14] recently proposed compact macromodels for the solid-state thin film memristor device. Even though the assumption is still based on the linear drift model, their approach provides a solution for bypassing current flow at the two boundary resistances.

C. Emerging Memory Devices and Technologies

Memory processing has been considered as the pace-setter for scaling a technology. A number of performance parameters including capacity (that relate to area utilization), cost, speed (both access time and bandwidth), retention time, and persistence, read/write endurance, active power dissipation, standby power, robustness such as reliability and temperature related issues characterize memories. Recent and emerging technologies such as phase-change random access memory (PCRAM), magnetic RAM (MRAM), ferroelectric RAM (FeRAM), resistive RAM (RRAM), and memristor, have shown promise and some are already being considered for implementation into emerging products. Table II summarizes a range of performance parameters and salient features of each of the technologies that characterize memories [15], [16]. A projected plan for 2020 for memories highlight a capacity greater than 1 TB, read/write access times of less than 100 ns and endurance in the order of 10^{12} or more write cycles.

Flash memories suffer from both a slow write/erase times and low endurance cycles. FeRAMs and MRAMs are poorly scalable. MRAMs and PCRAMs require large programming currents during write cycle, hence an increase in dissipation per bit. Furthermore, voltage scaling becomes more difficult. Memristors, however, have demonstrated promising results in terms of the write operation voltage scaling [10], [17].

Memristor crossbar-based architecture is highly scalable [18] and shows promise for ultra-high density memories [19]. For example, a memristor with minimum feature sizes of 10 and 3 nm yield 250 Gb/cm^2 and 2.5 Tb/cm^2, respectively.

In spite of the high density, zero standby power dissipation, and long life time that have been pointed out for the emerging memory technologies, their long write latency has a large negative source of impact on memory bandwidth, power consumption, and the general performance of a memory system.

III. CONVENTIONAL CAM AND THE PROPOSED MCAM STRUCTURES

A content addressable memory illustrated in Fig. 3 takes a search word and returns the matching memory location. Such an approach can be considered as a mapping of the large space

TABLE II
TRADITIONAL AND EMERGING MEMORY TECHNOLOGIES

	Traditional Technologies				Emerging Technologies			
			Improved Flash					
	DRAM	SRAM	NOR	NAND	FeRAM	MRAM	PCRAM	Memristor
Knowledge level	mature		advanced		product		advanced	early stage
Cell Elements	1T1C	6T	1T		1T1C	1T1R	1T1R	1M
Half pitch (F) (nm)	50	65	90	90	180	130	65	3-10
Smallest cell area (F^2)	6	140	10	5	22	45	16	4
Read time (ns)	< 1	< 0.3	< 10	< 50	< 45	< 20	< 60	< 50
Write/Erase time (ns)	< 0.5	< 0.3	10^5	10^6	10	20	60	< 250
Retention time (years)	seconds	N/A	> 10	> 10	> 10	> 10	> 10	> 10
Write op. voltage (V)	2.5	1	12	15	0.9-3.3	1.5	3	< 3
Read op. voltage (V)	1.8	1	2	2	0.9-3.3	1.5	3	< 3
Write endurance	10^{16}	10^{16}	10^5	10^5	10^{14}	10^{16}	10^9	10^{15}
Write energy (fJ/bit)	5	0.7	10	10	30	1.5×10^5	6×10^3	< 50
Density (Gbit/cm^2)	6.67	0.17	1.23	2.47	0.14	0.13	1.48	250
Voltage scaling	fairly scalable					no	poor	promising
Highly scalable	major technological barriers				poor		promising	promising

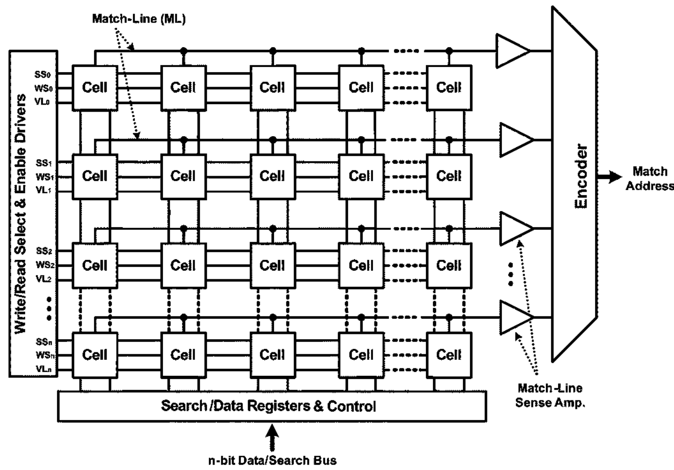
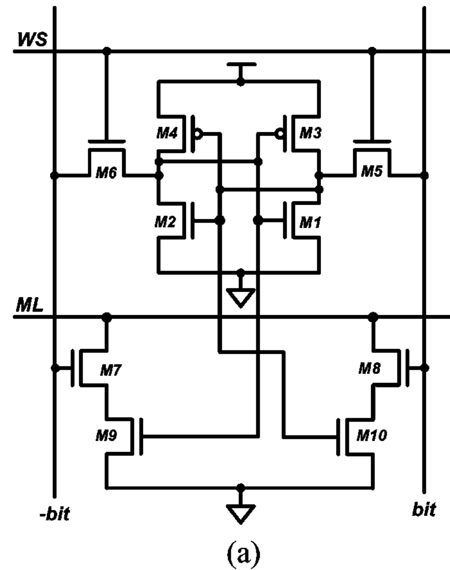


Fig. 3. Generic content addressable memory architecture for $n \times n$ NAND-type CAM cells. In this structure each data (D) and search (S) bits share one common bus line (D/S) to reduce the interconnection complexity. The architecture is based on the MCAM cell of Fig. 6(d) and the match lines (MLs) composed of nMOS pass transistors.

of input search word to that of the smaller space of output match location in a single clock cycle [20]. There are numerous applications including translation lookaside buffers (TLB), image coding [21], classifiers to forward Internet protocol (IP) packets in network routers [22], etc. Inclusion of memristors in the architecture ensures that data is retained if the power source is removed enabling new possibilities in system design including the all important issue of power management.

A. Conventional CAM

To better appreciate some of the benefits of our proposed structure we provide a brief overview of the conventional CAM cell using static random access memory (SRAM) as shown in Fig. 4(a). The two inverters that form the latch use four transistors including two p-type transistors that normally require more silicon area. Problems such as relatively high leakage current particularly for nanoscaled CMOS technology [23] and the need for inclusion of both $V_{\rm DD}$ and ground lines in each cell bring further challenges for CAM designers in order to increase the packing density and still maintain sensible power dissipation. Thus, to satisfy the combination of ultra dense designs, low-power (low-leakage), and high-performance, the SRAM cell is the focus of architectural design considerations.



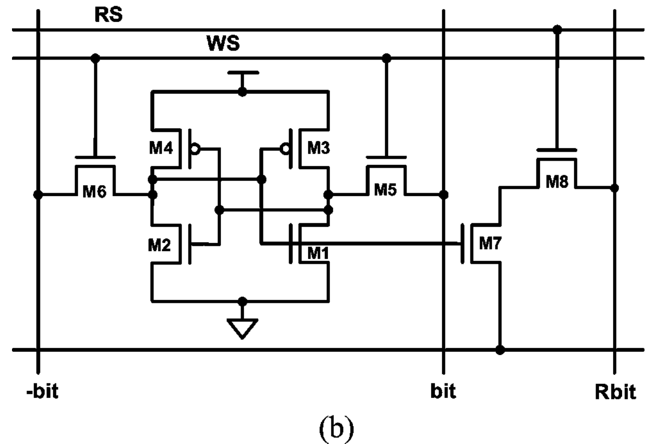


Fig. 4. Conventional CAM cell structure and the design of a SRAM cell for ultra low-power applications. In (a) a conventional 10-T NOR-type CAM circuit is demonstrated. Usually, conventional NOR- or NAND-type CAM cells have more than 9 transistors [26]. In (a) and (b), RS, Rbit, WS, ML, bit, and -bit lines are read select, read bit-line, word select, match line, data, and complementary data signals. (a) Conventional 10-T NOR-type CAM Cell. (b) 8-T subthreshold SRAM Cell [23].

For instance, one of the known problems of the conventional 6-T SRAM for ultra low-power applications is its static noise margin (SNM) [23]. Fundamentally, the main technique used to design an ultra low-power memory is voltage scaling that brings CMOS operation down to the subthreshold regime. Verma and Chandrakasan [23] demonstrated that at very low supply voltages the static noise margin for SRAM will disappear due to process variation. To address the low SNM for subthreshold supply voltage Verma and Chandrakasan [23] proposed 8-T SRAM cell shown in Fig. 4(b). This means, there is a need for significant increase in silicon area to have reduced failure when the supply voltage has been scaled down.

Failure is a major issue in designing ultra dense (high capacity) memories. Therefore, a range of fault tolerance techniques are usually applied [24]. As long as the defect or failure results from the SRAM structure, a traditional approach such as replication of memory cells can be implemented. Obviously it causes a large overhead in silicon area which, exacerbates the issue of power consumption.

Some of the specific CAM cells, for example, ternary content addressable memory (TCAM) normally used for the design of high-speed lookup-intensive applications in network routers, such as packet forwarding and classification two SRAM cells, are required. Thus, the dissipation brought about as the result of leakage becomes a major design challenge in TCAMs [25]. It should be noted that the focus in this paper is to address the design of the store/compare core cell only, leaving out details of CAM's peripherals such as read/write drivers, encoder, matchline sensing selective precharge, pipelining, matchline segmentation, current saving technique, etc., that characterize a CAM architecture [26].

B. Generic Memristor-nMOS Circuit

Fig. 5 shows the basic structure for a memristor-nMOS storage cell. For writing a logic "1," the memristor receives a positive bias to maintain an "ON" state. This corresponds to the memristor being programmed as a logic "1." To program a "0" a reverse bias is applied to the memristor, which makes the memristor resistance high. This corresponds to logic "0" being programmed.

C. MCAM Cell

In this subsection, variations of MCAM cells as well as a brief architectural perspective are introduced. The details of read/write operations and their timing issues are also discussed in Section IV. A CAM cell serves two basic functions: "bit storage" and "bit comparison." There are a variety of approaches in the design of basic cell such as NOR-based match line, NAND based match line, etc. This part of the paper reviews the properties of conventional SRAM-based CAM and provides a possible approach for the design of content addressable memory based on the memristor.

1) MCAM Cell Properties: Fig. 6 illustrates several variations of the MCAM core whereby bit-storage is implemented by memristors ME1 and ME2. Bit comparison is performed by either NOR or alternatively NAND-based logic as part of the match-line ML_i circuitry. The matching operation is equivalent to logical XORing of the search bit (SB) and stored bit (D). The match-line transistors (ML) in the NOR-type cells can be considered as part of a pull-down path of a precharged NOR gate connected at the end of each individual ML_i row. The NAND-type CAM functions in a similar manner forming the pull-down of a precharged NAND gate. Although each of the selected cells in Fig. 6 have their relative merits, the approach in Fig. 6(c) where Data bits and Search bits share a common bus is selected for detailed analysis. The structure of the 7-T NAND-type, shown in Fig. 6(d), and the NOR-type are identical except for the position of the ML transistor. In the NOR-type, ML makes a connection between shared ML and ground while in the NAND-type, the ML transistors act as a series of switches between the ML_i and ML_{i+1}.

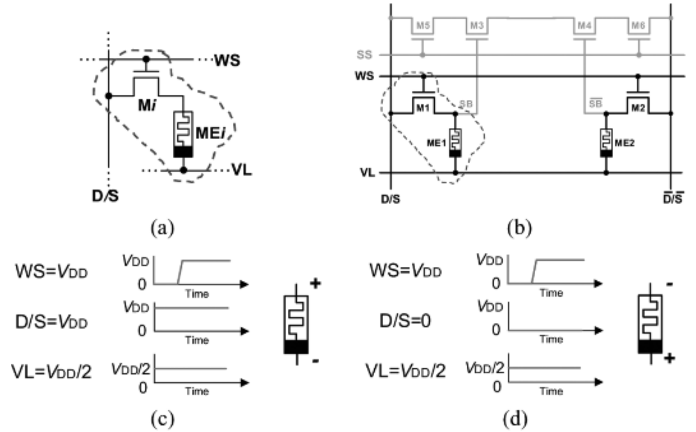


Fig. 5. Basic memristor-nMOS storage cell and the timing diagram. (a) shows write mode part of the ith cell in a row. (b) Basic cell circuit without the match-line transistor. (c) "Low" resistance, R_{ON}, programing. Equivalent to logic "1." (d) "High" resistance, R_{OFF}, programing. Equivalent to logic "0." (a) Structure of write mode. (b) Basic cell. (c) Program "Low" resistance "1." (d) Program "High" resistance "0."

IV. Simulation Results Analysis and Comparison

Generally, there are the "write" and "read" operations that require consideration. In this section the "write" and "read" operations of the basic MCAM cell for 7-T NOR-type are reported. Simulations of the circuits are based on the following parameters [27]: $R_{\mathrm{ON}} = 100\ \Omega$, $R_{\mathrm{OFF}} = 100\ \mathrm{k}\Omega$, $p = 4$, $L = 3$ nm, and $\mu_v = 3 \times 10^{-8}\ \mathrm{m}^2/\mathrm{s/V}$. Both the conventional CAM and MCAM circuits have been implemented using Dongbu HiTech 0.18-μm technology where 1.8 V is the nominal operating voltage for the CAM. The MCAM cell is implemented using nMOS devices and memristors without the need for V_{DD} voltage source. Using the above memristor parameters, together with the behavioral model B-II of Table I, satisfactory operation of the MCAM cell is achieved at 3.0 Volts. We have referred to this voltage as the nominal voltage for the MCAM cell. Furthermore, the initial state of the memristors ("ON," "OFF," or in between) is determined by initial resistance, R_{INIT}.

A. Write Operation

At the write phase, the memristor ME1 is programmed based on the data bit on the D line. The complementary data is also stored in ME2. During the write operation, the select line is zero

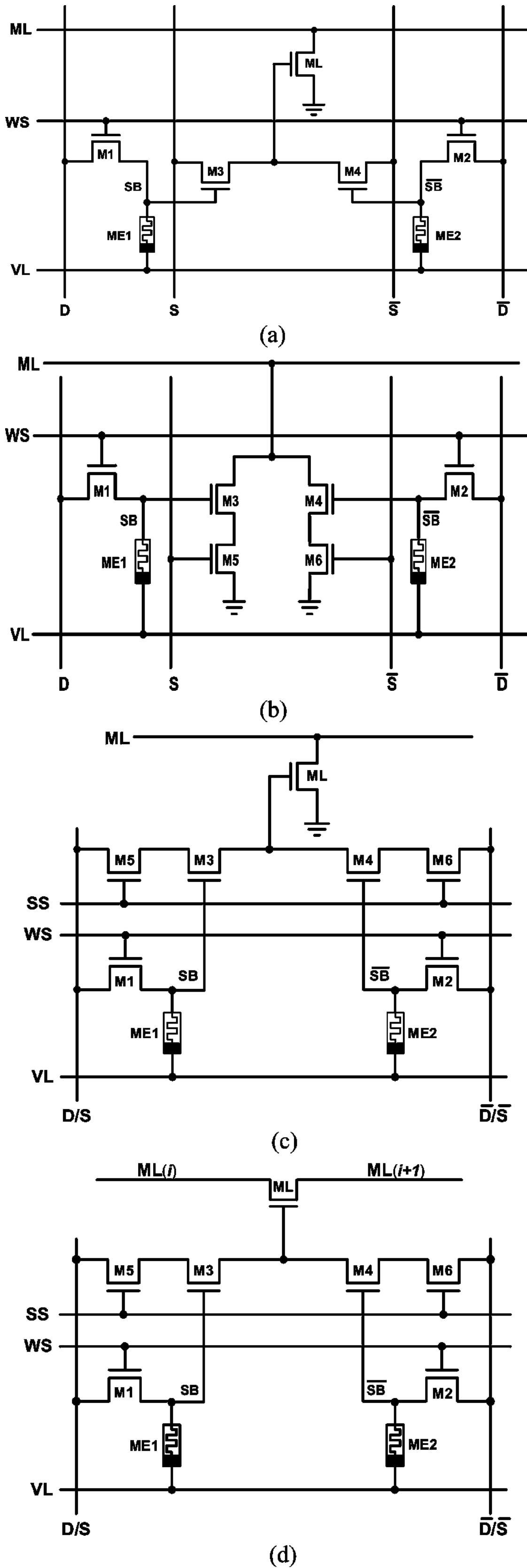


Fig. 6. Cell configurations of possible MCAM structures. (a) 5-T NOR-type. (b) 6-T NOR-type. (c) 7-T NOR-type. (d) 7-T NAND-type.

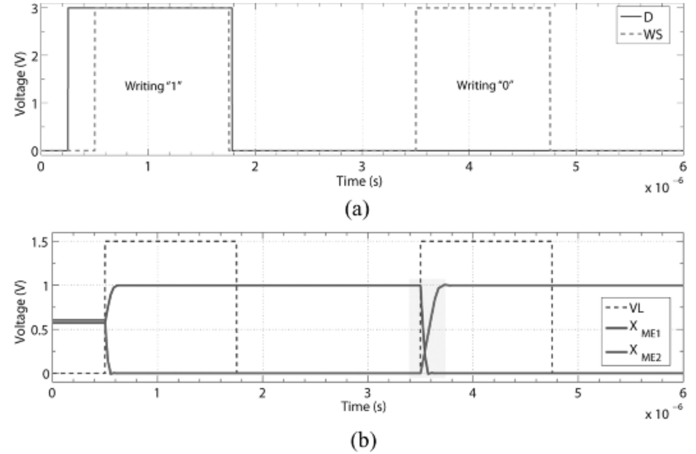


Fig. 7. Write operation timing diagram. The highlighted area in (b) shows the minimum time for writing, which is the maximum for both memristors, around 220 ns. In (b) x_{ME1} and x_{ME2} are dimensionless parameters and both are varying between 0 and 1. The rational for showing VL and x_{ME1} and x_{ME2} together is that VL acts as a trigger for the state variables. $\mathrm{VL}_{\mathrm{active}} = 1.5$ V$(V_{\mathrm{DD}}/2)$ for write operation. (a) Data (D) and Word Select (WS) signals. WS pulse width is 1.2 μs. (b) Write enable, VL, and memristors state, x_{ME1} and x_{ME2}, signals.

and an appropriate write voltage is applied on VL. The magnitude of this voltage is half of supply voltage, that corresponds to $V_{\mathrm{DD}}/2$. The pulse width is determined by the time required for the memristor to change its state from logic "1" (R_{ON}) to logic "0" (R_{OFF}) or vice versa. Waveforms in Fig. 7 illustrate the write operation. In this case $R_{\mathrm{INIT}} = 40$ kΩ and the initial state is around 0.6. The diagrams show two write operations, for both when D is "1" and when it is "0." By applying $V_{\mathrm{DD}}/2$ to VL line, there will be a $-V_{\mathrm{DD}}/2$ potential across the memristor ME2 and $V_{\mathrm{DD}} - V_{\mathrm{th,M1}}$ across the memristor ME1.

The highlighted area in Fig. 7(b) shows the difference in the write operation between ME1 and ME2. When $D = 0$ and $\overline{\mathrm{D}} = V_{\mathrm{DD}}$, there is a threshold voltage (V_{th}) drop at the $\overline{\mathrm{SB}}$ node. Thus, the potential across the memristor would be $V_{\mathrm{DD}}/2 - V_{\mathrm{th,M2}}$. At the same time, $-V_{\mathrm{DD}}/2$ is the voltage across the ME1, so the change in state in ME1 occurs faster than memristor ME2. The time for a state change is approximately 75 ns for ME1 and 220 ns for ME2. Therefore, 145 ns delay is imposed because of the voltage drop across the ME2. Fig. 7(b) illustrates simulation results carried out using a behavioral SPICE macro-model.

B. Read Operation

Let us assume that ME1 and ME2 were programmed as a logic "1" and logic "0," respectively. Therefore, ME1 and ME2 are in the "ON" and "OFF" states and $R_{\mathrm{INIT,ME1}} = 200\ \Omega$ and $R_{\mathrm{INIT,ME2}} = 99$ kΩ. In this case, the search line, S, is activated first. At the same time search select signal, SS, is activated to turn on the two select transistors, M5 and M6. The word select (WS) is disabled during the read operation. Fig. 8 shows the waveforms for a complete read cycle. Read operation requires higher voltage for a short period of time. The VL pulse width (PW) for read operation is 12 ns as illustrated in Fig. 8(b) which is the "minimum" pulse width necessary to retain memristor's state.

For a matching "1" (when $S = V_{\mathrm{DD}}$), the sequence of operations are as follows: 1) match line, ML, is pre-charged; 2) SS is

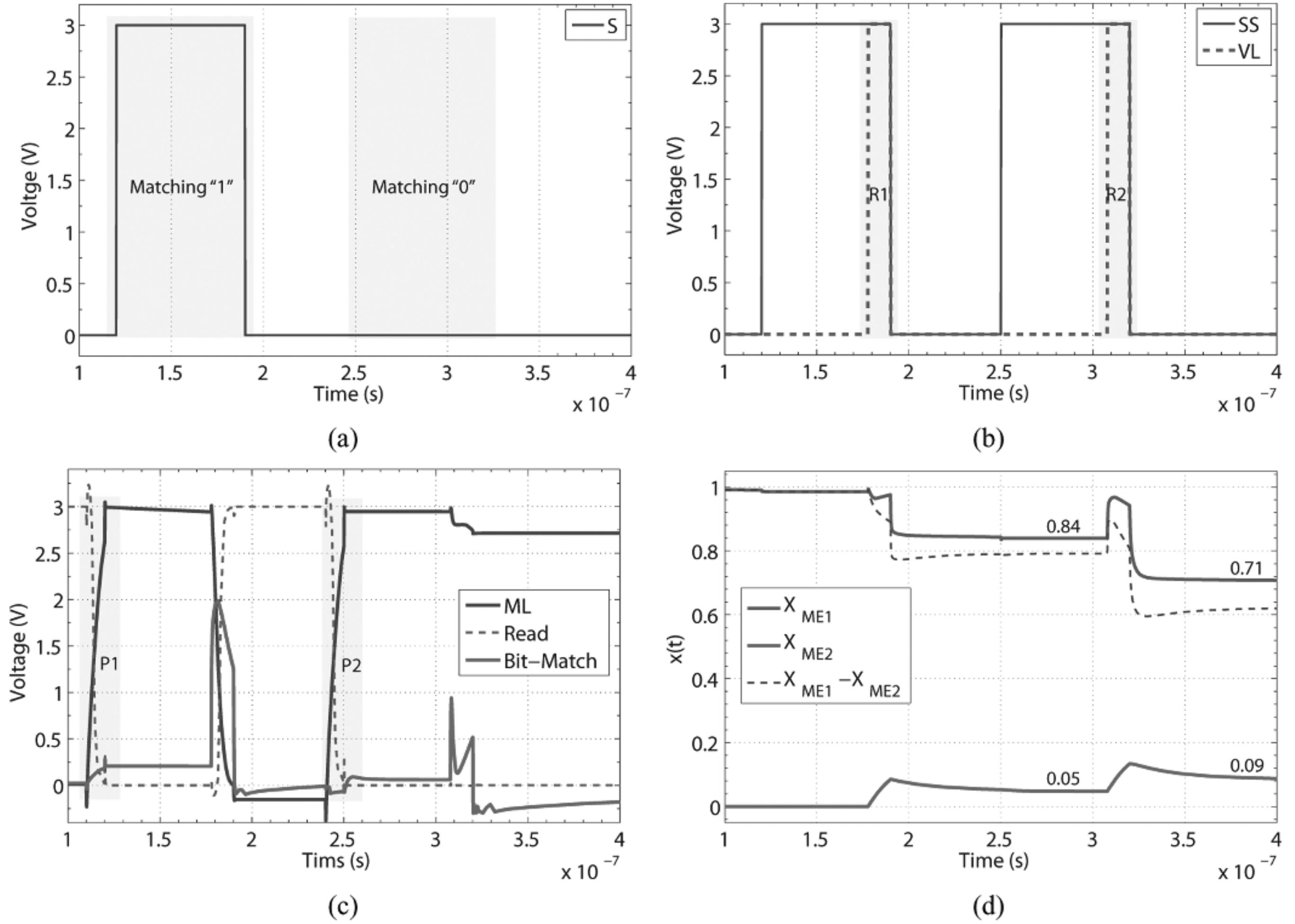


Fig. 8. Read operation timing diagram: (a) Search signal (S). For matching "1" $S = V_{\rm DD}$ and for matching "0" $S = 0$. (b) Search select (SS) and read enable (VL) signals. $\rm VL_{active} = 3.0\ V(V_{DD})$. (c) Bit-match, read, and match-line (ML) signals. $\rm Read = \overline{ML}$. (d) ME1 and ME2 state variable signals. In (b) and (c), R1, R2, P1, and P2 represent two read and match-line pre-charge phases, respectively. The final (stable) values for $x_{\rm ME1}$ and $x_{\rm ME2}$ after two read operations are around 0.7 and 0.09. The difference between $x_{\rm ME1}$ and $x_{\rm ME2}$, in terms of time is also shown in (d).

TABLE III
COMPARISON BETWEEN THE PROPOSED CAM CELLS IN FIG. 6

Cell name	$\rm VL_{min.PW,W}$ [ns] $\rm VL_W = V_{DD}/2$	$\rm VL_{min.PW,R}$ [ns] $\rm VL_R = V_{DD}$	$\rm V_{drop}$(bit-match) Voltage [V]	Data & Search Buses
6-T NOR (Fig. 6(b))	223	5	0	Separate
5-T NOR (Fig. 6(a))	219	9	$V_{\rm th}$	Separate
7-T NOR/NAND (Fig. 6(c/d))	220	12	$V_{\rm th}$	Shared

activated; and 3) VL is enabled as is shown in Fig. 8(a)–(c). A logic "1" is transferred to the bit-match node, which discharges the match line, ML_i, through transistor ML. At this point $x_{\rm ME1}$ commences to decrease its state from 1 to 0.84 and $x_{\rm ME2}$ increases its state from 0 to 0.05. Thus, there is a match between stored Data and Search Data. The following read operation for $S =$ "0" follows a similar pattern as shown in Fig. 8(c). The simulation results confirm the functionality of proposed MCAM circuitry.

C. Simulation Results Analysis

Table III provides a comparison between the various MCAM cells that are proposed in Fig. 6. It is worth noting that simulations are based on a single cell. Therefore there are no differences in characteristics between 7-T NAND and 7-T NOR cells. The difference in minimum VL pulse width for read operation $(\rm VL_{min.PW,R})$, between different MCAM cells, is relatively significant and is brought about as the result of pass-transistors in the path from search line to the bit-match node. One important issue in the design of MCAM cells is endurance. For instance, DRAM cells must be refreshed at least every 16 ms, which corresponds to at least 10^{10} write cycles in their life cycle [28]. Analysing a write operation followed by two serial read operations shows that 5-T, 6-T, and 7-T NOR/NAND cells deliver a promising result. After two serial read operations the memristor state values for $x_{\rm ME1}$ and $x_{\rm ME2}$ are, 0.74 and 0.06, and 0.71 and 0.09, for 5-T, 6-T, and 7-T NOR/NAND cell, respectively. The overall conclusion from the simulation results shows that in terms of speed, the 6-T NOR-type MCAM cell has improved performance, but it uses separate Data and Search lines. The 7-T

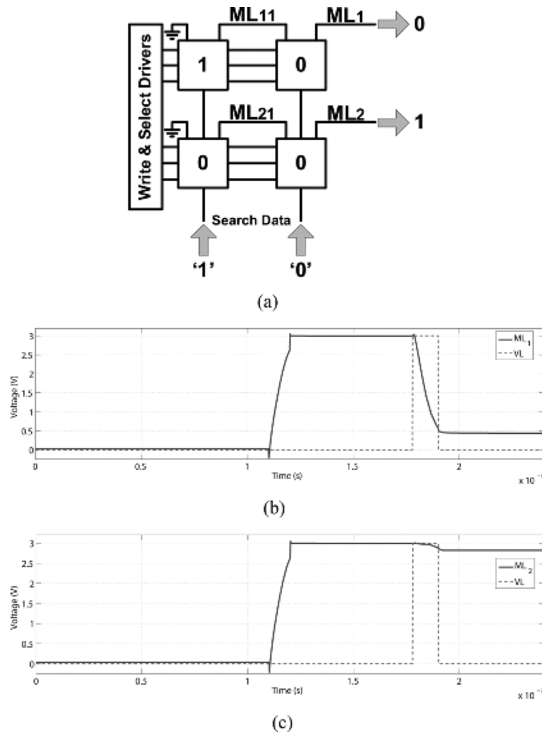


Fig. 9. 2×2 MCAM structure. (a) 2×2 architecture. (b) ML_1 signal. (c) ML_2 signal. The search data ("10") is matched with the first row stored information so the $\mathrm{ML}_1 = 0$ shows the search data is matched with row_1 and $\mathrm{ML}_2 = 1$ shows the data is not matched with the stored information in the second row (row_2). (a) 2×2 architecture, search data ("10"), and matching information. (b) ML_1 signal behavior once VL triggers matching operation. (c) ML_2 signal behavior once VL triggers matching operation.

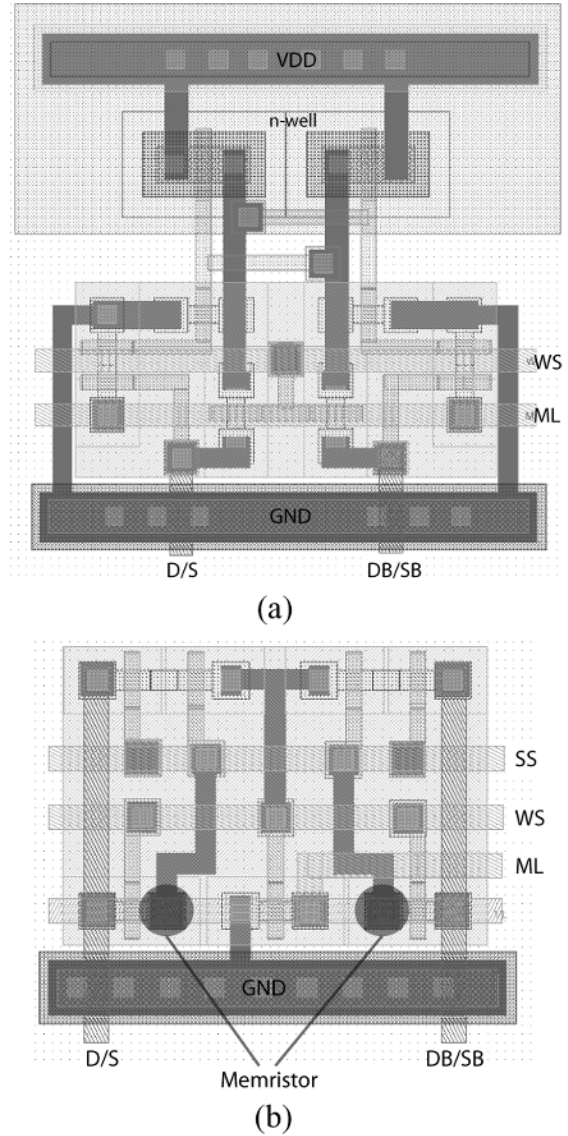


Fig. 10. Layout implementation (a) conventional SRAM-based and (b) proposed MCAM cells. In (a) V_{DD} line is required. In (b), highlighted regions show the two memristors in the upper layer. (a) Conventional 10-T NOR-type CAM cell. (b) 7-/T, 2-M NOR-type MCAM cell.

NOR/NAND cell shares the same line for Data and Search inputs. However, it is slightly slower $\mathrm{VL}_{\min,\mathrm{PW,R}} = 12$ ns, while the swing on the match-line is reduced by threshold voltage (V_{th}) drop.

1) Power Analysis: A behavioral model was used to estimate peak, average, and RMS power dissipation of an MCAM cell compared to the conventional SRAM-based cell. The power consumption is the total value for the static and dynamic power dissipation. A reduction of some 96% in average power consumption with an MCAM cell was noted. The maximum power dissipation reduction is over 74% for the memristor-based structure. The root mean square (RMS) value of current, which is sunk from the supply rail for the MCAM, is around 47 μA less than the conventional SRAM-based circuitry, which shows over 95% reduction. To the best of our knowledge this is the first power consumption analysis of a memristor-based structure using a behavioral modeling approach. As the technology matures it is conjectured that a similar power source could be used for the hybrid scaled CMOS/Memristor cell.

D. A 2×2 Structure Verification

Fig. 9 illustrates implementation of a 2×2 structure whereby the 7-T NAND-type [see Fig. 6(d)] is used. As is stated before, in the NOR-type, ML makes a connection between shared ML and ground while in the NAND-type, the ML transistors act as a series of switches between the $\mathrm{ML}_{\mathrm{out}}$ and ground. The ML_1 and ML_2 match signals, illustrated in Fig. 9(a), are these $\mathrm{ML}_{\mathrm{out}}$ signals. The cells are initially programmed to be "0" or "1" and the search bit vector is "10." The first row cells are programmed "10." As the consequence, ML_1 is discharged since there is a match between the stored and search bit vectors. Fig. 9(b) and (c) demonstrate the ML_1 and ML_2 outputs, respectively. Basically, using the ML transistors as an array of pass-transistors in a NAND-type structure imposes a significant delay, but in this case, the timing information shows the delay of matching process is around 12 ns.

A large scale cosimulation of crossbar memories can be carried out each junction assumed to be either a diode or a 1D-1R (a parallel structure of one diode and one resistor) or even a linear resistor [29]. However, the modeling approach should be carefully revisited since large resistor nonlinearity is associated with crosspoint devices [19]. A cosimulation of crossbar memories, considering the highly nonlinear crosspoint junctions, underpins our longer term research objective.

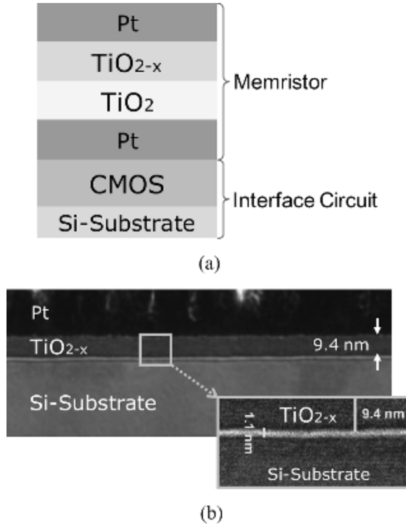


Fig. 11. Cross sectional view of the memristor-MOS implementation and TEM microphotograph of TiO_{2-x} deposition. (a) Cross section of memristor-MOS layout. (b) TEM microphotograph.

V. Physical Layout and Fabrication

A. Physical Layout

Layout of conventional 10-T NOR-type CAM and 7-T NOR-type MCAM cells are shown in Fig. 10. The MCAM cell has a dimensions of 4.8 $\times$ 4.36 μm^2 while the dimensions for the conventional SRAM-based cell is 6.0 $\times$ 6.5 μm^2. Thus, the reduction in silicon area is in the order of 46%. The 2×2 structure also shows over a 46% area reduction. The two memristors, shown in highlighted regions of Fig. 10(b) are implemented between metal-3 and metal-4 layers as part of CMOS post processing.

B. Fabrication and Layer Definitions

Fig. 11(a) illustrates a cross-section of Pt, TiO_2, and TiO_{2-x} layers over silicon substrate. The TiO_2 layer thickness must be restricted below two nanometers, to prevent separate conduction through the individual layers. The n-type MOS devices are patterned onto a silicon wafer using normal CMOS processing techniques, which subsequently is covered with a protective oxide layer. The Pt memristor wires are patterned and connections made to the n-type MOS devices. The upper Pt nanowire is patterned and, electrical connections made by photolithography (to spatially locate the vias) and aluminum metal deposition [4].

Fig. 11(b) demonstrates a TEM microphotograph of a TiO_{2-x} overlay on a silicon substrate in order to explore the controllability of oxygen ions. The device consists of a top gate Pt, $\mathrm{TiO}_2/\mathrm{TiO}_{2-x}$ layer and back gate Pt on SiO_2 layer of silicon. TiO_{2-x} thin film with a thickness of 9.4 nm was deposited on a silicon wafer using sputtering technique. Table IV is deposition result with sputtering technique. Samples show that 1.85% oxygen (O) vacancy can be achieved keeping within the 2% tolerance.

TABLE IV
Deposition Results Using Sputtering Technique

	O %	Ti %	$\mathrm{O} - 2 \times \mathrm{Ti}$ Normalized	$(\mathrm{O} - 2 \times \mathrm{Ti})/\mathrm{Ti}$ Normalized
1	66.46	33.54	−0.62	−1.85
2	66.67	33.32	0.03	0.09

VI. Conclusion

The idea of a circuit element, which relates the charge q and the magnetic flux ϕ realizable only at the nanoscale with the ability to remember the past history of charge flow, creates interesting approaches in future CAM-based architectures as we approach the domain of multi-technology hyperintegration where optimization of disparate technologies becomes the new challenge. The scaling of CMOS technology is challenging below 10 nm and thus nanoscale features of the memristor can be significantly exploited. The memristor is thus a strong candidate for tera-bit memory/compare logic.

The non-volatile characteristic and nanoscale geometry of the memristor together with its compatibility with CMOS process technology increases the memory cell packing density, reduces power dissipation and provides for new approaches towards power reduction and management through disabling blocks of MCAM cells without loss of stored data. Our simulation results show that the MCAM approach provides a 45% reduction in silicon area when compared with the SRAM equivalent cell. The Read operation of the MCAM ranges between 5 to 12 ns, for various implementations, and is comparable with current SRAM and DRAM approaches. However the Write operation is significantly longer.

Simulation results indicate a reduction of some 96% in average power dissipation with the MCAM cell. The maximum power reduction is over 74% for the memristor-based structure. The RMS value of current sunk from the supply rail for the MCAM is also approximately 47 μA, which correspond to over a 95% reduction when compared to SRAM-based circuitry. To the best of our knowledge this is the first power consumption analysis of a memristor-based structure that has been presented using a behavioral modeling approach. As the technology is better understood and matures further improvements in performance can be expected

Acknowledgment

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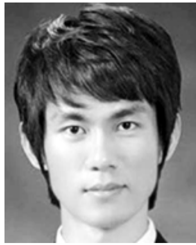

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