Merged Two-Stage Power Converter With Soft Charging Switched-Capacitor Stage in 180 nm CMOS

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***Abstract*—In this paper, we introduce a merged two-stage dc-dc power converter for low-voltage power delivery. By separating the transformation and regulation function of a dc-dc power converter into two stages, both large voltage transformation and high switching frequency can be achieved. We show how the switched-capacitor stage can operate under *soft charging* conditions by suitable control and integration (merging) of the two stages. This mode of operation enables improved efficiency and/or power density in the switched-capacitor stage. A 5-to-1 V, 0.8 W integrated dc-dc converter has been developed in 180 nm CMOS. The converter achieves a peak efficiency of 81%, with a regulation stage switching frequency of 10 MHz.**

***Index Terms*—DC-DC converter, merged two-stage, soft charging, switched capacitor converter, power management, buck converter, feed-forward, CMOS power delivery**

I. Introduction

THE advent of low-voltage digital circuitry has created a need for improved dc-dc converters. Dc-dc converters that can provide a low-voltage output (< 2 V) regulated at high bandwidth, while drawing energy from a higher (5-12 V) input voltage are desirable. In addition, the size, cost, and performance benefits of integration make it advantageous to integrate as much of the dc-dc converter as possible, including control circuits and power switches. Moreover, in some applications it would be desirable - if possible - to integrate the power converter or portions thereof with the load electronics.

One common approach is the use of a switched-mode power converter (e.g. synchronous buck converter, interleaved synchronous buck, three-level buck, and like designs [1]–[8]). For magnetics-based designs operating at low, narrow-range input voltages and moderate conversion ratios, it is possible to achieve extremely high switching frequencies (up to hundreds of MHz [3], [6], [7]), along with correspondingly high control bandwidths and small passive components (e.g., inductors and capacitors). It also becomes possible to integrate portions of the converter with a microprocessor load in some cases. These opportunities arise from the ability to use fast, low-voltage, process-compatible transistors in the power converter. However, at higher input voltages and wider input voltage ranges, much lower switching frequencies (on the order of a few MHz and below) are the norm, due to the need to use slow extended-voltage transistors (on die) or discrete high-voltage transistors. This results in much lower control bandwidth, and large, bulky passive components (especially magnetics) which are not suitable for integration or co-packaging with the devices.

Another conversion approach that has received attention for low-voltage electronics is the use of switched-capacitor (SC) based dc-dc converters [9]–[15]. This family of converters is well-suited for integration and/or co-packaging of passive components with semiconductor devices, because they do not require any magnetic devices (inductors or transformers). A SC circuit consists of a network of switches and capacitors, where the switches are turned on and off periodically to cycle the network through different topological states. Depending on the topology of the network and the number of switches and capacitors, efficient step-up or step-down power conversion can be achieved at different conversion ratios.

There are, however, certain limitations of the SC dc-dc converters that have prohibited their widespread use. Chief among these is the relatively poor output voltage regulation capability for varying input or output voltages. The efficiency of SC converters drops quickly as the conversion ratio moves away from the ideal (rational) ratio of a given topology and operating mode. In fact, in many topologies the output voltage can only be regulated for a narrow range of input voltages while maintaining an acceptable conversion efficiency [11], [12], [16].

One means to partially address these limitations is to cascade a SC converter having a fixed step-down ratio with a low-frequency switching power converter having a wide input voltage range [1] to provide efficient regulation of the output. Other techniques [17], [18] integrate a SC circuit within a buck or boost converter to achieve large conversion ratios. However, the regulation bandwidth of these techniques is still limited by the slow switching of the SC stage.

Another approach that has been employed is to use a SC topology that can provide efficient conversion for multiple specific conversion ratios (under different operating modes) and select the operating mode that gives the output voltage that is closest to the desired voltage for any given input voltage [12], [19]. This technique, while offering increased efficiency, does so at the expense of additional capacitors and transistors, as well as increased control complexity.

None of these approaches are entirely satisfactory in achieving the desired levels of performance and integration. In particular, they do not fully leverage the benefits of integrated circuits and the device characteristics that CMOS IC processes

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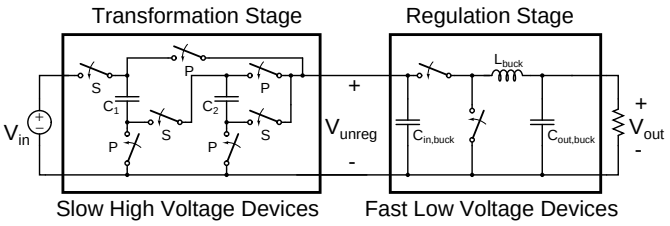
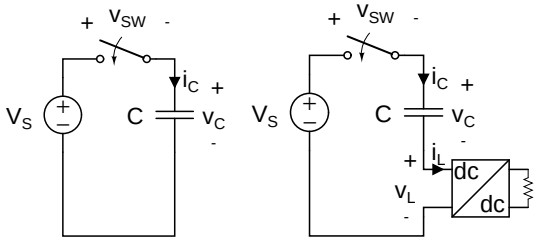


Fig. 1. Block diagram illustrating the two-stage architecture, which enables a single-die power converter providing both large voltage step down and high frequency operation.



(a) Hard charging. (b) Soft charging.

Fig. 2. Simplified circuits for illustrating capacitor charging in a switched capacitor system. (a) Hard charging in a conventional SC system. (b) Soft charging with energy recovery.

provide. The availability of low-voltage high frequency transistors in advanced CMOS processes enables dramatic reduction in passive components size [20], but conventional single-stage designs only achieve this high frequency at low voltage (and hence conversion ratios). The availability of slower, higher-voltage devices (typically used for I/O connections) in the same process offers opportunities to achieve both high voltage step-down *and* high switching frequency, through the use of appropriate circuit topologies. We seek to take advantage of these characteristics of CMOS processes in the architecture presented here.

II. Architecture

Shown in Fig. 1 is a two-stage architecture that combines a high efficiency switched-capacitor (SC) transformation stage with a high-frequency regulation stage. The architecture, first introduced in [20], achieves both large voltage step-down and high bandwidth regulation (owing to the high switching frequency of the regulation stage) across a wide output and input voltage range. The architecture makes use of the transistors typically available in a CMOS process: slow, moderate blocking voltage devices (e.g. thick gate oxide and/or extended drain transistors) and fast, low-voltage transistors. The SC transformation stage, employing slow-switching moderate voltage devices and off-chip capacitors, can be designed for very high power density and efficiency. The intermediate voltage, $V_{\rm unreg}$, can be made sufficiently low such that the regulation stage can utilize low-voltage, fast-switching transistors that enable high switching frequency with correspondingly high bandwidth regulation and small passive components.

The separation of the transformation (step-down) and regulation functionality of the converter into two stages provides substantial advantage: the architecture makes use of the inherent advantages of SC power converters (high voltage step-down, high efficiency), while not tasking it with regulation, which SC converters cannot do efficiently. The regulation functionality is performed by the low-voltage synchronous buck converter, and since that stage operates at low voltage and transformation ratio, it can operate at high frequency with small magnetics size. As was shown in [20], substantial advantages in terms of size and efficiency can be realized by employing highly scaled CMOS transistors in switched-mode power converters.

A. Soft Charging

The architecture of Fig. 1 can provide yet another attractive benefit if designed and operated in a specific manner ("merging" of the two stages). In this case, the regulation stage can provide *soft charging* of the SC stage, a mode of operation that provides increased efficiency and power density of the SC converter as compared to conventional designs. In a conventional SC power converter, the capacitor size and switching frequency are constrained by the requirement to keep the voltage ripple of the capacitors low to achieve high efficiency [15]. This constraint restricts the designer of SC power converters to either use large capacitors (with corresponding low power density) or operate at a high switching frequency (with attendant increases in switching losses). For a given switch and capacitor technology implementation, conventional SC dc-dc converters are thus limited in terms of their achievable power density and efficiency. Soft charging operation, however, enables an increased capacitor ripple while maintaining low-loss operation.

The circuits shown in Fig. 2 help illustrate the loss mechanism in SC dc-dc power converters, and the role that soft charging can play to decrease power losses. Fig. 2a shows an example of hard charging (sometimes also referred to as impulse charging), which happens at each switching interval in conventional SC converters. The capacitor (representing a "stack" of capacitors in an actual SC circuit) has an initial voltage of $V_C(t<0) = V_S - \Delta V$, and the switch is closed at time $t = 0$. After a sufficiently long time, the capacitor voltage will charge up to V_S. During the charging period, however, $\frac{1}{2}C(\Delta V)^2$ of energy is dissipated as heat in the switch resistance. It should be noted that this energy dissipation is independent of the value of switch resistance, and cannot be reduced by employing a switch with lower on-state resistance. In order to reduce the power loss in conventional SC power converters, one typically attempts to minimize ΔV, either by using large capacitors or by operating at high switching frequency. In doing so, the capacitors are not utilized well from an energy storage perspective, as the ratio of energy transferred in a cycle to energy stored in each capacitor is kept low.

The circuit of Fig. 2b illustrates the soft charging concept. In this circuit, a dc-dc converter is placed in series with the voltage source and capacitor. The dc-dc converter is designed to operate at a much higher switching frequency than the

SC stage, so that it appears as a constant power load. The system is designed such that during charging, the majority of the voltage difference between the capacitor and the voltage source appears across the input of the dc-dc converter, instead of the switch resistance, reducing the $\frac{1}{2}C(\Delta V)^2$ energy that would be lost in the hard charging circuit. With the soft charging technique, rather than being dissipated as heat in the resistive elements, the majority of the energy is captured and transferred to the output of the dc-dc converter where it provides useful work. The important thing to note is that a SC converter operating with soft charging is no longer restricted to keep the capacitor voltage ripple small for efficiency reasons, and can more effectively utilize the energy stored on the capacitors (enabling reduced switching frequency or capacitor size).

In the circuit of Fig. 1, the high frequency regulation stage (a synchronous buck converter) provides soft charging for the series-parallel SC transformation stage. When the SC stage is configured to charge capacitors C_1 and C_2 in series (switches S closed), the capacitors are charged at a rate determined by the power drawn from the regulating stage, ensuring soft charging operation. When the SC stage is configured to discharge C_1 and C_2 in parallel (switches P closed), the capacitor voltages appear directly across the input terminal of the regulating stage, providing soft discharging of the capacitors. It should be noted that the input capacitor of the buck converter, $C_{in,buck}$ is considerably smaller than C_1 and C_2, as it serves only to filter the high frequency ripple of the buck converter.

Another advantage of the the soft charging architecture is that the number of capacitors in the SC stage can be reduced from N to N-1 for an N-to-1 step-down topology. In the 3-to-1 transformation stage of Fig. 1, only two capacitors (C_1 and C_2) are used in the SC stage, compared to the three capacitors typically required in a conventional 3-to-1 series-parallel SC converter (note, however, that the much smaller input capacitor of the regulation stage is still required, as discussed above). The proposed architecture thus enables a reduction in overall capacitance of the SC stage, both through the elimination of one capacitor, and by the ability to operate the remaining capacitors at increased voltage ripple.

III. Control

In this section, we present soft charging control techniques suitable for implementation in a CMOS process.

A. Control of Switched-Capacitor Output Voltage

Conventional SC power converters are often controlled with a simple two-phase clock to alternate between two switch configurations. The soft charging technique presented in this work exploits a more sophisticated control implementation to ensure that the SC output voltage stays within a suitable range. Fig. 3 shows a hysteretic control strategy that ensures that the input voltage to the regulation stage (V_{unreg}) is maintained below a maximum value (V_{max}). The value of V_{max} is chosen to be below the maximum operating voltage of the (low-voltage) transistors of the regulation stage. The two reference

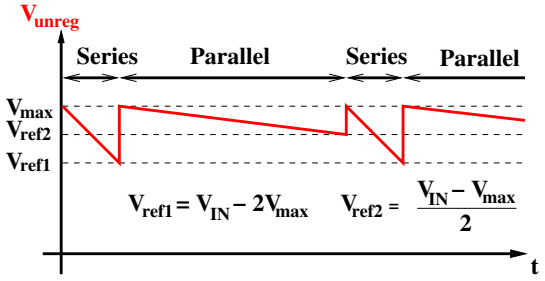


Fig. 3. Idealized waveforms illustrating the switched-capacitor control strategy. This approach maintains the SC stage output voltage below V_{max}, thus enabling the use of low-voltage devices in the regulation stage.

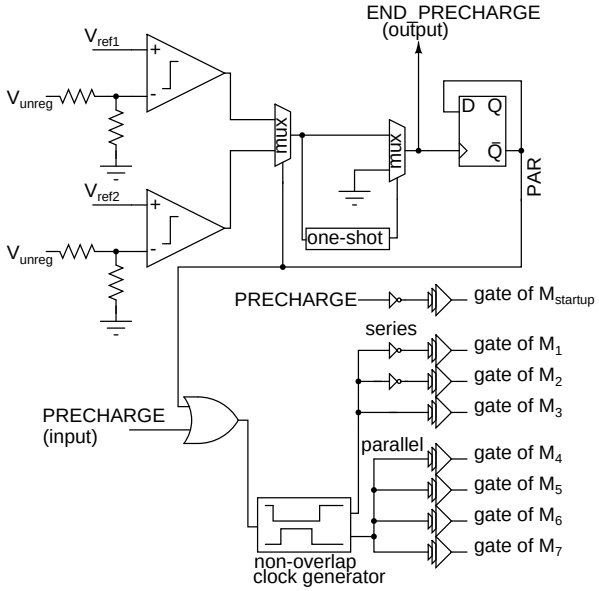


Fig. 4. Schematic drawing of the SC stage control implementation.

voltages V_{ref1} and V_{ref2} can be derived from the input voltage V_{IN} and V_{max}, as shown below:

$$V_{ref1} = V_{IN} - 2V_{max} \tag{1}$$

$$V_{ref2} = \frac{V_{IN} - V_{max}}{2} \tag{2}$$

A schematic drawing of the control circuitry is shown in Fig. 4. The two different reference voltages (V_{ref1} and V_{ref2}) are provided from an off-chip source in this implementation, to allow flexibility in the characterization of the control technique. Reference [21] contains a detailed description and analysis of many of the circuit blocks of Fig. 4, including the comparators.

A flip-flop is used to keep state of the operation mode (series or parallel), and the inverted output controls a multiplexer such that the corresponding comparator output is used to trigger a change in series-parallel operation. The one-shot circuitry (with details provide in Figure 5) is used to introduce a blanking time immediately following a comparator transition. This is added as a safeguard against any oscillations caused by the other comparator. Without the blanking period, a high output of the other comparator could be propagated to the flip-flop when the multiplexer changes. The blanking period

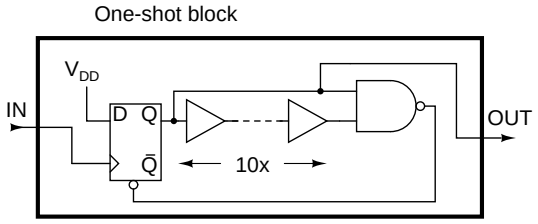


Fig. 5. Schematic drawing of the one-shot circuitry used in Figure 4. The one-shot circuit is used to introduce a blank-out period when the output of the comparator is not propagated to the rest of the control circuit.

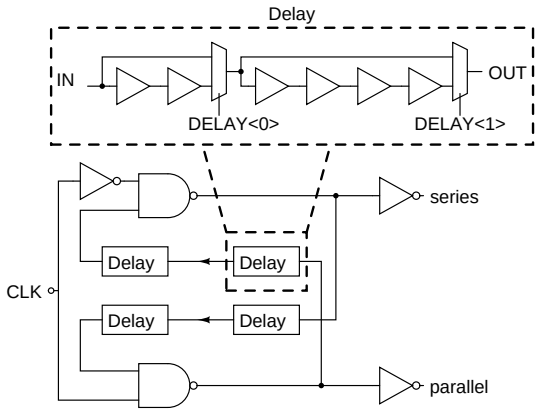


Fig. 6. Schematic drawing of the non-overlap generator with 2-bit programmable delay.

is chosen to be long enough to prevent this from accidentally happen (based on simulation), and must not be so long that it interferes with the correct switching operation (i.e. must be significantly shorter than a switching period of the SC stage).

Finally, a programmable non-overlap generator (shown in Figure 6) is used to ensure that there is sufficient dead-time between the transitions between series and parallel modes. All the control circuitry was implemented using low-voltage 180 nm transistors, while the final tapered gate drivers (shown in Fig. 7) employed high voltage devices. The choice of tapering factor was determined through simulation, where the objective is to minimize overall loss by trading off device switching loss and gate drive power consumption. The transistors corresponding to the output of the tapered gate drivers are shown in the schematic drawing of Figure 8. Note that two of the SC power stage transistors (M_1 and M_2) are implemented as PMOS devices, and therefore requires inverted gate drive signals.

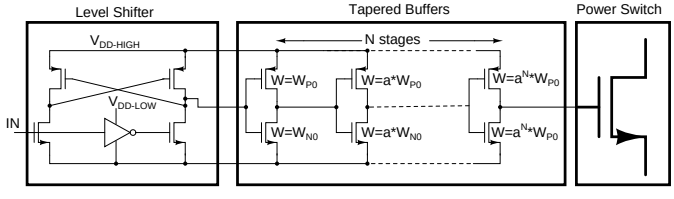


Fig. 7. Tapered gate drive circuit with a tapering factor of a (a=10 in this design). The level shifter interfaces the low-voltage control circuitry to the higher gate drive voltage. The implemented design uses N = 6 buffer stages.

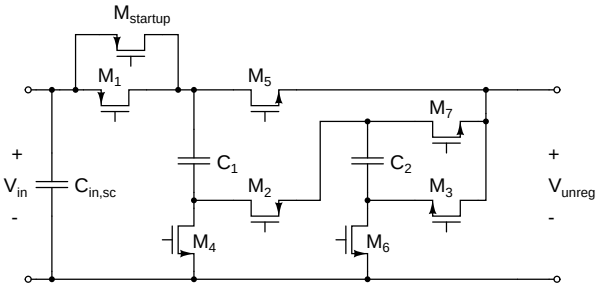


Fig. 8. Schematic drawing of switched-capacitor transformation stage. The capacitors are off-chip, and the transistors are 5 V triple-well thick-oxide devices available in the 180 nm CMOS process.

B. Startup of the Switched-Capacitor Stage

A key challenge in switched-capacitor converters is the issue of startup conditions. While it is true that the individual transistors and capacitors in a SC converter typically only see fractions of the input voltage in steady-state operation, large voltage stresses can develop across individual components during startup. In the merged two-stage converter, it is therefore critical to implement a startup sequence that ensures that the voltage across all transistors and capacitors remain below their rated voltage.

Since the switched-capacitor transistors and capacitors are all rated for a voltage higher than (or equal to) the input voltage, the critical voltage that must be controlled is the output voltage of the SC stage (V_{unreg}), which is connected to the low (2 V) devices of the regulation stage. It can be seen from Figure 8 that if capacitors C_1 and C_2 have no charge (which will be the case if V_{in} has been kept low for some time), and the SC stage is configured to operate in series mode (M_1, M_2, M_3 closed), the full input voltage (5 V) appears across the output terminals of the SC stage. Since these terminals are also connected to the input of the low-voltage (2 V) devices of the regulation stage (as shown in Fig. 1), care must be taken to never allow $\mathrm{V_{unreg}}$ to go above 2 V.

Shown in Figure 9 is a schematic drawing of the startup circuitry. The circuit employs a comparator that compares the output voltage of the SC stage (V_{unreg}) to a reference voltage ($V_{\mathrm{ref-startup}}$), which is lower than V_{ref1} and V_{ref2}. The AND logic block is used together with a slow clock to ensure that the the flip-flop will indeed trigger when the startup is detected. Since the flip-flop is of the edge-detect type, there could be a situation at startup where the comparator output is not detected if the flip-flop is not properly initialized before the signal arrives at the clock input. The slow clock and the AND block ensures that once the comparator has detected an under-voltage situation, this information will be captured by the flip-flop. Finally, the multiplexer is used together with an SC-ENABLE signal to ensure that the pre-charge signal is not initiated when the SC stage is not enabled.

The pre-charge signal is applied to the startup transistor (M_{startup}, as shown in Figures 4 and 8), which has a gate width many times smaller than the other power transistors. The pre-charge signal is also driving the input node of the non-overlap clock generator high (through the OR block, as

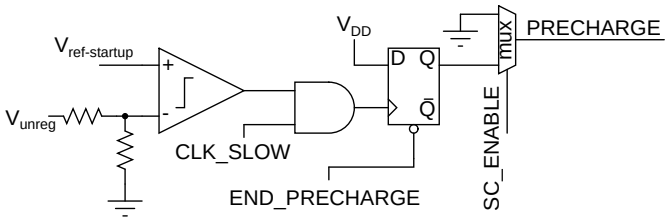


Fig. 9. Schematic drawing of the SC startup control circuitry. At startup, this control circuitry ensures that no node voltages exceed the ratings of the on-chip transistors.

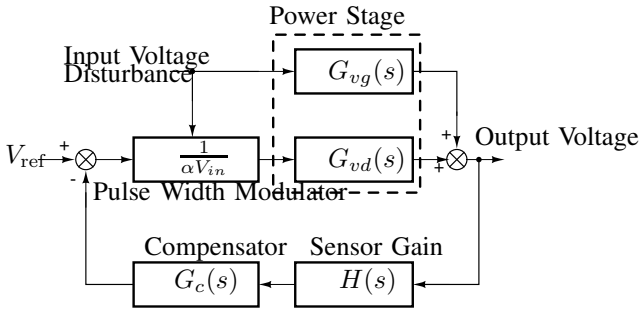


Fig. 10. Block diagram illustrating the feed-forward control used in the system. The gain of the PWM block is inversely proportional to the input voltage, enabling cycle-by-cycle feed-forward control with fast response.

seen in Figure 4). This ensures that the SC stage remains in parallel mode while the pre-charge signal is high. Transistors M_4, M_5, M_6 and M_7 are thus on, and the output node V_{unreg} is slowly brought up from zero volts through the transistor M_{startup}.

The pre-charge phase is turned-off by the END-PRECHARGE command from the circuit of Figure 4, which goes high once the voltage V_{unreg} is high enough to trip one of the other two comparators. At this point, the control circuitry transitions to two-level hysteretic control of the SC stage. The advantage of this startup scheme is that it only requires one additional (small) power transistor, and a few additional analog and digital blocks. In regular operation, the M_{startup} transistor is not used, and does not incur any additional loss, as compared to some other series-connected startup schemes in the literature [22].

C. Regulation Stage Control

While the SC stage operates with significant output voltage ripple (as seen in Fig. 3), the frequency of this ripple is substantially lower than the control bandwidth of the regulation stage (this is possible because the switching frequency of the regulation stage is many times higher than the switching frequency of the SC stage). However, the transitions at the switching intervals nevertheless present a problem to a regular feedback controller, and the sharp edges can appear at the output (audio susceptibility). In order to maintain the output voltage steady despite the sharp voltage transitions at its input terminals, the regulation stage employs feed-forward control, as shown in the block diagram of Fig. 10.

In this implementation, the pulse width modulator gain is inversely proportional to the input voltage, rather than fixed,

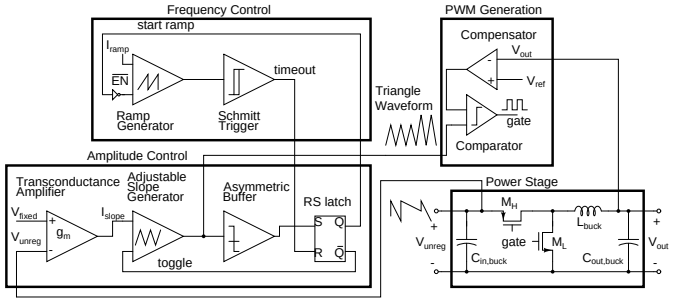


Fig. 11. Schematic block diagram illustrating the feed-forward control implementation. The height of the triangle waveform is proportional to the regulation stage input voltage (V_{unreg}).

as is done in conventional feedback-only control. The effect of this change is that any input voltage disturbance that is propagated from the input to the output through the line-to-output transfer function $G_{vs}(s)$ can be cancelled by an immediate change in the input to the control-to-output transfer function $G_{vd}(s)$ [23].

A schematic drawing illustrating the implementation of the feed-forward control is shown in Fig. 11. The feed-forward control is accomplished by making the amplitude of the triangle wave reference of the comparator in the PWM block proportional to the buck converter input voltage (V_{unreg}). With this method, any sharp edges in the input voltage will immediately appear as an increased triangle amplitude at the input of the comparator, which controls the PWM signal to the gate. The overall feedback loop (controlled by the compensation network of the error amplifier) can still be kept slow enough to ensure stability, while the response of the feed-forward control can be made very fast, and is only limited by the speed of the transconductance amplifier which controls the triangle waveform amplitude. The feed-forward circuitry of Fig 11 was implemented on-die, using 180 nm core transistors and on-chip capacitors and resistors for compensation networks, and off-chip controllable bias currents to accommodate a wide switching frequency range of the regulation stage, as well as enabling fine-tuning of the feed-forward compensation.

Detailed descriptions of the design and implementation of the circuit blocks of Fig. 11 are provided in [21]. Here we provide schematic drawings of a few key components of Fig. 11, and refer readers interested in more detailed descriptions to [21]. Shown in Fig. 12 is a schematic drawing of the transconductance amplifier and adjustable slope generator of Fig. 11. The transconductance amplifier generates an output current that is directly proportional to the regulation stage input voltage (V_{unreg}). This current sets the charge and discharge current of the capacitor C_T through a current-starved inverter in the adjustable slope generator. In this manner, the slope of the generated triangle-waveform is directly proportional to V_{unreg}.

Shown in Fig. 13 is the circuit components responsible for ensuring that the variable-amplitude triangle wave remains at a a fixed frequency. It comprises a current-controlled ramp generator and a Schmitt trigger, which resets the latch of Fig. 11, thereby toggling the triangle waveform generator to

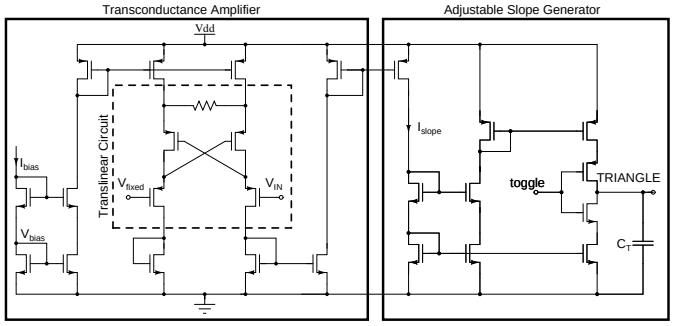


Fig. 12. Schematic drawing of the transconductance amplifier and adjustable slope generator. The transconductance amplifier circuit consists of a cascode input current mirror, and a translinear circuit that creates a differential current that is proportional to the differential voltage on the PMOS input transistors. A part of this current is used to drive the current-starved inverter that charges and discharges a capacitor in the adjustable slope generator.

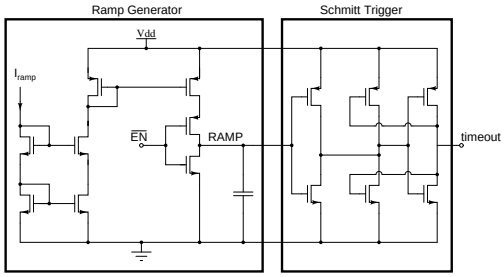


Fig. 13. Frequency Control: A resettable ramp generator and a Schmitt trigger are used to control the switching frequency of the buck converter. The bias current I_{ramp} is provided from off-chip.

switch direction. The frequency of the regulation stage is thus set by $I_{\rm ramp}$, which in our implementation was provided from an off-chip source to enable a wide range of operating frequencies for testing and characterization.

It should be noted that as regards output voltage regulation, the relevant dynamics of the system are effectively those of the buck converter stage alone (i.e., those of the second stage only), as the buck stage control naturally rejects the variations at its input. This fact leads to a substantial advantage over conventional step-down converters, for two reasons. First, because the second stage operates at low voltage, it can utilize a much higher switching frequency than could a single-stage converter operating from the high-voltage input. This directly provides a much higher achievable control bandwidth (which is proportional to switching frequency). Secondly, the achievable overall response speed in a buck converter is best near 2:1 voltage conversion and declines for higher conversion ratios [24]. The second stage operates at much closer to a 2:1 ratio than would a buck converter operating directly from high voltage, enabling further improvements in response speed.

IV. CMOS Implementation

The soft charging two-stage architecture of Fig 1 with the control circuitry described in Section III has been implemented in a 180 nm CMOS process (CMOS9T5V from National Semiconductor). Table I lists the specifications of the converter.

The transistors in the SC stage (as shown in Fig. 8) are 5 V isolated triple-well thick-oxide devices with extended drain

TABLE I
Converter Specifications

Input Voltage Range	4.0-5.5 V
Output Voltage Range	0.8-1.3 V
Output Power Range	0.3-0.8 W
SC Switching Frequency	2-100 kHz (load dependent)
Buck Switching Frequency	10 MHz
Peak Efficiency	81%
Line Regulation (V_{out}=1.0 V)	2 mV/V
Load Regulation (V_{out}=1.0 V)	6 mV/A

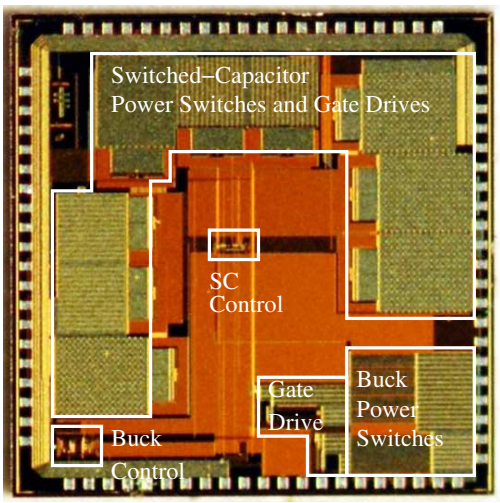


Fig. 14. Die photograph of the converter implemented in 180 nm CMOS technology. The total die area is 3.6x3.6 mm, although much of that area is not used. An approximate die-are breakdown is provided in Table II.

regions. It should be noted that in soft charging operation, the conventional methods of sizing the SC stage transistors should not be used. Since the charging loss is negligible in our proposed architecture, the two main switch loss mechanisms are conduction loss and gating loss. The sizing of the SC transistors thus involves a careful balance between these two loss mechanisms, which can be optimized through mathematical modeling and simulation, for a given capacitor size and desired ripple [21]. The capacitors C_1 and C_2 are 4 V 22 μF off-chip ceramic (X5R) capacitors in an 0603 package. The transistor $\rm M_{startup}$ is activated during start-up (by the on-chip control circuitry) to ensure that the SC output voltage never rises above 2 V (the maximum working voltage of the regulation stage transistors) by slowly charging capacitors C_1 and C_2. During regular operation, $\rm M_{startup}$ remains off.

Shown in Fig. 14 is an annotated die photo of the converter. It can be seen that the majority of the die area is taken up by the SC power transistors, as they are high voltage devices switching at low frequency. It should be noted that the design was not optimized for die area but was instead driven by the required number of I/O pins for power delivery, control, and testing. This resulted in a IC package size that was larger than the required active die area of the converter. Table II provides an listing of the approximate area occupied by the different circuit blocks outlined in Fig 14.

TABLE II
CONVERTER AREA BREAKDOWN

Circuit Block	Area [mm^2]
SC Power Switches	3.78
SC Gate Drives	1.62
SC Control	0.01
Buck Power Switches	0.41
Buck Gate Drivers	0.30
Buck Control	0.03
Decoupling Capacitance (oversized)	3.00
$C_{in,buck}$ (on-die)	0.50
Total Used Die Area	9.65

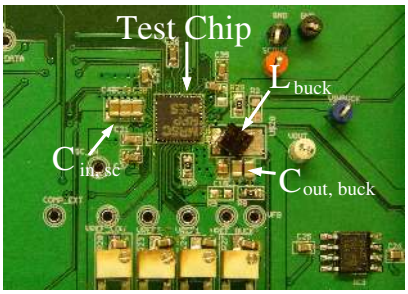


Fig. 15. Photograph of merged two-stage test chip mounted on PCB, along withi top-side passive components. Some capacitors were placed on the bottom side to minimize inductance.

The 10 MHz regulation stage switching frequency enables the use of a very small output inductor (28 nH mini-spring Coilcraft air-core) and capacitors (2 and 4.7 μF 4 V X5R capacitors for $C_{in,buck}$ and $C_{out,buck}$, respectively). A photograph of the experimental PCB and external components is shown in Fig. 15. Note that $C_{in,buck}$, C_1 and C_2 are placed on the bottom side of the PCB to minimize stray inductance, and are thus not shown.

V. EXPERIMENTAL RESULTS

Shown in Fig. 16 are steady-state experimental waveforms of the converter. The input voltage in this plot is 5 V, and the output is regulated to 1 V, with a load resistance of 5 Ω. Note that despite the large voltage ripple (more than 200 mV) at the input of the regulation stage (V_{unreg}), the feed-forward control maintains the output voltage with a ripple of less than 75 mV. It should be noted that the ripple is dominated by the spurs associated with the switching of the SC stage. There are a number of ways to further reduce this ripple if desired. One method is to improve the feed-forward control, either through more careful tuning of the circuit employed here, or by implemenation of current-mode control, which provides cycle-by-cycle attenuation of input voltage ripple. Increased regulation stage switching frequency (and corresponding control bandwidth) would also help mitigate this ripple, as would a larger output capacitor. A more subtle method to reduce the ripple is to operate the SC stage with less voltage swing on the capacitors to begin with. This would require larger SC stage capacitors (for a given power level), so careful considerations of this trade-off must be made at design time.

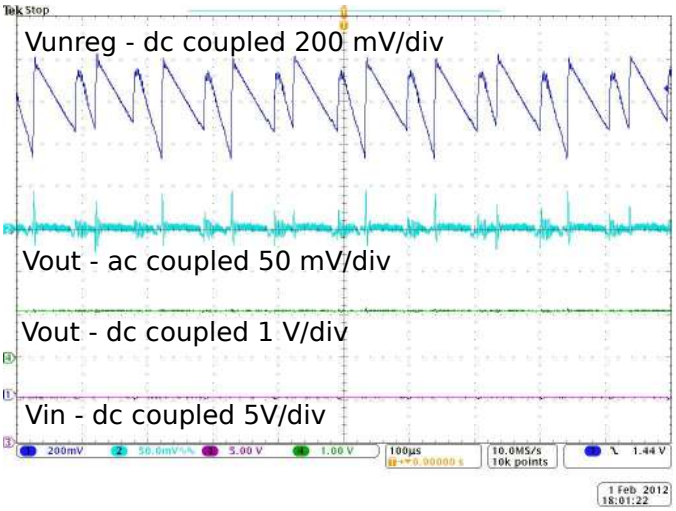


Fig. 16. Experimental waveforms showing converter operation. Note that the input voltage is 5 V, and the output voltage is steady at 1 V, despite the large voltage swings at the input of the buck converter (V_{unreg}).

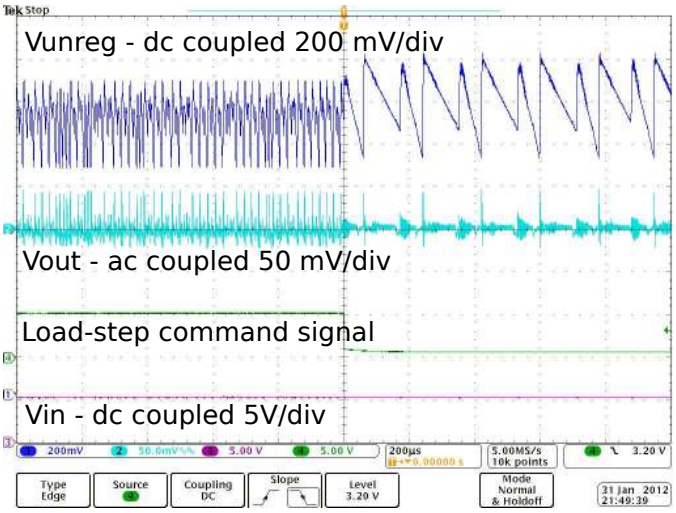


Fig. 17. Experimental waveforms showing the converter response to a load-step between 90 and 10% of full load.

Fig. 17 shows transient waveforms of the converter when the load is stepped between 90 and 10 % of full load. The output voltage remains steady, and the light-load operation of the SC stage is apparent in the V_{unreg} waveform, which shows low switching frequency at light load, and increased switching frequency at heavy load. Shown in Fig. 18 is a zoomed in version of Fig. 17 to illustrate the bandwidth of the step response.

Measured efficiency for a few different output voltages are shown in Fig. 19. The efficiency measurement includes all power losses associated with the control circuitry, all gating losses, as well as packaging and bond-wire losses. The decrease in efficiency at low input power is almost entirely due to the regulation stage, which was operated at a fixed frequency (10 MHz) at all times. Although we did not implement it in this prototype, it should be noted that in general, efficiency

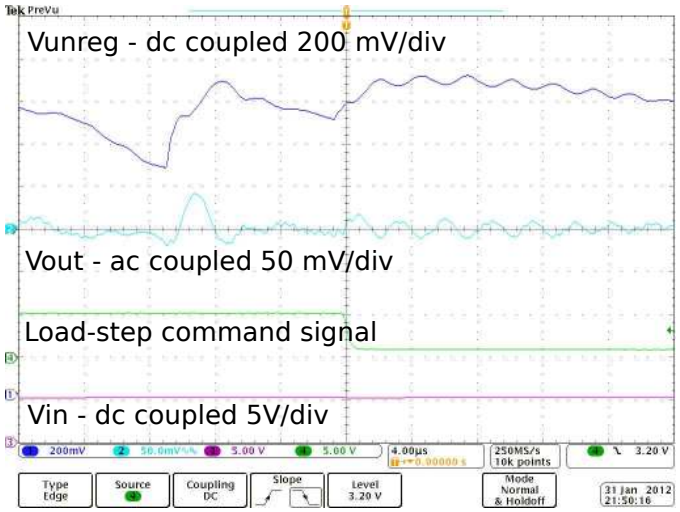


Fig. 18. Zoomed in transient load-step of Fig. 17.

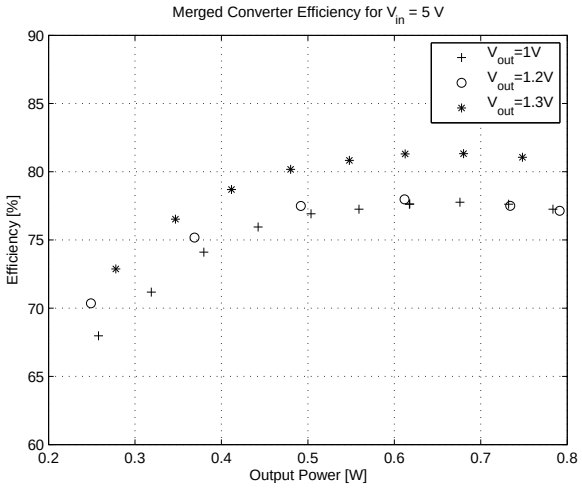


Fig. 19. Plot showing measured efficiency for the prototype merged two-stage converter across output power range. All control and gate drive losses are included in the efficiency measurement. In this prototype, the regulation stage is operating in PWM mode at all times, which results in low efficiency at light load. There are well-known techniques (such as PFM) that can improve the light-load performance, which can be implemented in the regulation stage if so desired.

at low power levels can be increased with suitable light-load control schemes such as pulse-frequency modulation (PFM), if desired. The SC stage is inherently light-load efficient due to the hysteretic controller, which automatically operates at a lower switching frequency at low output power.

Table III shows an estimated breakdown of losses. A significant portion of the losses come from bond-wire resistance and on-chip metallization resistance, owing to the package used. There are well-known techniques to mitigate these losses (e.g thick top layer metallization, flip-chip technology). It is therefore expected that the overall converter efficiency can be significantly improved through appropriate packaging techniques. In this implementation, we estimate that an overall efficiency of 92% could have been achieved if it were not for packaging limitations.

Shown in Fig 20 is the measured efficiency of the merged

TABLE III
ESTIMATED CONVERTER LOSS BREAKDOWN AT P_{out}=0.8 W

Bond-wire conduction loss	60 mW
Transistor gating loss	45 mW
On-die metallization conduction loss	40 mW
Transistor conduction loss	11 mW
Inductor loss	5 mW
Control losses	2 mW

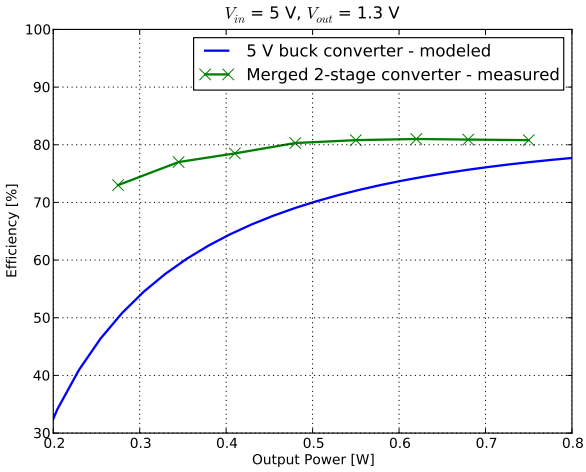


Fig. 20. Plot showing experimentally measured efficiency for the prototype merged two-stage converter compared to modelled efficiency of a single-stage 5-to-1 V buck converter using transistors from the same process.

two-stage converter together with *modeled* efficiency for a single-stage buck converter operating at 10 MHz. The single-stage buck converter is modelled with the same 5 V devices (and attendant packaging losses) that were used in the SC stage, and provides a benchmark for comparison. The area of the power switches only (i.e. no decoupling or filter capacitors, control, gate driver, etc.) is approximately 0.52 mm^2 for the modeled single-stage buck converter. A single-stage buck converter would thus occupy less die area than our solution, but incurr higher loss at this operating frequency.

It should also be noted that only gate drive and conduction losses (including packaging) were modelled, and that an experimental implementation would likely see an even lower measured efficiency than what is shown in Fig 20, owing to additional control and switching losses of the single-stage buck converter. Moreover, while a switching frequency of 10 MHz is approaching the practical limit of a single-stage 5-to-1 V buck converter, the merged two-stage converter can be operated at even higher switching frequencies without difficulty, owing to its use of low-voltage devices in the regulation stage.

Table IV shows a comparative listing of some previous work in this space. The presented converter achieves the largest voltage step-down ratio, while operating at one order of magnitude higher switching frequency than many of the other converters. As discussed previously, owing to the packaging limitations our efficiency is lower than desired, but still within

a acceptable range for the application, and higher than a single buck converter stage at the same frequency would achieve. We are therefore hopeful that with improvements in packaging and further refinement of the design, the merged two-stage architecture will enable further increases in frequency and voltage step-down, as well as high conversion efficiency.

VI. Conclusion

We have presented a merged two-stage power converter architecture that offers both large voltage step-down and high frequency operation by making full use of integrated CMOS devices. The proposed architecture enables *soft charging* of the SC stage, a technique that captures the energy normally lost in each switching cycle of SC converters. This technique enables a reduction of the capacitor sizes in the SC converter by more effectively utilizing the energy storage capabilities of the capacitors (through operation at a high capacitor voltage ripple).

We have presented suitable control techniques to ensure safe operation of the converter both in steady state and during startup, as well as for transient load changes. In addition, we have developed feed-forward control techniques that provide high bandwidth, low ripple regulation of the output voltage. These control techniques have been implemented in a design in a 180 nm CMOS process, and verified experimentally.

Experimental measurements show good efficiency and stable operation, as well as fast transient response in the face of load steps. It is worth noting that the conversion efficiency in our experimental prototype is limited primarily by packaging losses, which can be greatly reduced by employing a more suitable packaging implementation. Furthermore, we show, by way of comparison to a modeled single-stage buck converter implementation with the same operating conditions, that the two-stage architecture provides improved efficiency at a switching frequency of 10 MHz. The more important result, however, is that compared to a single-stage topology, the two-stage architecture that we have presented scales well to significantly higher switching frequencies than what was demonstrated here. Consequently, we expect the benefits in terms of size and efficiency of our proposed architecture to be even more apparent as higher switching frequencies are pursued.

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TABLE IV
PERFORMANCE COMPARISON

Reference	[25]	[26]	[27]	[28]	[29]	**This work**
Year	2011	2004	2004	1997	2012	
Topology	Buck	Cascaded Buck	Buck	Cascaded buck	Cascaded buck	Merged two-stage
Technology	0.35 μm	0.25 μm	0.6 μm	0.15 μm	0.35 μm	0.18 μm
Input Voltage	2.7-4.2 V	2.8-5.5 V	3-5.2 V	3.3 V	2.5-5 V	4.0-5.5 V
Output Voltage	2.4 V	1.0-1.8	V_{in} - 0.2 V	1.65 V	1.0-1.8 V	0.8-1.3 V
Switching Frequency	5 MHz	0.5-1.5 MHz	300 kHz-1 MHz	12.8 MHz	1.3 MHz	10 MHz
Efficiency (η_{peak})	91 %	92%	89.5%	75%	94%	81%
Voltage step-down at η_{peak}	3.3 V to 2.4 V	4 V to 1.5 V	3.6 V to 2.0 V	3.3 V to 1.65 V	2.5 V to 1.8 V	5.0 V to 1.3 V
Output power	0.12 W to 1.2 W	0.15 mW to 0.6 W	0.1 W to 0.8 W	8.25 mW to 82.5 mW	18 mW to 0.675 W	0.3W to 0.8 W

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