Merits of Heat Assist for Melt Laser Annealing

Kentaro Shibahara, *Senior Member, IEEE*, Takanori Eto, and Ken-ichi Kurobe

***Abstract*—In this paper, the potential for sub-10-nm junction formation of partial-melt laser annealing (PMLA), which is a combination of solid-phase regrowth and heat-assisted laser annealing (HALA), is demonstrated. HALA and PMLA are effective for reducing laser-energy density for dopant activation and for improving heating uniformity of device structure. The absence of melting at the dopant profile tail for PMLA results in a negligibly small diffusion at this region. A high activation rate is achievable by melting the upper part of the amorphous-silicon layer. The obtained sheet resistance of 10-nm-deep junctions was about 700 Ω/sq. for both n^+/p and p^+/n junctions. These results imply that PMLA is applicable for much shallower junction formation.**

***Index Terms*—CMOS, excimer laser, krypton flouride (KrF), laser annealing (LA), shallow junction.**

I. Introduction

POSTSPIKE annealing methods, such as flash-lamp annealing [1]–[3], solid-phase regrowth [4], and laser annealing (LA) [5], are currently being actively investigated for the scaling of source and drain (S/D) junction depth and MOSFET performance improvements. In terms of LA, laser spike annealing (LSA), which is milli- to microseconds annealing realized with continuous wave (CW) laser irradiation and very fast stage scanning, was recently reported to be promising for the 45-nm node [6]. However, LA with a pulse laser is also a candidate. There are many schemes for pulse LA. We previously reported heat-assisted LA (HALA) [7], [8], which is a combination of substrate heating and laser irradiation, showing 20-nm-deep ultrashallow Sb-doped junction formation. The heat assist at around 450–525 °C led to good dopant activation with a relatively wide process window against laser-energy density (E_L) and the heat-assist temperature.

There are several methodologies for LA besides HALA. LA is often classified as melt or nonmelt; melt-annealing accompanies surface Si melting, whereas nonmelt does not. Melt annealing is generally superior to nonmelt annealing in terms of sheet resistance, since the dopant in a recrystallized region from the melt phase shows a high dopant activation rate. Surface melting also leads to a boxlike dopant depth profile due to very fast dopant diffusion in the liquid phase. Therefore, the adjustment of melt depth is a key to controlling the junction depth (X_j) with melt-type LA. Laser thermal processing (LTP) is one of the most famous approaches for coping with this problem [5], [9]. LTP utilizes melting of an amorphous-silicon (a-Si) layer that was formed by Ge^+ or Si^+ preamorphization implantation (PAI). Because of a 300-°C difference between the melting points of a-Si and crystalline silicon (c-Si), laser irradiation that leads to melting of a-Si is only obtainable by adjusting the laser-energy density. In this case, junction depth is nearly equal to a-Si thickness and is controllable by PAI energy. Thus, methodologies to improve LA as an independent Si process technology has also been discussed. However, there are other aspects such as equipment design and integration to device fabrication.

In this paper, the advantage of HALA will be discussed comparing with LTP and LA with a TiN light absorber. The reduction of laser-energy density and improvement in side effects will be described. Next, a new methodology for LA, partial-melt LA (PMLA), will be proposed based on the experimental results obtained through the HALA investigation. To demonstrate the excellent potential of this new scheme for ultimately shallow junction formation, 10-nm-deep junctions with negligibly small diffusion were fabricated.

II. Experimental Conditions

A krypton flouride (KrF) excimer laser with a wavelength of 248 nm was used for HALA and PMLA. The full-width at half-maximum (FWHM) of the laser pulse was 38 ns. The laser-irradiation area was 4×4 mm^2. Si wafers were heated prior to laser irradiation and maintained at 450 or 525 °C during irradiation. The average heating time before irradiation was 5 min, and the annealing atmosphere was nitrogen. Sb and B were used as dopants. Si (100) wafers whose resistivity was 5–10 Ω · cm were used as substrates. For the 10-nm junction formation, after preamorphization with 3-keV Ge^+ implantation, 3.5-keV Sb^+ or 0.3-keV B^+ was implanted. No screen oxide was formed prior to the implantation steps in these cases. The implantation doses for preamorphization Ge^+, Sb^+, and B^+ were 1×10^{15}, 6×10^{14}, and 1×10^{15} cm^{-2}, respectively, and the amorphization depth was approximately 11 nm. Sheet resistance after annealing was evaluated with the four-point probe method.

III. Fundamental Merits of HALA

For pulse LA, die-by-die laser irradiation is the most desirable method for processing large-diameter wafers. The laser equipment used in our experiments outputs 1 J/pulse, which is much larger energy than ordinary excimer lasers used for lithography. Assuming the die size is 2 cm by 2 cm and there is no optical loss, the applicable maximum E_L with a 1-J pulse is calculated to be 250 mJ/cm^2. This value is too low considering our previous result that more than 600 mJ/cm^2 was needed

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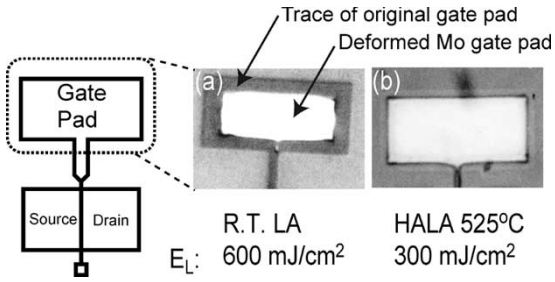

Fig. 1. Plan-view optical microphotographs of Mo gate pad after laser irradiation. Mo gate electrode shows deformation for: (a) non-heat-assisted case; (b) heat assist at 525 °C, which effectively suppressed the deformation. Although E_L for (b) is smaller than that for (a), the sheet resistances of the annealed junctions were nearly equal.

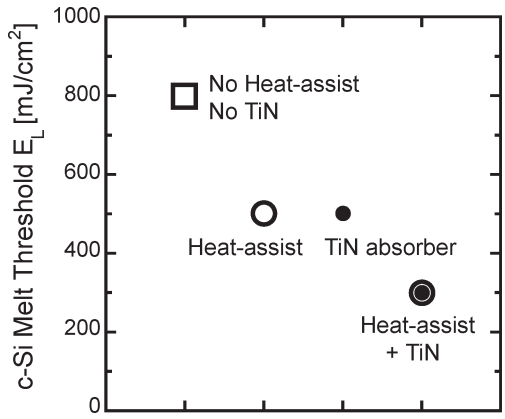

Fig. 2. Comparison threshold E_L for c-Si melting for various LA schemes. Although the threshold E_L is too high to form shallow junctions, the effects of heat assist and the TiN light absorber for E_L reduction are clearly indicated by this index.

to obtain a low-enough sheet resistance [10]. Thus, to obtain a large-enough irradiation area, E_L reduction is demanded. HALA is useful for such a purpose. In the case of ordinary LA, laser energy is converted to thermal energy and dissipated to heat up the substrate surface. Therefore, the necessary laser energy is a monotonic function of difference between the initial substrate temperature and the process temperature. Raising the initial substrate temperature by the heat assist naturally reduces the necessary E_L to heat up specimens to the target temperature. In truth, 300 mJ/cm^2 was enough to obtain a low-resistive 20-nm-depth Sb-doped junction with the heat assist of 450 °C [7], [8].

E_L reduction by HALA is also effective for improving heating uniformity. It is often degraded by light interference in thin films and patterned structures or by nonuniformity in heat conductivity in device structures. HALA can relieve the latter. As described above, the introduction of heat assist decreases the contribution of laser heating against total heating. Therefore, heat assist is expected to be effective for improving the uniformity. Fig. 1(a) shows an example of nonuniform heating by laser irradiation; an Mo gate, whose thickness was 50 nm, was formed after local oxidataion of silicon (LOCOS) formation. Irradiation of 600 mJ/cm^2 was carried out without heat assist. A selective a-Si melt, in other words LTP, occurs under this condition [7], [8], and [10]. The gate electrode on the active regions did not suffer from deformation. However, the gate pad located on a thick field oxide deformed by melting, as shown in Fig. 1(a), since the temperature for the gate pad was much higher than that for the gate electrode because of poor heat conduction through the field oxide. On the contrary, the gate pad after HALA did not show deformation, as shown in Fig. 1(b), in spite of the fact that E_L of 300 mJ/cm^2 was sufficiently high to melt a-Si. Thus, heat assist is helpful for improving the adaptability of LA for the device-fabrication process.

The use of a light absorber is another approach for the E_L reduction. Fig. 2 shows the threshold laser-energy density for c-Si melting. Since c-Si melting does not have a stopping mechanism different from a-Si melting for the LTP method, c-Si melting with remarkable profile broadening is detectable by checking secondary ion mass spectrometry (SIMS) depth profiles. Both heat assist and the TiN absorber reduced the threshold E_L about by half. In addition, their combination reduced c-Si melting threshold further. Although the TiN light absorber is thus effective for E_L reduction, it needs a barrier material like a silicon oxide to prevent reaction (or silicidation) with an Si substrate. The 5-nm screen oxide was not perfectly thick enough and the reaction was occasionally observed. Complex work on material selection and structure optimization is necessary to find practical absorber structures. In addition, we have recently reported that LA with a metal absorber easily led to the overmelting of the c-Si due to the absence of reflectivity reduction due to Si melting [11], [12]. As a result, the process-window width against E_L was decreased by the introduction of the absorber. Therefore, we can conclude that E_L reduction by HALA is more feasible for device fabrication than that by LA with the light absorber.

IV. Proposal of PMLA

The discussion in the previous section did not treat the influence of substrate heating on the crystallinity of implanted layers. Amorphized Si recrystallizes at high temperature by solid-phase regrowth from the a-Si/c-Si interface. PMLA utilizes solid-phase regrowth and it is a subset of HALA. HALA is a simple combination of LA and substrate heating. By choosing a moderate substrate temperature and heating time to recrystallize a part of amorphized Si, HALA leads to PMLA. Assuming that laser-energy density is appropriately adjusted to melt a-Si and not to melt c-Si, in the case of the LTP, melting depth and junction depth is nearly equal to amorphized depth. However, under the same assumption, substrate heating prior to laser irradiation shrinks a-Si thickness and melt depth. Fig. 3 shows cross-sectional transmission electron microscopy (XTEM) of the Si surface amorphized by Sb^+ implantation and thermally annealed for 8 min at 450 °C. Since the initial and residual a-Si thicknesses were 11 and 6 nm, respectively, the average regrowth rate obtained is 0.63 nm/min. Although the known solid-phase-regrowth rate at 450 °C is about 0.2 nm/min [13], regrowth was sometimes enhanced by impurity introduction [14]. However, substrate heating prior to laser irradiation shrinks a-Si thickness and melt depth. The Sb SIMS depth profiles shown in Fig. 4 show such examples. As shown in

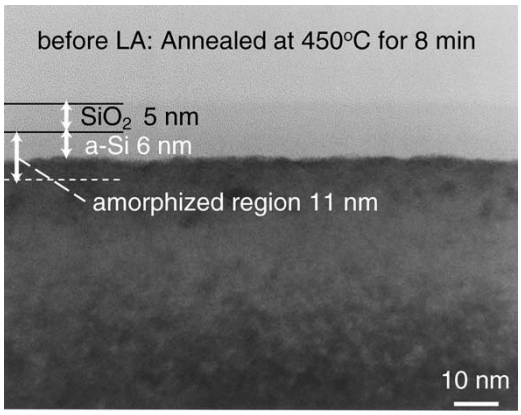

Fig. 3. Observation of solid-phase regrowth by XTEM photograph. About half of the amorphized layer recrystallized by annealing at 450 °C for 8 min. The annealing condition corresponds to the preheating condition for our HALA experiments.

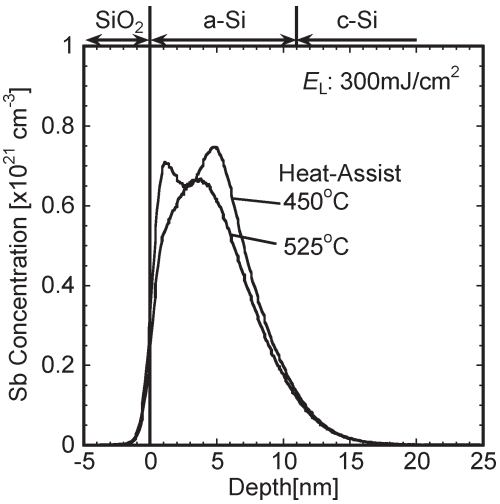

Fig. 4. Sb SIMS profiles after HALA at 450 and 525 °C.

Fig. 3, about a half of a-Si recrystallized before laser irradiation. HALA at 450 °C with E_L of 300 mJ/cm^2 does not melt c-Si. The profile with double peaks seen in Fig. 4 is considered to originate from the melting of the upper half portion of the amorphized layer. In other words, HALA at 450 °C with E_L of 300 mJ/cm^2 is an example of PMLA. If this is the case, the shallower peak is a pileup peak formed by Sb segregation to the melt phase [10] during resolidification after a-Si melting. The deeper peak is probably located just below the bottom of the shrunk a-Si layer. The deeper peak was a result of Sb redistribution toward the surface, which occurred at the shallower melt part. The profile for HALA at 525 °C has only one peak. This is understood as a result of faster solid-phase regrowth at 525 °C and the absence of an a-Si layer at the timing of laser irradiation. LA at this $E_L$without an a-Si layer also means nonmelt annealing.

Based on these experimental results, we propose a new LA scheme called PMLA. The basic concepts of PMLA can be explained upon referring to model drawings in Fig. 5, which illustrate how the dopant profile is modified by LA. As described in the introduction section, prior to dopant implantation, Ge^+ is usually implanted to suppress the channeling tail caused by ion

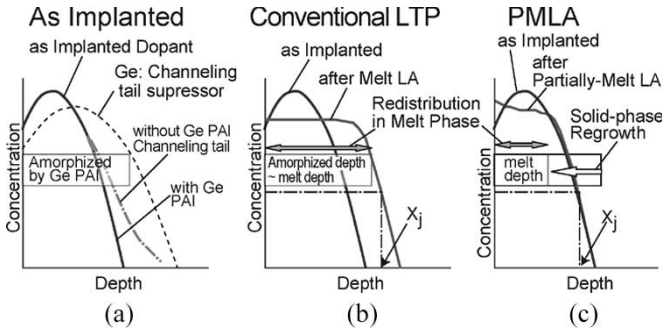

Fig. 5. Model drawing explaining the relationship between amorphized-layer depth, melt depth, and dopant profile. (a) As-implanted dopant and Ge profiles; profiles for (b) melt LA such as LTP; and for (c) proposed PMLA.

channeling, as shown in Fig. 5(a). Conventional LTP employs laser irradiation to melt all of the a-Si for activation annealing, as shown in Fig. 5(b). In the case of the proposed PMLA, wafers are heated to initiate the solid-phase regrowth of a-Si. The time and temperature of this heating process should be adjusted to obtain the desired a-Si thickness. The laser is then irradiated to the wafer to melt the remaining a-Si. Here, by continuing to heat the substrate, the advantages of HALA are inherited to PMLA. However, it is better to lower the substrate temperature for laser-irradiation timing to slow down regrowth rate and to avoid nonuniformity problem due to further regrowth during the irradiation process for a whole wafer. In the case of the PMLA, the redistribution of the dopant is mainly observed to the remaining a-Si depth because of its melting. The junction depth for PMLA is mainly defined by the original dopant-implantation profile because of the nearly diffusionless nonmelt LA feature. Therefore, the amorphization depth by PAI and melting depth is independently tunable considering the device features. For example, tailoring the extended defect depth by PMLA is possible. Since the extended defects, such as the end-of-range (EOR) defects, are mainly located just below the a-Si/c-Si interface, their depth can be controlled by PAI energy and the amorphization depth.

V. 10 nm Junction Formation With PMLA

We previously reported a 20-nm-deep junction formation with HALA [7], [8]. In order to demonstrate the potential of PMLA, we attempted to fabricate shallower junctions. Figs. 6 and 7 show SIMS depth profiles of an n^+/p junction with Sb and a p^+/n junction with B, respectively. Both junctions were formed with 450-°C PMLA. In both cases, junctions shallower than 10 nm and steeper than 2 nm/dec. were obtained. Since the profile-tail region did not melt because of solid-phase regrowth, the dopant profiles in that region were not affected by PMLA. Concerning the region of high dopant concentration close to the Si surface, in the case of Sb, dopant redistribution due to melting is seen, as shown in Fig. 6. However, in the case of the B profile in Fig. 7, the profile for post-PMLA is nearly identical to that of the as-implanted one. This is not because of the absence of melting, but due to SIMS quantification errors at the surface region. The SIMS B profiling condition for Fig. 7 is usually referred to as a nearly normal incidence with O_2^+ and it is also an oxidizing condition. This

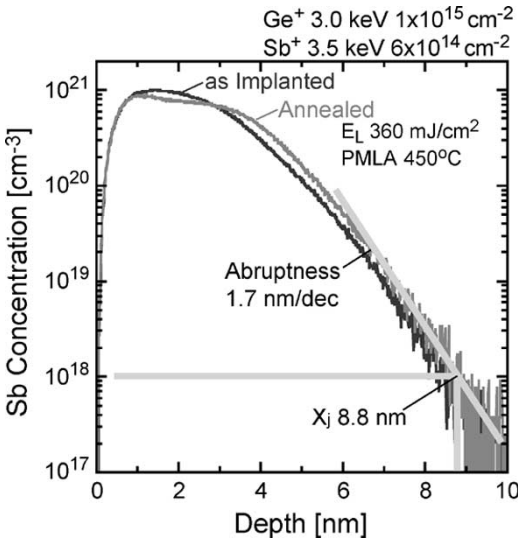

Fig. 6. SIMS depth profile of Sb ultrashallow junction formed with PMLA. Junction depth (X_J) is defined at 1×10^{18} cm^{-3}.

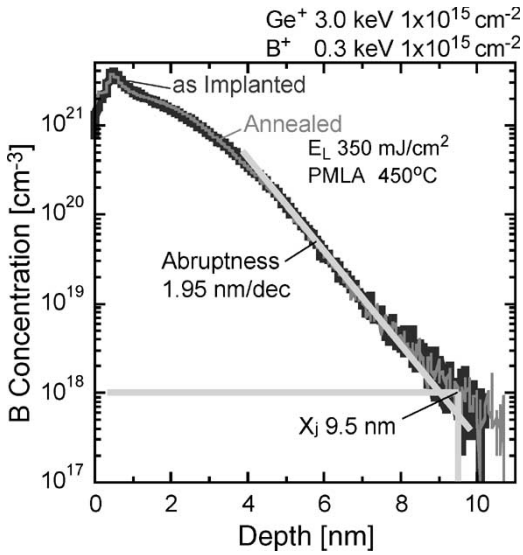

Fig. 7. SIMS depth profile of B ultrashallow junction formed with PMLA. Junction depth (X_J) is defined at 1×10^{18} cm^{-3}. SIMS measurement was carried out under oxidizing conditions to evaluate abruptness and junction depth.

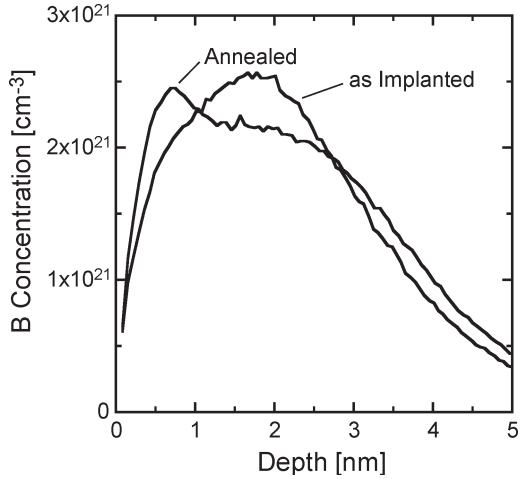

Fig. 8. B SIMS depth profile for the same specimen as Fig.8. Nonoxidizing SIMS condition was chosen to obtain accurate B concentration around the Si surface.

method has an advantage for depth resolution and is suitable for junction-depth and profile-steepness evaluations; however, it sometimes suffers from inaccuracy with respect to the B concentration in the near-surface region because of B migration due to oxidation [15]. The B migration during the SIMS measurement formed an additional small peak around the depth of 0.5 nm from the surface in Fig. 7. To avoid this problem, a nonoxidizing condition [15] obtained with higher incident-angle SIMS measurement was adopted for the same specimen. As Fig. 8 shows, B redistribution due to PMLA appeared via this alternative SIMS measurement. Since this SIMS is inferior in depth resolution for regions deeper than several nanometers from the surface, because of an increase in roughness due to ion sputtering, Fig. 8 should be ignored when considering junction depth and steepness. Instead, we can recognize B redistribution in Fig. 8, which is probably due to the melting of the upper half of the amorphized region.

From an application viewpoint, PMLA can be applied for much shallower junction formation, since the increase in junction depth by PMLA is negligible, as Figs. 6 and 7 indicate. In addition, a sheet resistance lower than 1 kΩ/sq. was obtained, as shown in Fig. 9, which illustrates the relationship between sheet resistance and E_L. The lowest sheet resistances obtained for 10-nm junctions were about 700 Ω/sq for both Sb n$^+$/p and B p$^+$/n junctions.

Concerning residual defects, we have observed a relatively high density of stacking faults in the non-heat-assist LA specimen [10]. Too-fast recrystallization from the melt phase due to nanosecond-order heating is a considerable origin of defect formation. Although reducing the recrystallization speed by increasing pulse duration is effective for reducing the defects [16], it is generally difficult to change the laser pulse duration. Therefore, the problem of residual defects should be solved by means of process modification. Fig. 10 shows XTEM photographs after PMLA or HALA. In Fig. 10(a), an Sb-doped specimen without Ge$^+$ PAI after 450 °C PMLA exhibits a high density of stacking faults that are in parallel to (111) planes. The Si surface of this specimen was amorphized by Sb$^+$ implantation to the depth of about 11 nm. The depth of the stacking faults is shallower than this amorphization depth, which supports partial melting of the a-Si layer. By changing the substrate temperature to 525 °C, the stacking faults disappeared, as shown in Fig. 10(b). This case does not correspond to PMLA, because no a-Si remained because of fast solid-phase regrowth. Ge$^+$ PAI was also effective for the reduction of the stacking faults for 450 °C PMLA, as shown in Fig. 10(c) and (d). Even if the stacking faults were eliminated, extended defects are observed below the original a-Si/c-Si interface in these figures. The investigation on the influence of these kinds of defects on device electrical characteristics remains an issue.

VI. Conclusion

The effectiveness of HALA for E_L reduction was discussed comparing LTP and LA with the light absorber. Based on

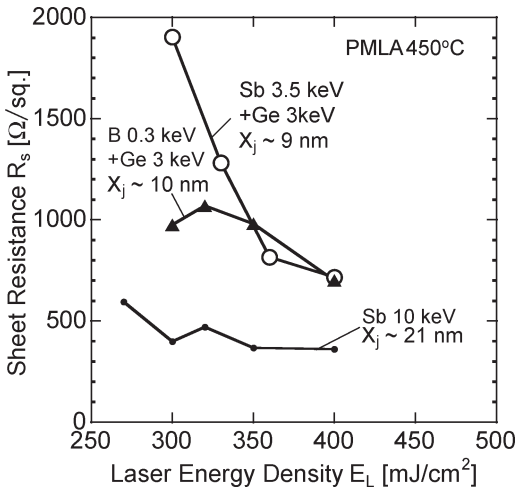

Fig. 9. Relationship between sheet resistance and laser-energy density E_L. Sheet resistance lower than 1000 Ω/sq was obtained with PMLA for 10-nm junctions.

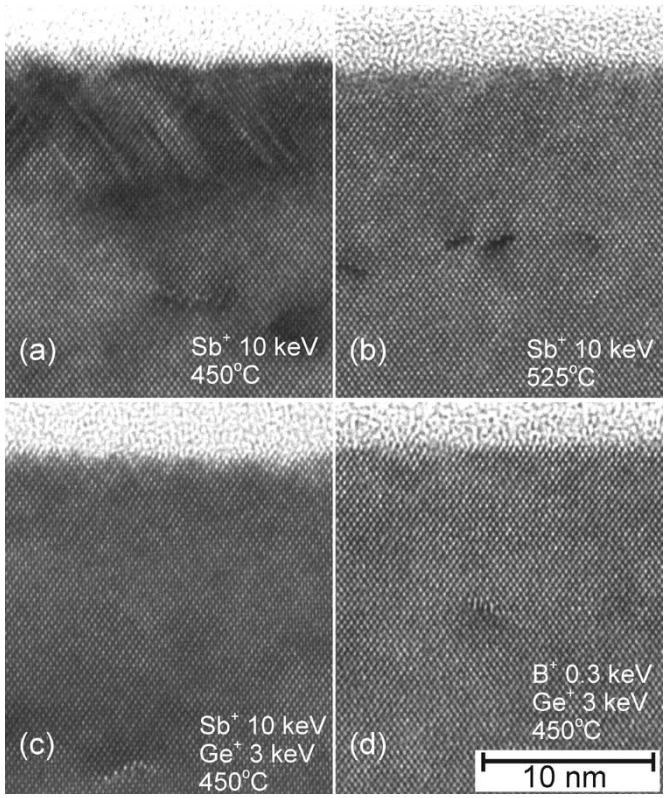

Fig. 10. (a), (c), and (d) XTEM photographs for evaluating residual defects after PMLA at 450 °C and (b) HALA at 525 °C. Stacking faults seen in (a) are reduced by using (b) high-temperature heat assist or (c) and (d) Ge PAI. E_L for (a)–(c) was 300 mJ/cm^{-2} and for (d) was 350 mJ/cm^{-2}.

experimental results of HALA, a new scheme for LA, called PMLA, was proposed. PMLA is combination of solid-phase regrowth and HALA. The 10-nm junctions whose sheet resistances were about 700 Ω/sq. were successfully fabricated with PMLA. This method accompanies a negligibly small diffusion at the profile tail. Consequently, the junction depth can be reduced as long as ion implantation provides a shallower profile via a decrease in the implantation energy. The Ge^+ implantation that was utilized for preamorphization was also effective at reducing stacking faults originating from the very fast recrystallization rate from the melt phase.

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REFERENCES

[1] K. Yamashita, M. Noguchi, H. Nishimori, T. Ida, M. Yoshioka, T. Kusuda, T. Arikado, and K. Okumura, "Kinetics of boron activation by flash lamp annealing," in *Ext. Abst. Int. Conf. Solid State Devices Mater.*, 2003, pp. 742–743.

[2] A. Mokhberi, L. Pelaz, M. Aboy, L. Marques, J. Barbolla, E. Paton, S. McCoy, J. Ross, K. Elliott, J. Gelpey, P. B. Griffin, and J. D. Plummer, "A physics based approach to ultra-shallow p^+-junction formation at the 32 nm node," in *IEDM Tech. Dig.*, 2002, pp. 879–882.

[3] T. Ito, K. Suguro, T. Itani, K. Nishinohara, K. Matsuo, and T. Saito, "Improvement of threshold voltage rolloff by ultra-shallow junction formed by flash lamp annealing," in *VLSI Symp. Tech. Dig.*, 2003, pp. 53–54.

[4] V. I. Kuznetsov, A. J. M. M. van Zutphen, H. R. Kerp, P. G. Vermont, X. Pages, J. J. van Hapert, K. van der Jeugd, and K. E. H. A. Granneman, "Continuity in the development of ultra shallow junctions for 130-45 nm CMOS: The tool and annealing methods," in *Ext. Abst. Int. Conf. Adv. Therm. Process. Semicond.*, 2003, pp. 63–74.

[5] A. Shima, H. Ashihara, T. Mine, Y. Goto, M. Horiuchi, Y. Wang, S. Talwar, and A. Hiraiwa, "Self-limiting laser thermal process for ultra-shallow junction formation of 50-nm gate CMOS," in *IEDM Tech. Dig.*, 2003, pp. 493–496.

[6] K. Adachi, K. Ohuchi, N. Aoki, H. Tsujii, T. Ito, H. Itokawa, K. Matsuo, K. Suguro, Y.Honguh, N. Tamaoki, K. Ishimaru, and H. Ishiuchi, "Issues and optimization of millisecond anneal process for 45 nm node and beyond," in *VLSI Symp. Tech. Dig.*, 2005, pp. 142–143.

[7] K. Kurobe, Y. Ishikawa, K. Kagawa, Y. Niwatsukino, A. Matusno, and K. Shibahara, "Formation of low-resistive ultra-shallow n^+p junction by heat-assisted excimer laser annealing," in *Ext. Abst. Int. Workshop Junction Technol.*, 2002, pp. 35–36.

[8] K. Kurobe, Y. Ishikawa, and K. Shibahara, "Sheet resistance reduction and crystallinity improvement in ultra-shallow n^+/p junctions by heat-assisted excimer laser annealing," *Jpn. J. Appl. Phys.* submitted for publication.

[9] T. Yamamoto, K. Goto, Y. Tada, Y. Kikuchi, T. Kubo, Y. Wang, S. Talwar, M. Kase, and T. Sugii, "Drive current enhancement by ideal junction profile using laser thermal process," in *VLSI Symp. Tech. Dig.*, 2002, pp. 138–139.

[10] K. Shibahara, Y. Ishikawa, D. Onimatu, N. Maeda, A. Mineji, K. Kagawa, A. Matuno, and T. Nire, "Antimony behavior in laser annealing process for ultra shallow junction formation," in *Ext. Abst. Int. Conf. Solid State Devices Mater.*, 2001, pp. 236–237.

[11] E. Takii, T. Eto, K. Kurobe, and K. Shibahara, "Ultra shallow junction formation by green-laser annealing with light absorber," *Jpn. J. Appl. Phys. 2, Lett.*, vol. 44, no. 24, pp. L756–L759, 2005.

[12] A. Matsuno, E. Takii, T. Eto, K. Kurobe, and K. Shibahara, "Merits and demerits of light absorbers for ultra shallow junction formation by green laser annealing," *Nucl. Instrum. Methods B (NIM-B)*, 2005. in press.

[13] L. Csepregi, E. F. Kennedy, J. W. Mayer, and T. W. Sigmon, "Substrate-orientation dependence of the epitaxial regrowth rate from Si-implanted amorphous Si," *J. Appl. Phys.*, vol. 49, no. 7, pp. 3906–3911, Jul. 1978.

[14] J. S. Williams and R. G. Elliman, "Role of electronic processes in epitaxial recrystallization of amorphous semiconductors," *Phys. Rev. Lett.*, vol. 51, no. 12, pp. 1069–1072, Sep. 1983.

[15] W. Vandervorst, T. Janssenns, B. Brijs, T. Conard, C. Huyghebaert, J. Freuhauf, A. Bergmaier, G. Dollinger, T. Buyuklimanli, J. A. vanden-Berg, and K. Kimura, "Errors in near-surface and interfacial profiling of boron and arsenic," *Appl. Surf. Sci.*, vol. 231–232, pp. 618–631, 2004.

[16] K. Kagawa, Y. Niwatsukino, A. Matsuno, and K. Shibahara, "Influence of pulse duration on KrF excimer laser annealing process for ultra shallow junction formation," in *Ext. Abst. Int. Workshop Junction Technol.*, 2002, pp. 31–34.

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