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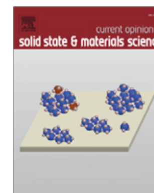

Metal assisted chemical etching for high aspect ratio nanostructures: A review of characteristics and applications in photovoltaics

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ABSTRACT

Metal assisted chemical etching (MacEtch) is a recently developed anisotropic wet etching method that is capable of producing high aspect ratio semiconductor nanostructures from patterned metal film. In this review article, we highlight the characteristics of MacEtch of silicon (Si) including controllability of the produced sidewall roughness, the inherent high aspect ratio, the weak crystal orientation dependence, impurity doping and solution concentration dependent porosity, as well as the applicability of MacEtch to non-Si based semiconductor materials including III–V compound semiconductors. Also reviewed are applications of MacEtch produced high aspect ratio Si nanostructures in photovoltaics, where the p–n junction can be in the planar Si tray, core–shell, or axial geometry, with nanowire, micropillar, or hole arrays serving as light trapping or carrier collection structures. The prospect of using MacEtch to improve the cost and efficiency of photovoltaic cells is discussed.

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1. Introduction

Etching is an important step in semiconductor device processing. Etching techniques are normally classified into two categories: wet and dry etching. For wet etch, the etchant is supplied from the liquid phase and can be carried out simply from a liquid container such as a beaker. For dry etch, etchant is supplied from the vapor phase. Common dry etching techniques include reactive ion etching (RIE), inductively coupled plasma (ICP)-RIE, chemical assisted ion beam etching (CAIBE), all of which require vacuum, plasma generation, ion optics etc. When appropriate mask is used to prevent local etching, both wet and dry techniques are capable of producing 3D structures with topographical variations that are defined by the mask and etching condition. However, wet etching of most semiconductors occurs isotropically, i.e. etching proceeds equally in depth and in the lateral direction. This results in the loss of lateral resolution defined by the mask dimension by as much as two times the depth, thus not suitable for producing high aspect ratio features. One of the exceptions is crystal orientation dependent etch rate enabled anisotropic wet etching, which results in structures that are bounded with slow etch planes. For example, the etch rate of Si(111) in KOH solution can be over two orders of magnitude slower than Si(110); therefore Si(110) surface can be etched to produce deep trenches with (111) sidewalls [1]. However, the application of this etching method can only produce limited types of structures.

Dry etch on the other hand, can be directional because etchant is ionized in the gas phase and accelerated towards the surface where etching takes place. High aspect ratio structures can be formed by several methods including the Bosch (also called deep RIE etching) and cryogenic processes [1]. The lateral resolution is typically defined by the mask itself. However, the achievable depth is limited by effects such as bottling where the bottom of the trench pinches off, and aspect ratio dependent etch rate [1] where etch rate reduces significantly as aspect ratio or depth increases. Sidewall roughness of the etched nanostructures, especially the scalloping effect associated with the time multiplexing Bosch process [1], remains a challenge. Another undesirable side effect of dry etch is ion induced damage to the sidewalls of the semiconductor [2], which increases surface states dramatically and leads to nonradiative recombination and degradation of carrier mobility. For silicon, (Si), thermal annealing has to be used to repair the surface damage; for compound semiconductors such as GaAs and GaN, even with meticulous balancing of ion energy and etching rate, as well as post-etching annealing, ion induced damage remains a challenge for achieving high device performance [3,4].

In this article, we review a recently developed etching technique, metal assisted chemical etching (MacEtch). MacEtch is essentially a wet etching method yet produces anisotropic high aspect ratio semiconductor micro and nanostructures without incurring lattice damage. These high aspect ratio structures can potentially be used for the formation of periodic nanostructures for photonic crystals, gratings, light trapping structures for LEDs and solar cells with better absorption and collection efficiency, for thermoelectric devices with low thermal conductivity when

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the sidewalls are rough [5], and for batteries with greater energy density [6]. Huang et al. recently did a comprehensive and systematic review of MacEtch mechanism and process parameters [7]. We attempt to share our perspective on the unique capabilities and characteristics of MacEtch for producing high aspect ratio semiconductor structures and briefly discuss the current status and future directions of their photovoltaic applications. We note that the topics covered and references cited here are not inclusive of the recent prolific activities on this topic of research, but intend to highlight aspects that are specific to high aspect ratio structures.

2. Background and mechanism of MacEtch

Metal assisted chemical etching (MacEtch), also abbreviated as MaCE or MCE previously [8,9], is fundamentally a wet but directional etch technique. MacEtch was first used as an electroless etching technique using unpatterned discontinuous layer of metal in a H_2O_2 and HF solution, to produce porous Si and porous III–V compound semiconductor by Li et. al. in 2000 and 2002, respectively [10,11], in contrast to the conventional anodic etching method for porous semiconductor formation. MacEtch uses noble metals to induce local oxidation and reduction reactions under open circuit. Metal such as Au, Pt and Ag, deposited on the surface of a semiconductor (e.g. Si) serves as a local cathode to catalyze the reduction of oxidants (e.g. H_2O_2) producing holes (h^+). The holes (h^+) are then injected into the valence band of the semiconductor to oxidize and form the ionic form that is soluble in an acidic solution (e.g. HF). This results in the removal of semiconductor materials without net consumption of the metal. The overall reaction of MacEtch of Si in a solution of H_2O_2 and HF catalyzed by Au can be written as $Si + H_2O_2 + 6HF \xrightarrow{Au} 2H_2O + H_2SiF_6 + H_2\uparrow$, where at the cathode (Au), $Si + 4h^+ \rightarrow Si^{4+}$, and at the anode (Si substrate), $2H^+ + 2e^- \rightarrow H_2$ [7,10]. Details on the MacEtch mechanism and development can be found elsewhere [7,12,13].

By varying the ratio of oxidant and acid in the solution, as well as the catalyst type and pattern, MacEtch can produce either solid or porous nanostructures depending upon the local current flux and subsequent removal of the oxidized semiconductor necessary to keep the local electrochemical reaction moving forward. Under controlled etching conditions, MacEtch reactions occur only at the interface between metal and the semiconductor. As a result, metal descends into the semiconductor as the semiconductor is being etched right underneath, acting as a negative resist etch mask. When the catalyst metal is patterned in any shape and dimension, the pattern can be engraved into the semiconductor to produce micro and nanostructures including arrays of pillars and the inverse holey structures.

Illustrated in Fig. 1 is the formation process of pillar arrays using MacEtch. Fig. 1a shows an Au metal mesh pattern deposited on the surface of a semiconductor (Si). Through MacEtch, the metal mesh sinks down as a result of sacrificial etching directly underneath and leaves behind an array of solid semiconductor pillars shown in Fig. 1b. If the generated holes (h^+) cannot be consumed at the metal–semiconductor interface, they can diffuse to areas not covered by metal forming porous structures, as depicted in Fig. 1c. Slanted pillar arrays (Fig. 1d) can also be formed depending on the availability of surface atoms (crystal orientation dependent) for oxidation reaction and the removal rate [14].

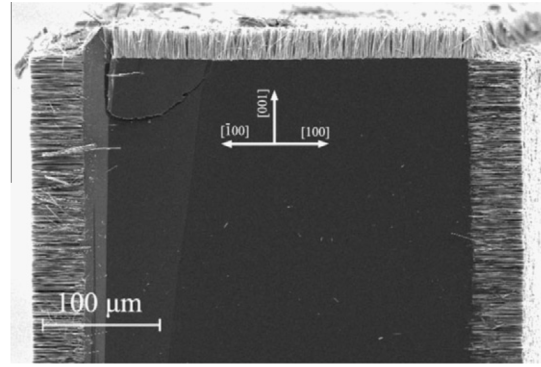

Fig. 2. Top-view SEM image of an etched Si(1 0 0) wafer in aqueous HF/H_2O_2 solution. All sides of the Si wafer were coated with Ag nanostructures before etching, while the top surface was intact. Reproduced from Ref. [15].

The nature of MacEtch was demonstrated through a clever experiment [15] shown in Fig. 2. Arrays of Si nanowires (NWs) were generated on all sidewalls where Ag was deposited, while no etching took place on the top surface where there was no Ag. Clearly, metal sinks, glides, drills through the Si surface irrespective of it being the top surface or sidewall [15].

3. Characteristics of MacEtch

3.1. Metal catalyst and patterning

Noble metals including Ag, Au, Pt, Pd, Cu, etc. have been demonstrated to be effective catalysts for MacEtch of Si [10,12,16–21]. In order to form high aspect ratio semiconductor array based structures, the catalyst pattern can be defined by lithography from evaporated or sputtered continuous metal films. It can also be self-generated by electroless plating from metal salt solution. For example, dendrite-like Ag metal network can be self-generated from $AgNO_3$ solution [16,22–24] NO_3^- in this case also acts as the oxidizing agent for MacEtch. Other oxidizing agents have also been explored [25,26].

Table 1 compares the advantages and disadvantages of MacEtch from solid metal thin film pattern vs. solution based metal network Obviously, solution based patterning is simple and less expensive since no evaporation/sputtering and lithography are involved. However, as expected, there is little control over the produced feature size and shape. For example, $AgNO_3$ solution based MacEtch of Si generates Si nanowires with diameters in the range of 20–

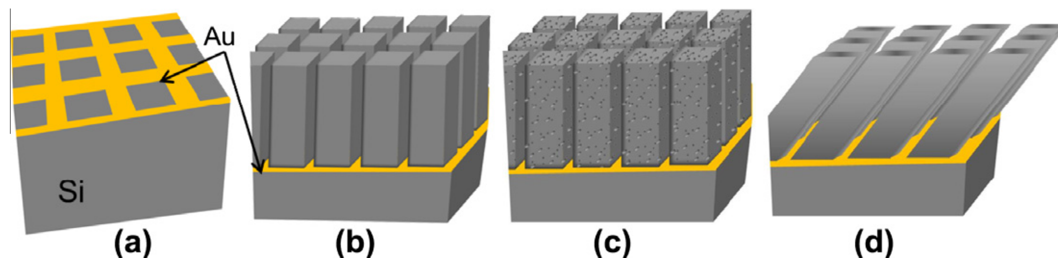

Fig. 1. Illustration of MacEtch process to form semiconductor (Si) pillar array with metal (Au) Mesh as catalyst. The Au Mesh grid pattern descends into the semiconductor (Si) and leaves Si pillars standing in vertical and solid (a), vertical and porous (b), slanted and solid (c), or slanted and porous (not shown) Morphology.

Table 1
Comparison between MacEtch using catalysts formed from gas phase deposited metal pattern and solution phase metal network.

	Evaporated or sputtered metal catalyst	Solution based metal catalyst
Pattern size	Micro and nanoscale	Nanoscale only
Pattern size distribution	Uniform, determined by lithography	Random, large distribution
Pattern site control	Complete control	Not feasible
Patterned structure	Versatile	Interconnected network
Etching rate	Fast	Slow
Scalability	Good	Good
Cost	Relatively high	Low

300 nm [5]. The etch rate of Si using solution based $AgNO_3$ varies with $AgNO_3$ concentration and etching time [22]. It can be as slow as 4–10 μm/h [5,22], which is ∼10 times slower than typical solid thin film catalyzed MacEtch [14]. In addition, with self-generated metal network, nanowires seem to be the only shape and size range this solution based method can produce. In contrast, solid metal film can be patterned into different shapes of various scales, continuous network or discrete patterns, leading to lines, wires, holes, pin-in-a-hole [27], or annular shapes with dimensions defined by lithography [14], even 3D geometries [9,28]. Both solution phase and solid film based MacEtch are scalable and can readily be done at wafer-scale.

3.2. Roughness

Depending on the catalyst type and etching conditions, nanowires formed can have rough or smooth surfaces. For example, Ag-MacEtch, from both solution and thin film based Ag patterns, yields rough sidewalls, while Au-MacEtch produces smooth sidewalls for Si. The hypothesis is that Ag nanoparticles or thin film nanopatterns actually disintegrate, diffuse out, redeposit randomly and sink into the formed nanowire surfaces continuously during the entire process of MacEtch to induce secondary MacEtch on the sidewalls forming pits [14,29–31]. Such pitting induced roughness increases with increasing etching temperature and Si doping level, due to the higher reactivity of highly doped Si [30]. Severe pitting from stray Ag particles can also lead to tapered profile from sidewall etching [29]. Shown in Fig. 3 is a TEM image showing the roughness of a Si nanowire produced. The Si nanowire was formed by Ag-MacEtch where the Ag pattern was produced by a non-lithographic patterning technique S4 (solid state superionic stamping) in a solution of [HF]:[H_2O_2] of (2.5–3.0):1 in volume [14]. In contrast, Au thin film nanopatterns appear to be stable against dissolution in MacEtch solution, avoiding attacking the NW sidewalls. In fact, an Au/Ag bilayer catalyst was recently used to counter the Ag oxidation dissolution problem to form vertical and smooth Si nanowires [29].

Controlled roughness of nanowire sidewalls is crucial for applications such as thermoelectrics. That is because correlated multiple scattering of phonons off the rough surface can lead to a reduced thermal conductivity below the Casimir limit. The reduction is dependent not only on the roughness amplitude but also on the roughness correlation length [32]. If the nanowire diameter is controlled so that it is small enough that phonons experience significant sidewall scattering while big enough that electrical carrier mobility is not affected by the sidewall roughness, a high ZT can be expected from such nanostructures [5,33]. Creating nanowires with controlled fine roughness is a distinct capability of MacEtch but hard to achieve using bottom-up deposition methods

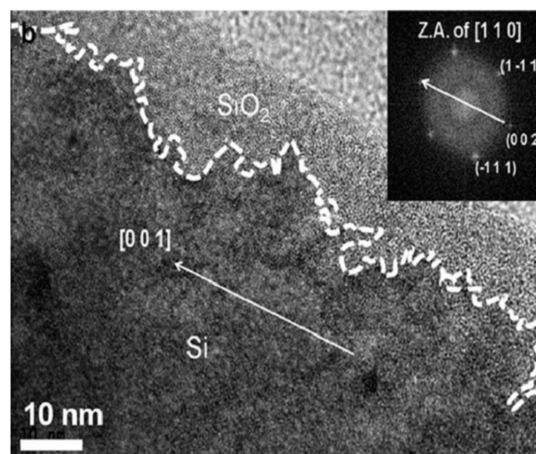

Fig. 3. High resolution TEM image with corresponding fast Fourier transform patterns along [1 1 0] zone axis, indicating the nanowire axial direction as ⟨1 0 0⟩. The image shows an extremely rough interface between silicon and the amorphous layer, presumably silicon oxide. The height variation on surface is as much as ∼12 nm and lateral undulating features are as small as ∼1 nm. The interface between silicon and the amorphous oxide layer is traced with dashed lines for visual clarity. Reproduced from Ref. [14].

through mechanisms such as the metal-catalyzed vapor–liquid–solid (VLS) growth.

3.3. Aspect ratio

Based on the mechanism of MacEtch, metal can drill through Si as far as etching time allows, as long as metal stays in intimate contact with the silicon surface. This makes the aspect ratio of the structure created essentially determined by etching time. Several groups have demonstrated boring silicon with nanoparticles with extremely high aspect ratio [34,35]. A 50 nm Au colloidal particles drilled all the way down to ∼85 μm below the Si(1 0 0) surface after two hours in a HF/H_2O_2 solution, corresponding to an aspect ratio of 1700 [36]. The Au nanoparticle was clearly visible at the bottom of the trench. However, the uniformity of such trench structures drilled by discrete nanoparticles is poor compared to MacEtch with interconnected metal catalyst pattern such as a mesh, probably because the mobility of discrete metal nanoparticles is larger than a whole perforated sheet. Maintaining the intimate contact with the semiconductor surface is the challenge for achieving unlimited high aspect ratio. In addition, having H_2

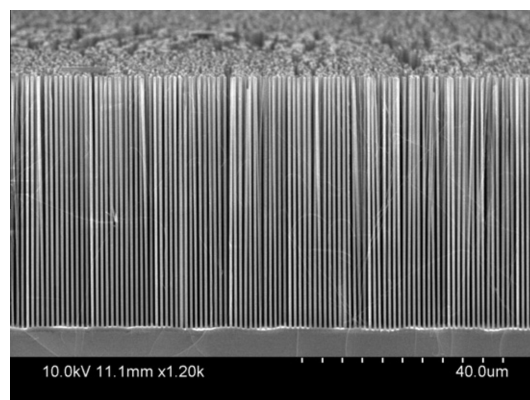

Fig. 4. SEM image of an array of Si nanowires with diameter of 550 nm, height of 51 μm, thus an aspect ratio of ∼93, produced through Au-MacEtch with Au mesh film patterned using soft lithography on p^+ Si. Reproduced from Ref. [37].

gas as the product does not help preventing metal delamination from the surface. Nonetheless, ordered high aspect structures can be readily achieved when the etching condition is well controlled. Shown in Fig. 4 is a titled SEM image showing a well-ordered array of Si nanowires with aspect ratio close to 100, produced by Au-MacEtch with Au mesh film patterned by soft lithography [37]. Densely packed Si nanowire array, with sub-10 nm diameters and aspect ratio as high as 220, has also been demonstrated [38,39]. The Au mesh patterns used in these studies were patterned using either block-copolymer or AAO template lithography.

3.4. Orientation dependence

Several groups systematically studied the effect of etchant concentration on etching direction as well as morphology using (1 0 0), (1 1 0), and (1 1 1) Si substrates [14,40,29]. It was found that for p-type Si (1 0 0) wafers with resistivity of 6–8 Ω cm, vertical ⟨1 0 0⟩ nanowires are formed at lower volumetric ratio HF/H_2O_2 ratio of 3:1 while ⟨1 1 1⟩ nanowires are generated when the HF concentration is increased by 25%, as verified by TEM [14]. Huang et al. concluded that in solutions with low oxidant concentration, etching proceeds along the crystallographically preferred ⟨1 0 0⟩ directions, whereas etching occurs along the vertical direction relative to the surface of the substrate in solutions with high oxidant concentrations [40]. This was attributed to the competition of hole injection (oxidation) and mass transport (dissolution) with respect to surface atom density. The amount of carriers (h^+) injected and consumed could regulate both the etching direction and morphology. Based on these phenomena, Si nanopores with modulated orientations by periodically etching a (1 1 1) substrate in solutions of low and high oxidant concentrations have been demonstrated [40].

Taking advantage of the crystal orientation dependence on etching conditions, strikingly periodic zigzag Si nanowires have been reported [41,42]. Notably, an initial porous Si layer was deemed important for the formation of zigzag Si nanowires using Si(1 0 0) wafers through MacEtch using patterned Au mesh as catalyst at an elevated temperature (60 °C) [41]. The axial thickness and orientation undulation along the zigzag profile for these Si nanowires, were attributed to a periodic fluctuating concentration of oxidant directly above the wafer during etching as a result of delayed solution equilibrium from a non-stirred reaction. The porous surface layer was believed to deter the solution trying to reach equilibrium. In another report, an intentionally scratched rough surface leads to zigzag while polished smooth surface yielded straight wires using (1 1 1) n-type or p-type Si substrates in HF-$AgNO_3$ MacEtch solution [42]. The controlled etching direction is attributed to the preferred movement of Ag nanoparticles under controlled conditions. The ability of controlling the turning angle of etching is unprecedented. By using a two-step MacEtch process, where the concentration ratio of HF to H_2O_2 changed from etching vertically for nanohole array formation to lateral etching at the bottom of the holes, Shiu et al. demonstrated a MacEtch enabled lift-off (or detaching) of high aspect ratio nanohole thin film from the Si(1 0 0) substrate [43].

The concentration effect also enables MacEtch of polycrystal Si as long as the etching condition is controlled in the range where there is a weak dependence on crystal orientation. Large area free-standing Si nanowire arrays have been successfully prepared on polycrystalline Si, as reported by Peng et al. [44]. As shown in Fig. 5, the Si nanowires are bundled up into clusters, which occurs naturally for high aspect ratio vertical nanowires due to surface tension, if supercritical drying is not applied. Many structural domains composed of bundles of Si nanowires can be seen on the etched poly Si surface and separated by presumably domain boundaries that are of the same size of a single Si crystallite.

3.5. Porosity

In principle, MacEtch works for all doping types and doping levels because the local oxidation dissolution is driven by externally generated holes. In the scenario illustrated in Fig. 1b, etching occurs exclusively beneath the metal. However, porous nanowires (Fig. 1c) can form if the generated holes (h^+) diffuse beyond the metal–semiconductor interface. Excess hole (h^+) generation (high H_2O_2 concentration) or high rate of Si^{4+} removal (high HF concentration) allow hole (h^+) diffusion to areas that are between the patterned metals. Solid nanowires can only be produced when the HF and H_2O_2 concentration ratio is somewhat balanced, and beyond that window on both sides of the concentration chart, porous structures are generated, as observed by Chern et al. [14]. Porosity has been found to be higher at the top of nanowires, which resulted in bending or cone formation due to subsequent porosity accelerated oxidation and etching [45,46]. In addition to etchant concentration, Si doping level affects the nanowire porosity significantly [47]. For highly doped Si wafers, etching conditions used for p- and n- Si wafers do not readily produce high aspect ratio solid nanowire arrays. The probability of generating porous wires or even electropolishing significantly increases with increasing doping concentration. Qu et al. has reported systematic study of MacEtch of highly doped n-type Si wafers (resistivity 0.008–0.02 Ω cm) using dry Ag nanoparticle network deposited from $AgNO_3$ solution [48,31]. By systematically tuning the H_2O_2 concentration in the etching solution, solid nonporous, nanoporous silicon nanowires, or nonporous/nanoporous core/shell nanowires were obtained. Shown in Fig. 6 are a series of TEM images of single Si nanowires produced using four doping levels of Si wafers by Ag-MacEtch [31]. Clearly, the porosity increases as the wafer resistivity decreases. The same trend applies to p-type Si. This poses challenges for producing solid nanowires from degenerately doped Si.

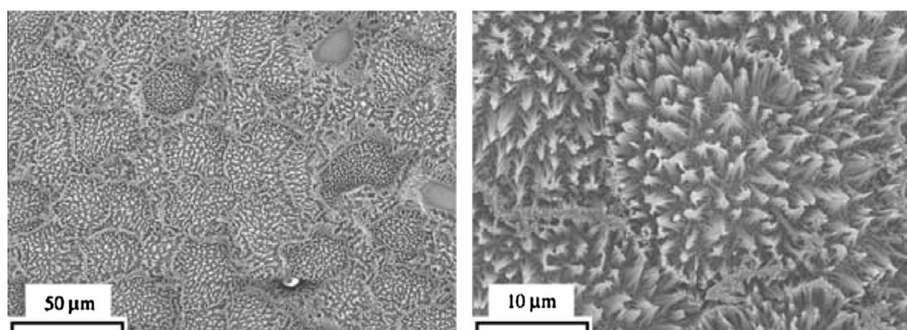

Fig. 5. Top-view SEM images of Si nanowire array prepared from a polycrystalline Si wafer. Reproduced from Ref. [4].

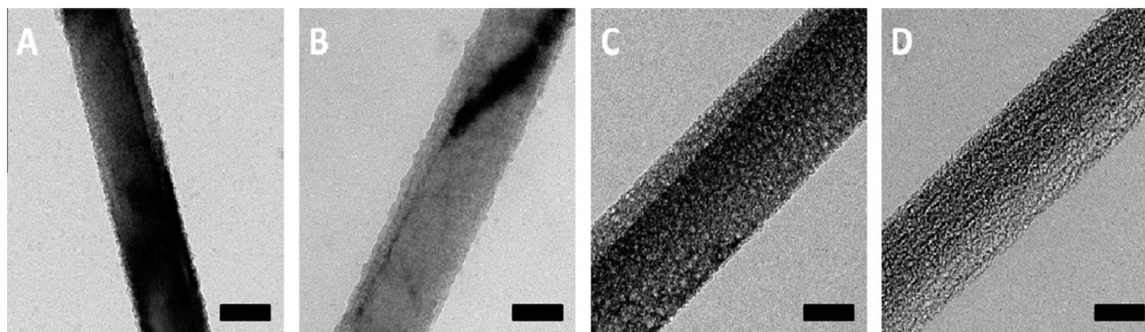

Fig. 6. TEM images of the silicon nanowires obtained from Ag-MacEtch of wafers with four doping levels in etchant solutions composed of 4.8 M HF and 0.3 M H2O2 for 15 min: (A) silicon nanowires from a 1–5 Ω cm wafer, (B) silicon nanowires from a 0.3–0.8 Ω cm wafer, (C) silicon nanowires from a 0.008–0.016 Ω cm wafer, and (D) silicon nanowires from a 0.001–0.002 Ω cm wafer. The scale bars are 100 nm. Reproduced from Ref. [31].

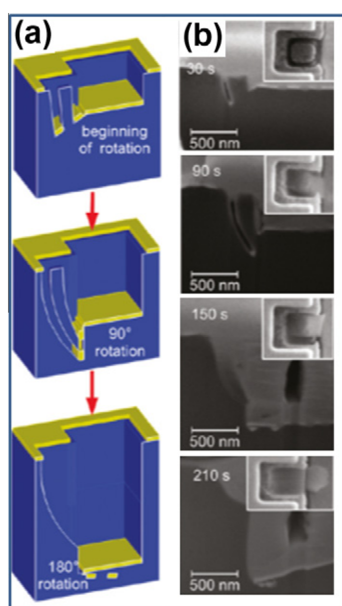

Fig. 7. (a) Schematic representation of the two part hinged Au template folding dynamics. (b) Top and cross-sectional SEM images demonstrating time progression of 350 nm side length perforated squares with a characteristic length of ≈60 nm folding around a ~6 μm uniform film square. Adapted from Ref. [9].

3.6. Etch rate

In general, etch depth increases linearly with etch time for MacEtch [7]. However, etch rate varies greatly depending on the metal catalyst size, shape, spacing, connectivity etc. Etch rate does not scale with the total area of metal catalyst, because of variation in liquid access and possible sharing of generated holes within adjacent areas.

Rykaczewski et al. performed a systematic study on the effect of catalyst template geometry on the etching rate of Si [8]. It was found that the etch rates for uniform Au film templates with similar areas match regardless of the geometry (square, circle, or rectangle) and generally increase with a decrease in the area. Not surprisingly, etch rates for the perforated templates do not match the etch rates of the uniform film templates with similar areas, but scales with the inverse of a characteristic length defined as the ratio of the cut out gold surface area (void) to edge distance. Taking advantage of the differential in-plane etch rate that can be controlled by topological varying metal patterns, translational and rotational movement of the metal catalyst film into silicon can be realized. Out-of-plane rotational etching has been demonstrated, which yields topologically complex 3D nanostructures with intimately integrated metal and silicon features [9,28] An example is shown in Fig. 7.

3.7. Applicability to non-Si semiconductors, alloys, and heterojunctions

In principle, high aspect ratio structures can be produced from other types of semiconductors by MacEtch, as long as there exists a large differential etching rate of the semiconductor with and without the metal. The ideal MacEtch solution needs to be inert without the presence of metal, regardless of the semiconductor material system. Naturally, the etchant solution including the oxidant and acid types, concentration, and ratio, as well as etching temperature need to be adjusted for different types of semiconductors. However, other than Si, MacEtch of other semiconductors remain a virgin area, especially for high aspect ratio ordered structures.

Sub-20 nm Si/Ge superlattice nanowires have been formed by Ag-MacEtch using AAO as a template for Ag patterning [45,49]. Wang et al. has demonstrated the formation of ordered arrays of SiGe nanowires by Au-MacEtch of composition graded Si_xGe_{1-x} alloy wafers using Au mesh patterns created by nanosphere lithography [50]. The chemical compositions and axial heterostructures in the formed nanowires have been verified to be the same as those of the as-grown films, as shown in Fig. 8. These alloy nanowires and one-dimensional heterostructures may have great potential for thermoelectric, vertical logic, photovoltaic, and memory-device applications.

Wire-like GaN nanostructures that are small enough to show quantum confinement effect has been produced using Pt as a catalyst in HF/H_2O_2 MacEtch solution [11,51]. Nanoporous 6H and 4H n-type SiC has been achieved in a $HF/K_2S_2O_8$ Pt-MacEtch aqueous solution [52]. MacEtch has also been combined with UV irradiation to accelerate the etch rate, i.e. metal assisted photodissolution [51–57]. Asoh et al. [55] demonstrated the formation of n-type InP ($1–5 \times 10^{18}$ cm^{-3} S doped) microbump arrays with ordered intervals, using MacEtch with noble metal film (<=30 nm) patterned using a Cu mesh in a H_2SO_4 and H_2O_2 solution (Fig. 9a). In contrast to standard MacEtch, metal assisted photodissolution in this case took place in exposed InP surfaces around metal-coated areas while the Pt coated area remained almost unetched during UV irradiation. The metal assisted photodissolution mechanism, which involves the recombination of photogenerated electrons in the uncovered area with holes generated from the metal catalyst, was illustrated in Fig. 9b. The etching rate of the InP substrate was drastically accelerated by UV irradiation from a mercury lamp. The etching speed increased in the order of Au < Pd < Pt, corresponding to the order of the magnitude of the work function of each metal. Producing high aspect ratio structures using this

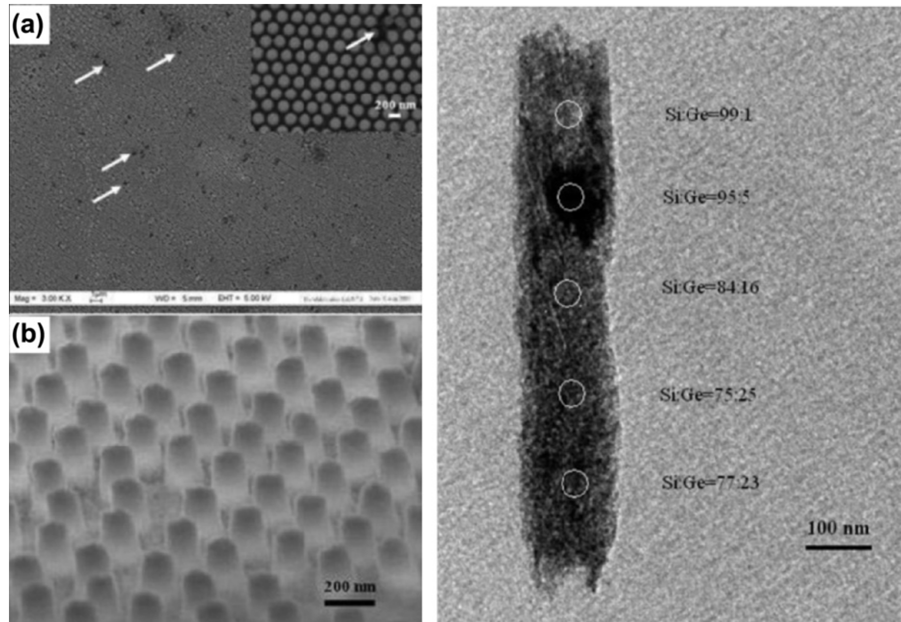

Fig. 8. SEM images of homogeneous SiGe nanowire arrays: (a) low-magnification plane-view showing large-area arrays and (b) 30° tilted cross-sectional view of nanowire arrays. (c) TEM image of SiGe nanowire heterostructure. Shown to the right are Si/Ge ratios determined by EDS taken from the corresponding area highlighted by circles in the Si/SiGe nanowire. Reproduced from Ref. [50].

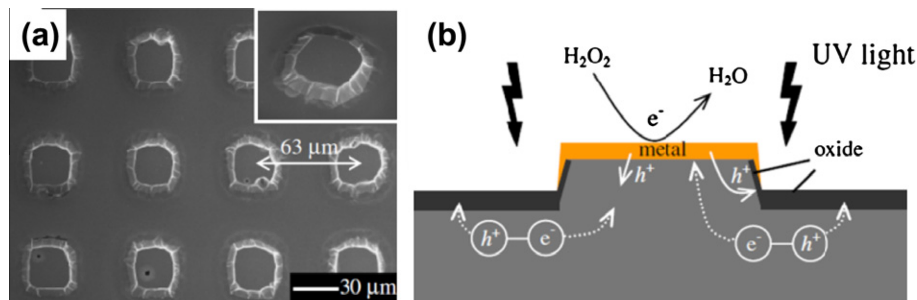

Fig. 9. (a) SEM image of an array of InP micro-bumps spaced by 63 μm with a height of ~7.5 μm fabricated under UV irradiation in a Au-MacEtch solution for 60 min. (b) Illustration of the metal-assisted photodissolution mechanism that promotes etching in non-metal coated areas, in contrast to standard MacEtch. Adapted from Ref. [55].

method might be challenging since the etch rate appears to be slow (~0.1 μm/min) and verticalness of the sidewalls is not clear.

Built upon previous reports [58–60] on MacEtch generated III–V nanoporous columnar structures, crevices, protrusions, and periodic micro hole arrays, very recently, Dejarld et al. has successfully demonstrated for the first time the formation of periodic high aspect ratio III–V nanostructures. In particular, GaAs nanopillars, vertical and undulated, have been produced by Au-MacEtch of n-type (1 0 0) GaAs wafers without UV illumination using $KMnO_4$ as the oxidizing agent and soft-lithography patterned Au mesh as catalysts [61], as shown in Fig. 10. The realization of high aspect ratio III–V nanostructure arrays using MacEtch can potentially transform the fabrication of distributed Bragg reflector, distributed feedback, and photonic crystal semiconductor lasers where surface gratings are currently fabricated by dry etching.

To summarize the essential aspects of MacEtch, Table 2 compares the general properties of MacEtch with traditional wet and dry etching methods including verticalness of the side wall (or as-

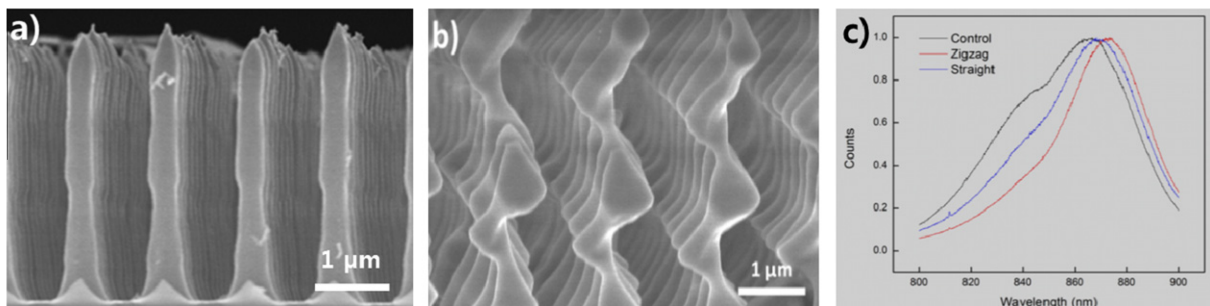

Fig. 10. Side view SEM images of an array of high aspect ratio GaAs vertical (a) and zigzagging (b) nanopillars produced from a 600 nm diameter Au mesh on n-type (100) GaAs wafer patterned by soft lithography; and room temperature PL spectra (c) taken from GaAs pillars in (a) and (b) along with a planar GaAs substrate control sample. Adapted from Ref. [61].

Table 2
Typical characteristics of three etching techniques for semiconductors.

	Wet etch	Dry etch	MacEtch
Directionality	Isotropic	Anisotropic	Anisotropic
Aspect ratio	Low	Medium	High
Ion induced damage	None	Mild to severe	None
Crystal orientation dependence	Some	Weak	Weak
Etch rate	Fast	Slow	Fast
Sidewall smoothness	Smooth	Not smooth	Smooth or rough
Chemical selectivity	Good	Poor	Depends
Cost	Low	High	Low

pect ratio), smoothness, etch rate, selectivity etc. Note that metal used in MacEtch is not incorporated in the core of the semiconductor because the etching takes place near room temperature. MacEtch is no doubt a new paradigm that holds much potential to be a complimentary etching technique to wet and dry etch methods.

4. Photovoltaic Applications of MacEtched high aspect ratio nanostructures

Nanowire based solar cells have been explored to reduce optical loss, enhance optical absorption, and improve carrier extraction for high performance and low cost designs. Anisotropic alkaline texturization is a standard process for commercial monocrystalline Si solar cell production. However, for polysilicon, this method is not effective because of the presence of grains of non-⟨1 0 0⟩ orientations. It is also well known that porous Si can reduce the reflectance to as much as less <4% in 400–1000 nm wavelength range and therefore can replace other surface-textured microstructure and antireflection coatings. Si nanowires and micropillars can reduce the reflectivity even further by accurately controlling the nanowire orientation (vertical vs slanted), size (nano vs microscale), density, length [62]. At the same time, high aspect ratio nanowires and micropillars can enhance absorption through superior light trapping mechanism, allowing significantly thinner structures thus reduced material cost [62–64]. This is especially important for Si because of the low absorption cross-section inherent to its indirect bandgap, which requires tens to hundreds of times thicker materials for complete absorption compared to direct bandgap material solar cells. The thicker structure also adversely affects carrier extraction due to bulk recombination, especially for less pure low cost materials. Furthermore, high aspect ratio structures allow core–shell radial p–n junctions, which effectively reduces the minority carrier collection path to be on the same order of the wire/pillar diameter [62,65]. The short collection path allows the use of low purity materials that have a short minority carrier diffusion length, thus lower the solar cell cost dramatically.

In contrast to bottom-up grown nanowires, MacEtched nanowires are produced without the need for infrastructures for crystal growth, which could offset some material cost resulting from removed portion of the material during etching. Notably, there is little risk of metal contamination due to its near room temperature nature. High quality Si nanostructures with desirable size, density, crystallographic orientation, and doping characteristics can be readily prepared on single or polycrystal Si substrates at the wafer scale. Texurization using Ag- or Pt-MacEtch on Si surfaces has already been demonstrated to be more effective than conventional alkaline roughening for antireflection coating [23,66–68]. In the following we highlight examples of high aspect ratio nanostructures produced by MacEtch for photovoltaic devices and discuss the characteristics each type of structure presents towards more efficient energy harvesting.

4.1. Planar p–n junction single and poly Si solar cells with MacEtched Si nanowires as antireflection coating

Peng et al. [44] reported photovoltaic devices based on Si nanowire arrays prepared on both single and poly crystalline Si substrate, where the Si nanowires were fabricated by Ag-MacEtch using $AgNO_3$ in aqueous HF solution in sealed vessels for 20 min at 50 °C. The height of the nanowires appears to be ~10 μm. The wafer used was p-type and nanowires were completely converted to n-type by post MacEtch thermal diffusion. Note the produced p–n junction in this case is in the planar Si as well as Si nanowires on top of the n-type layer serving as antireflection coating, as illustrated in Fig. 11a. An average reflectance of less than 2% was measured for the poly Si nanowires and <1.4% for single crystal Si NW sample, much lower than porous and polished Si surfaces in comparison (Fig. 10c). A power conversion efficiency of 9.31% (V_{oc} = 0.55 V, I_{sc} = 26.1 mA, FF = 0.65) for single crystal Si and 4.73% (V_{oc} = 0.48 V, I_{sc} = 21 mA, FF = 0.48) Si. Clearly, the conversion efficiency observed is still lower than those without nanowires and less than what the low reflectance implies. The authors believe that the low current-collection efficiency of the front grid electrodes (large longitudinal surface resistance) and ultrahigh surface area of the nanowires (reduced minority carrier lifetime and diffusion length) were possible reasons and could be improved.

4.2. 3D p–n junction Si nanowire based solar cells with MacEtch produced n-type Si nanowire core and ex situ deposited homojunction p-type poly Si or heterojunction p-type TiO_2 shell

Garnett and Yang [69] have reported Si nanowire radial pn junction solar cells, with single crystal n-Si nanowire core that are ~20 μm in height formed by $AgNO_3$ MacEtch and p-type poly Si shell from deposited amorphous Si that was subsequently annealed to poly Si (Fig. 12). Note that the same junction was formed in the planar part of the base in-between nanowires, thus we refer

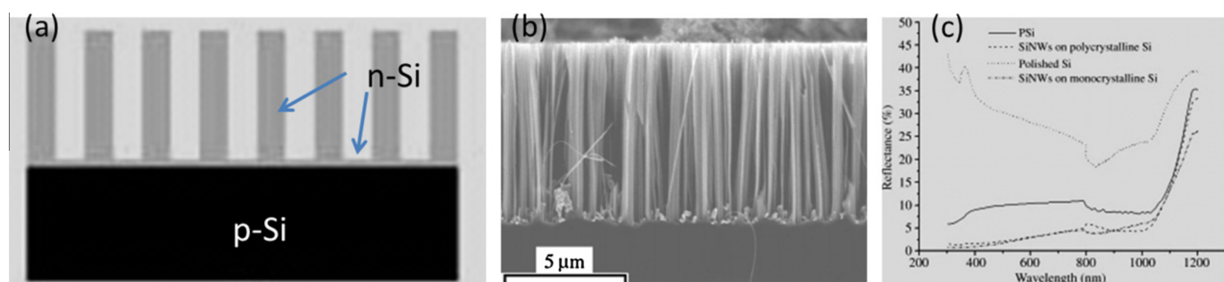

Fig. 11. (a) Schematic cell design with a p-Si nanowire wafer and a tray of n-type Si with n-type Si nanowires on top. (b) Cross-sectional SEM of an array of Si single crystalline nanowires produced by solution Ag-MacEtch. (c) Reflectance spectra for single and poly silicon nanowires, porous Si (Psi) and polished Si. Adapted from Ref. [44].

this type as 3D contoured junction. With a much bigger junction area than in Fig. 10, the cell efficiency reported was only 0.5%, with a Voc of 0.29 V and FF of 0.33. The low efficiency was mostly attributed to the high series resistance of the poly Si shell and high surface area related recombination. Interfacial recombination as indicated by the high dark current and high diode ideality factor (2.1) are also responsible for the low efficiency. Surface roughness resulted from Ag-MacEtch which resides right at the p–n junction interface could be detrimental to the performance. It is also possible that some nanowires located underneath the contacts were broken, exposing the underlying n-Si and leading to a reduced shunt resistance, which would also give a lower *V*oc and increased dark current. Nonetheless, the same low Voc was reported even when VLS grown Si nanowires were used, which appears to indicate that interface produced from smooth VLS wires vs Ag-MacEtched wires are similar.

The same group has investigated Si/TiO_2 core shell nanowire heterojunctions to determine their potential for photooxidation of water for hydrogen generation [70]. Photocurrent was enhanced by 2.5× compared to planar Si/TiO_2 structure due to their low reflectance and high surface area. Also, n-Si/n-TiO_2 exhibited larger photocurrent and Voc than p-Si/n-TiO_2 nanowires due to a barrier at the heterojunctions. TiO_2 was grown on Si NWs by ALD.

The radial p–n junction can be readily formed by post-MacEtch timed thermal diffusion. Shin et al. have systematically studied the diameter dependence of such a structure on the solar cell efficiency and a conversion efficiency of ~7% was realized with 2 μm diameter pillars without optimizing surface passivation [71].

4.3. Co-integrated MacEtched microwire (with diffused radial p–n junction) and nanowire (n-type) solar cells for improved light trapping

Jung et al. recently explored a structural composite of Silicon Si nanowires (NWs) and microwires (MWs) fabricated using MacEtch for solar cell applications [72]. MWs are periodically positioned using low-level optical patterning in between a dense array of NWs. Controlled tapering of the NWs results in additional optical enhancement via optimization of the tradeoff between increased light trapping (by a graded-refractive-index) and increased reflectance (by decreasing areal density of NWs). Fig. 13a shows the fabrication process flow and 13b shows the cross-section of such an array after MacEtch (or electroless etching – step 2 in Fig. 13a), and Fig. 13c shows an array that was further etched by KOH treatment for 60 s. A spin-on-doping technique was used for the formation of heavily doped, thin n-type shells for the MWs, while the entire nanowires were converted to n-type due to the small diam-

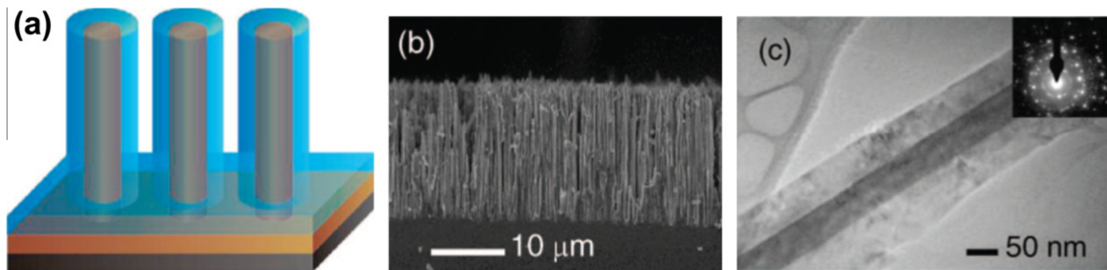

Fig. 12. (a) Schematic cell design with the single crystalline n-Si NW core in brown, the polycrystalline p-Si shell in blue, and the back contact in black. (b) Cross-sectional SEM of a completed device demonstrating excellent vertical alignment and dense wire packing. (c) TEM image showing the single crystalline n-Si core and polycrystalline p-Si shell. The inset is the selected area electron diffraction pattern. Adapted from Ref. [70].

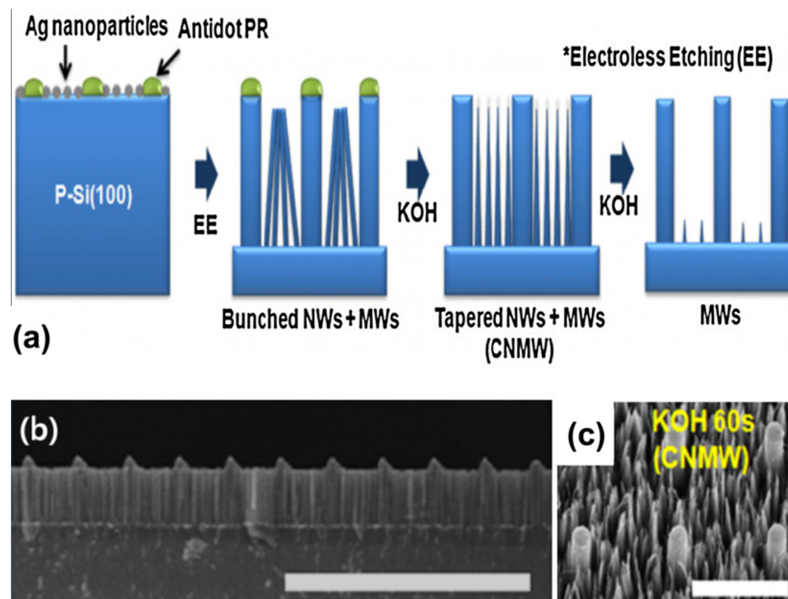

Fig. 13. (a) Schematic illustration showing the fabrication procedure for the co-integrated wire structure (CNMW) of MWs and tapered NWs: (1) Ag nanoparticles deposited by galvanic displacement after the formation of antidot PRs patterned by low-level optical lithography; (2) the CNMW formed by MacEtch; (3) formation of the CNMW structure consisting of tapered NWs with MWs in which the tapering is done by KOH etching for 60 s; (4) further KOH tapering for a total of 240 s results in the MWs remaining with only some NW residues. (b) Low-magnification cross-sectional scanning electron microscopy (SEM) image of the CNMW sample with a scale bar of 50 μm. (c) 30°-tilted view SEM image of CNMW after 60 s KOH etching of a MacEtched CNMW structure. The scale bars are 10 μm. Adapted from Ref. [73].

eters (Fig. 14a). The radial doping profile was confirmed by contrast in low voltage SEM images and SIMS profile. Compared to single NW (or MW) arrayed cells, the co-integrated nano and microwire (CNMW) solar cells demonstrate remarkably low reflectivity (Fig. 14b), improved photovoltaic performance, with a short circuit current of 20.59 mA cm^{-2} and a cell conversion efficiency of ~7.19% at AM 1.5G illumination (Fig. 14c).

4.4. 3D radial p–n junction Si nanohole based solar cells with nanohole array formed by MacEtch

In addition to nanowires or pillars produced by MacEtch, the inverse pattern, nanoholes, has been examined as potential candidate for high efficiency solar cell structures [73]. Shown in Fig. 15 is a wafer-scale ordered Si nanohole array fabricated by Ag-MacEtch with Ag dot pattern formed by deep ultraviolet lithography (UVL) on p-type Si(1 0 0) wafer. 3D radial p–n junction was formed by thermally diffusing phosphorous dopant on the top surface including the sidewalls of nanoholes, as depicted in Fig. 15c and d. The photovoltaic characteristics of a nanohole cell with 2 μm hole depth is shown in Fig. 15e and f, along with planar as well as pyramid-textured Si structures fabricated under identical conditions. The nanohole structure showed a power conversion efficiency of 9.51%, much higher than those from Si nanowires radial p–n junction solar cells of similar dimension. The authors believed that effective optical coupling between the nanohole array and the incident light as well as a large density of waveguide modes are responsible for the improved efficiency. In fact, it was calculated [74] that to obtain the same ultimate efficiency as a standard 300 μm crystalline silicon wafer, nanohole arrays require twelve times less Si by mass and nanohole arrays have an efficiency superior to nanorod arrays for practical thicknesses.

It is interesting to note that Si nanowire solar cells fabricated using the same etching technique but with the p–n junction deep within the wafer (as opposed to within the wire) in general showed a higher efficiency. Similar to bottom-up grown or dry etch

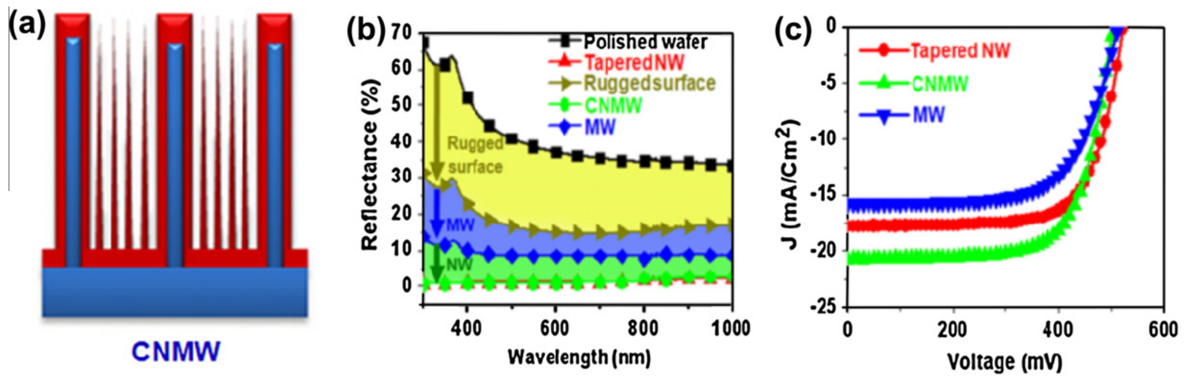

Fig. 14. (a) Illustration of the doping profile in co-integrated wire structure (CNMW) solar cell structure with red (blue) color represents n-type (p-type), (b) Optical reflectance spectra, and (c) typical *I–V* characteristics of tapered NW, CNMW, and MW solar cells. Colored areas present the effect of major principles for further suppressing the reflectance compared to a polished wafer, i.e. rugged surface (yellow), MWs (blue), NWs (green). Adapted from Ref. [73].

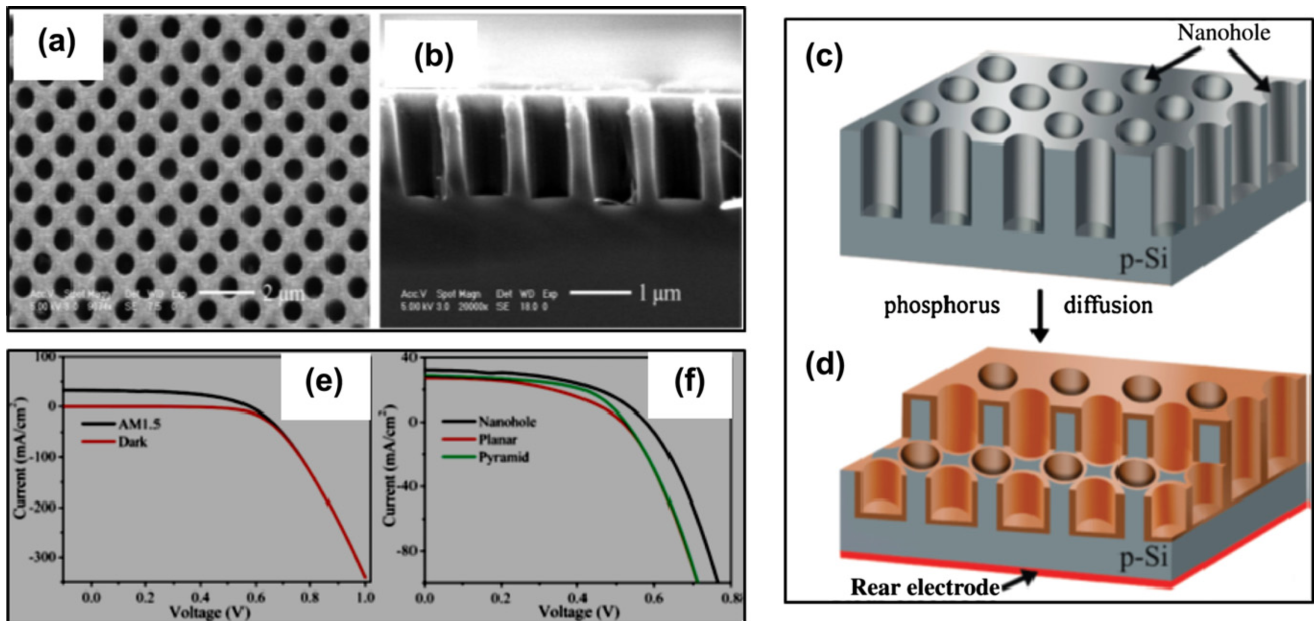

Fig. 15. (a and b) Top and side view SEM images of ordered silicon nanoholes produced by Ag-MacEtch using an 8–12 Ω cm p-Si(1 0 0) wafer, where Ag dot array was deposited in a mesh template fabricated by DUV lithography. (c and d) Sectional illustration of the process of fabricating the Si nanohole solar cell with radial p–n junctions via thermal phosphorus dopant diffusion. The n+ layer is shown in purple bronze, the p-Si substrate in gray, and the rear electrode in red; the front Ti/Pd/Ag grid electrode is not shown here. (e) *I–V* curves for Si nanohole solar cells in the dark and under Am1.5 illumination. (f) *I–V* curves for solar cells with different geometries fabricated under identical conditions for comparision. Adapted from Ref. [74].

fabricated nanowire solar cells, despite the ultralow reflectivity and high absorption for high aspect ratio structures, to the best of our knowledge, none of the reports so far demonstrated efficiencies that surpass commercial planar Si cells. It goes without saying that, the doping profile needs to be optimized to reduce bulk recombination and improve electrical resistance and top contact needs to have better transparency and lower resistance. However, the elephant in the room is probably surface passivation. This is because by making a nanowire solar cell, the surface area increases a significant percentage, 4 $\times$ aspect ratio $\times$ fill-factor. Therefore surface passivation is imperative to keep the surface recombination low, yet due to their small size and the fact that multiple facets with different crystalline orientation are exposed, passivating nanostructures has proven to be challenging. CVD deposited SiNx, thermally grown SiO_2, low temperature atomic layer deposition (ALD) grown Al_2O_3, and in situ deposited amorphous Si shell have been shown to lower the surface recombination rate by several orders of magnitude [75,76] and more development on this front is definitively much needed.

5. Concluding remarks

In summary, MacEtch is a simple, cost-effective, and powerful semiconductor etching technique that is capable of producing high aspect ratio semiconductor nanostructures. By combining with metal patterning lithography or non-lithographic patterning methods, accurate control of the nanowire orientation (vertical vs slanted), size (nano vs microscale), shape, architecture, density, length, doping characteristics can be achieved readily at wafer scale. More advancement in MacEtch controllability including cryogenic MacEtch [37], combination of MacEtch with conventional electrochemical etching [77], development of III–V, III–nitrides, as well as II–VI (no reports yet) semiconductor MacEtch can be expected. Many applications including solar cells, thermoelectrics, and other optoelectronics that involve structures that are currently fabricated by dry etch or bottom-up growth and assembly techniques, can benefit from this facile fabrication technique tremendously, including GaN based solar cells [78] and LEDs [79–81]. Although many challenges have to be addressed before the performance of MacEtched high aspect ratio structures exceeds that of its planar counterpart, the path is clear as progress in surface passivation, series resistance, uniformity, controllability continues to be made.

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