Metal-Density-Driven Placement for CMP Variation and Routability

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***Abstract*—In this paper, we propose the first metal-density-driven (MDD) placement algorithm to reduce chemical–mechanical planarization/polishing (CMP) variation and achieve higher routability. To efficiently estimate metal density and thickness, we first apply a probabilistic routing model and then a predictive CMP model to obtain the metal-density map. Based on the metal-density map, we use an analytical placement framework to spread blocks to reduce metal-density variation. Experimental results based on BoxRouter and NTUgr show that our method can effectively reduce the CMP variation. By using our MDD placement, for example, the topography variation can be reduced by up to 38% (23%) and the number of dummy fills can be reduced by up to 14% (8%), compared with those using wirelength-driven (cell-density-driven) placement. The results of our MDD placement can also lead to better routability.**

***Index Terms*—Manufacturability, physical design, placement, VLSI.**

I. Introduction

FOR 90 nm and more advanced process technologies, manufacturability and yield-related issues are becoming more and more important. In particular, topography (thickness) variation after chemical–mechanical planarization/polishing (CMP), i.e., CMP variation, is shown to be systematically determined by wire-density distribution [23], [27], [33]. Even after CMP, intrachip topography variation can still be on the order of 20%–40% [18], [27]. Such a topography variation leads to not only increased wire resistance and capacitance but also serious manufacturing issues like etching and printability [18], [27], [30]. Therefore, it is essential to have more uniform copper (Cu) thickness of interconnect, so that timing analysis in the early stages can be more accurate, and thus, timing can be optimized more effectively.

Effectively distributing pins and cells into a placement region with metal-density consideration can provide more flexibility for routing, leading to better metal-density topography. Without considering metal density during placement, routers may fail to optimize metal density because of inferior pin locations, which is observed by Cho *et al.* [11]. The task of a router is to complete all the connections among pins. As a result, it cannot avoid routing through some highly dense region in which a pin lies.

In addition to wirelength, there are many recent works on placement optimizing for cell density [9], [29], congestion [24], [28], [32], and timing [19]. However, none of them considers metal-density and CMP variation. Cell density has been considered for placement [2], [9], [29], but it cannot address metal density well. Since the wire density among cells of a functional unit is usually much higher than the wire density between cells of different functional units, simply distributing cells evenly cannot guarantee uniform metal density. Congestion and metal density are closely related, but a congestion-driven placement still cannot reflect metal density directly and effectively. It has been shown that even under the same routing congestion, metal densities are very different when wide wires exist [11]. Since no previous work focuses on metal-density optimization, it shows the importance of our work. Note that metal density and wire density are related; metal density consists of both wire density and dummy fill density, and metal-density distribution is thus the major factor that affects CMP results. Consequently, we shall optimize metal-density distribution directly (instead of wire density since it cannot directly address the metal density).

In this paper, we propose a metal-density-driven (MDD) placement algorithm for CMP variation and routability optimization. Because metal density needs to be estimated and updated frequently during the placement process, an efficient approach is required. Therefore, we use a probabilistic routing model [25], [31] and a predictive CMP model [11] to evaluate metal density. Then, the metal-density map is used to guide block (cell/macro) spreading to find a uniform metal-density result. Note that our placement approach is not limited to the probabilistic routing model and the predictive CMP model. To increase the accuracy, a global router and/or an accurate CMP simulator, such as in [15], can be used. Five adaptec benchmarks [2] are used to conduct our experiments. The placement results are routed by BoxRouter [10] and NTUgr [4]. The results show that our MDD placement can effectively

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TABLE I
NOTATIONS IN THIS PAPER

$V = \{v_1, v_2, ..., v_n\}$	blocks (cell/macro)
$E = \{e_1, e_2, ..., e_m\}$	nets
x_i, y_i	center coordinate of block v_i
w_i, h_i	width and height of block v_i
w_b, h_b	width and height of bin b
P_b	area of preplaced blocks in bin b
D_b	area of movable blocks in bin b
D_b^{max}	the maximum allowable area in bin b
R_b^v, R_b^h	the wire density in the vertical/horizontal routing layer of bin b
M_b^v, M_b^h	the metal (wire + dummy) density in the vertical/horizontal routing layer of bin b
u^h	the average metal width for horizontal routings
u^v	the average metal width for vertical routings
$t_{density}$	target cell density

reduce the topography variation by up to 38% (23%), compared with wirelength-driven (WLD) [cell-density-driven (CDD)] placement. In addition, the experimental results also show that the MDD placement can lead to higher routability. All circuits placed by the MDD placement do not have any routing overflow, while only one (three) circuit placed by the WLD (CDD) placement has no overflow. Higher routability from our MDD placement enables BoxRouter to achieve 33.4× (4.7×) speedup, compared with BoxRouter with the WLD (CDD) placement. These results show that our MDD placement is effective in improving both CMP variation and routability.

The remainder of this paper is organized as follows. Section II gives essential background for analytical placement, CMP model, and metal-density estimation. Our MDD placement algorithm is explained in Section III. Section IV reports the experimental results. Finally, the conclusions are given in Section V.

II. PRELIMINARIES

We describe the placement model, placement metrics, and the predictive CMP model in the following.

A. Placement Model

We use a hypergraph $H = (V, E)$ to model a circuit. Let vertices $V = \{v_1, v_2, \ldots, v_n\}$ represent blocks (cells and macros), and let hyperedges $E = \{e_1, e_2, \ldots, e_m\}$ represent nets. Let x_i and y_i be the x- and y-coordinates of the center of block v_i, respectively. The circuit may contain some *preplaced blocks* which have fixed x- and y-coordinates and cannot be moved. Table I gives the notation used in this paper.

B. Placement Metrics

The main purpose for placement is to find desired positions for all blocks such that some placement metrics are optimized. The following gives important placement metrics for modern circuit designs.

1) **Wirelength** is the main objective for placement. Usually shorter wirelength leads to better routability and timing. However, considering total wirelength alone is not enough for modern circuit designs. For example, squeezing blocks can reduce total wirelength but may be harmful for routability.
2) **Routability** is an important metric for both placement and routing. A placement with high routability can reduce routing time and result in fewer routing detours. It is important to have fewer routing detours so that the wirelength estimation in the placement stage can be more accurate.
3) **Cell density** is also an important consideration for modern placement. Since buffer insertion and gate sizing are commonly used in modern designs, some whitespace should be reserved for further optimization.
4) **Manufacturability** also needs to be considered in the placement stage for nanometer designs. Cell/macro positions can roughly determine the wire-density distribution. To effectively reduce the CMP variation, we shall consider cell/macro positions.

C. Predictive CMP Model

We use the predictive CMP model proposed in [11]. The metal thickness variation after CMP is determined by metal density that includes both wires and dummies. The number of dummy fills depends on wire density. Thus, we can predict the resulting normalized copper (Cu) thickness from the wire density. The normalized Cu thickness T_{Cu} can be computed by

$$T_{\mathrm{Cu}} = \alpha \left(1 - \frac{M_b^2}{\beta}\right), \qquad 0.2 \le M_b \le 0.8 \tag{1}$$

where M_b is the metal density of a bin, and α and β are technology-dependent constants. The metal density M_b includes the wire density and the dummy density in a bin. Fig. 1 shows the required dummy density and the predicted Cu thickness with respect to the wire density. Given the wire density R_b, we can look up the number of dummy fills to be inserted to obtain the total metal density M_b. Then, the final Cu thickness can be predicted using (1). This predictive model has been verified with a commercial CMP simulator [5] and industry test cases.

III. MDD PLACEMENT

Our MDD placement is based on an analytical placer. We use metal-density-aware spreading forces to guide block spreading to reduce CMP variation. Fig. 2 shows our placement framework. The wire density is updated during the placement process based on the predictive CMP model described in Section II-C.

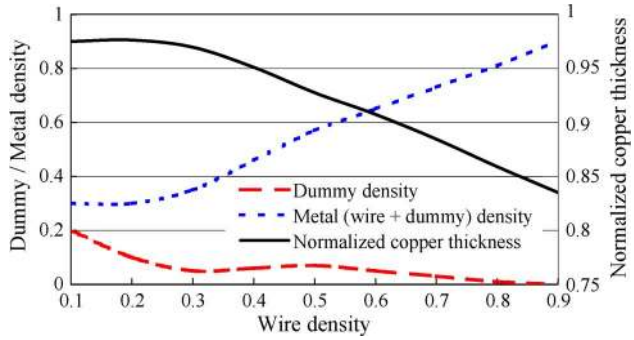

Fig. 1. Predictive CMP model.

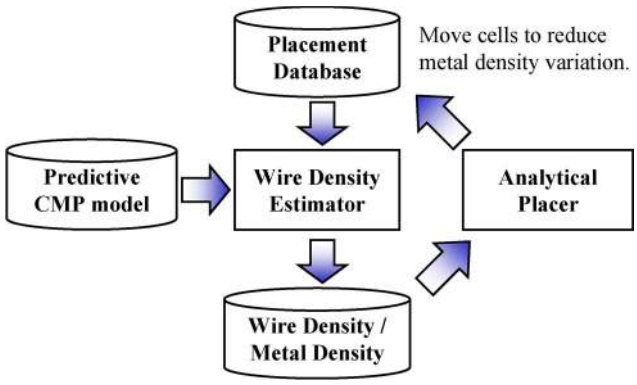

Fig. 2. Our MDD placement framework.

Then, the metal-density topography is used in the analytical placer to move blocks to reduce metal-density variation. Then, block coordinates are updated into the placement database for the next placement iteration.

A. Placement Framework

The analytical placement framework optimizes wirelength and spreads blocks to reduce the overlaps between blocks [9]. To evenly distribute the blocks, we divide the placement region into uniform nonoverlapping bin grids. Then, the global placement problem can be formulated as a constrained minimization problem as follows:

$$\begin{aligned} \min \quad & W(V,E) \\ \text{s.t.} \quad & D_b(V) \le D_b^{\max}, \qquad \text{for each bin } b \end{aligned} \tag{2}$$

where $W(V,E)$ is the wirelength function, $D_b(V)$ is the potential function that is the total area of movable blocks in bin b, and $D_b^{\max}$ is the maximum allowable area of movable blocks in bin b. $D_b^{\max}$ can be expressed as

$$D_b^{\max} = t_{\text{density}}(w_b h_b - P_b) \tag{3}$$

where t_{density} is a user-specified target cell density value for each bin ($t_{\text{density}} < 1.0$), $w_b(h_b)$ is the width (height) of bin b, and P_b is the *base potential*. The base potential equals the preplaced block area to prevent blocks from being overlapped with preplaced blocks.

The wirelength $W(V,E)$ is defined as the total half-perimeter wirelength (HPWL) as follows:

$$W(V,E) = \sum_{e \in E} \left(\max_{v_i, v_j \in e} |x_i - x_j| + \max_{v_i, v_j \in e} |y_i - y_j| \right). \tag{4}$$

Since $W(V,E)$ is not smooth and nonconvex, it is hard to minimize it directly. Thus, several smooth wirelength approximation functions are proposed, such as quadratic wirelength [14], [22], L_p-norm wirelength [6], [21], and log-sum-exp wirelength [7], [9], [20], [26]. Since recent results show that the log-sum-exp wirelength model achieves the best results among these three models [7], [9], we apply the log-sum-exp wirelength model in our placer.

We express the function $D_b(V)$ as

$$D_b(V) = \sum_{v \in V} P_x(b,v) P_y(b,v) \tag{5}$$

where P_x and P_y are the overlap functions of bin b and block v along the x- and y-directions. However, the overlap functions P_x and P_y are neither smooth nor differentiable. We adopt the bell-shaped potential function $\tilde{P}_x$ to smooth P_x. The bell-shaped function was first proposed in [26] and then was extended to handle mixed-size blocks in [20]. We use the later version of the bell-shaped function $\tilde{P}_x$, which is defined by

$$\tilde{P}_x(b,v) = \begin{cases} 1 - p l_x^2, & 0 \le l_x \le \frac{w_v}{2} + w_b \\ q\left(l_x - \frac{w_v}{2} - 2w_b\right)^2, & \frac{w_v}{2} + w_b \le l_x \le \frac{w_v}{2} + 2w_b \\ 0, & \frac{w_v}{2} + 2w_b \le l_x \end{cases} \tag{6}$$

where

$$\begin{aligned} p &= \frac{4}{(w_v + 2w_b)(w_v + 4w_b)} \\ q &= \frac{2}{w_b(w_v + 4w_b)} \end{aligned} \tag{7}$$

where w_b is the bin width, w_v is the block width, and l_x is the center-to-center distance of the block v and the bin b in the x-direction.

The quadratic penalty method is used to solve (2), implying that we solve a sequence of unconstrained minimization problems of the form

$$\min \quad W(V,E) + \lambda \sum_{\forall b} (D_b(V) - D_b^{\max})^2 \tag{8}$$

with increasing λ's. The solution of the previous problem is used as the initial solution for the next one. We solve the unconstrained problem in (8) by the conjugate gradient (CG) method.

B. Metal-Density Estimation

To compute the metal density, we need to know the wire density first. Based on the bin structure, the wire density of a

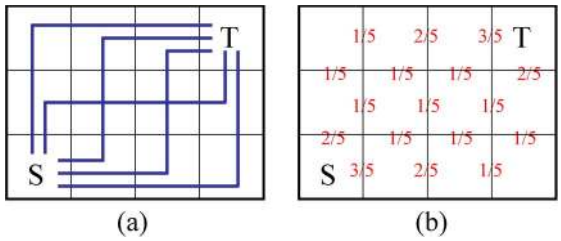

Fig. 3. Probabilistic routing model for a two-pin net from S to T. (a) Five possible L- and Z-shaped routings. (b) The expected track usage for each edge.

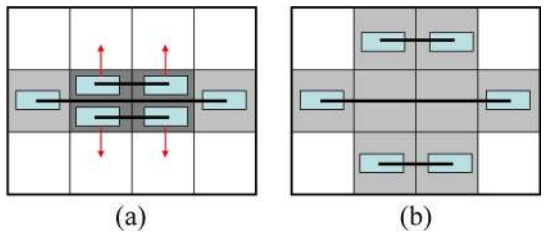

Fig. 4. Concept of reducing the wire density. (a) The blocks in the high metal-density regions receive forces to leave the region. (b) After moving blocks, a more uniform wire-density result is obtained.

bin can be computed by the numbers of tracks going through four edges of the bin. Let t_b^l, t_b^t, t_b^r, and t_b^b be the numbers of tracks going through the left, top, right, and bottom edge of the bin b, respectively. In each bin, we use two layers, a vertical routing layer and a horizontal routing layer, to compute the wire density (we will extend the computation to multiple layers in Section III-F.). The average wire density R_b^v in the vertical routing layer of bin b can be estimated by

$$R_b^v = u^v \left(\frac{t_b^t + t_b^b}{2w_b} \right) + B_b^v \tag{9}$$

and the average wire density R_b^h in the horizontal routing layer of bin b is

$$R_b^h = u^h \left(\frac{t_b^l + t_b^r}{2h_b} \right) + B_b^h \tag{10}$$

where $u^v(u^h)$ is the average metal width for vertical (horizontal) routing, $w_b(h_b)$ is the bin width (height), and $B_b^v(B_b^h)$ is the base density of the vertical (horizontal) routing layer contributed by the internal routing of the cells/macros, which can be extracted from the standard cell layout. After obtaining the wire density, we can use the predictive CMP model to compute the metal density and the resulting Cu thickness.

To predict the expected horizontal/vertical track usage for each bin, we first decompose multiterminal nets into Steiner trees using FLUTE [12], [13]. Then, the track usage for each two-pin net is estimated by the probabilistic routing model [25], [31]. Fig. 3 shows an example. For a two-pin net from S to T, there are two possible L-shaped routes and three possible Z-shaped routes. The expected track usage for each edge is computed by the number of possible routes that goes through it divided by the number of the total possible routes.

C. Metal-Density-Aware Block Spreading

To reduce the metal-density variation, the placement needs to have uniform wire density. We use Fig. 4 to illustrate the concept of reducing the wire-density variation. Usually, the high wire-density region is caused by not only local nets but also global nets. In Fig. 4(a), there are three nets in the central region, two local nets and one global net. Then, extra forces are applied to the blocks in the central region to push out blocks from this region to obtain the result in Fig. 4(b). As a result, the metal density in the central region is reduced, and a more uniform metal-density result is obtained.

The MDD placement problem can be formulated as a constrained minimization problem as follows:

$$\begin{aligned} \min \quad & W(V,E) \\ \text{s.t.} \quad & D_b(V) \le D_b^{\max}, \qquad \text{for each bin } b, \\ & M_b^v(V) \le M_b^{v,\max} \\ & M_b^h(V) \le M_b^{h,\max} \end{aligned} \tag{11}$$

where $W(V,E)$ is the wirelength function, $D_b(V)$ is the total area of movable blocks in bin b, $D_b^{\max}$ is the maximum allowable area of movable blocks in bin b, $M_b^v(M_b^h)$ is the metal density in the vertical (horizontal) routing layer in bin b, and $M_b^{v,\max}(M_b^{h,\max})$ is the maximum allowable metal density in the vertical (horizontal) routing layer in bin b.

We could use the quadratic penalty method to solve the problem

$$\begin{aligned} \min \quad & W(V,E) + \lambda_1 \sum_{\forall b} (D_b(V) - D_b^{\max})^2 \\ & + \lambda_2 \sum_{\forall b} (M_b^v(V) - M_b^{v,\max})^2 \\ & + \lambda_3 \sum_{\forall b} \left(M_b^h(V) - M_b^{h,\max} \right)^2. \end{aligned} \tag{12}$$

However, the gradients of $\sum_{\forall b}(M_b^v(V) - M_b^{v,\max})^2$ and $\sum_{\forall b}(M_b^h(V) - M_b^{h,\max})^2$ provide extra forces on blocks, and the weights of λ_1, λ_2, and λ_3 are not easy to be determined. As a result, the approach may not converge to an evenly distributed placement or cause numerical instability. To prevent the aforementioned problem, we add extra forces implicitly by modifying the base potential P_b to maintain the stability of the nonlinear solver. The original base potential P_b considers only preplaced blocks, while the metal-density-aware base potential P_b^m considers both preplaced blocks and metal density. We have

$$P_b^m = \min(P_b + \kappa M_b, w_b h_b) \tag{13}$$

where

$$M_b = \left(M_b^v - \min_{\forall b} M_b^v \right) + \left(M_b^h - \min_{\forall b} M_b^h \right) \tag{14}$$

and κ is a parameter to control the strength of the metal-density-aware forces. The value of P_b^m is restricted to be less than the area of bin b to ensure the numerical stability. Then, we use the

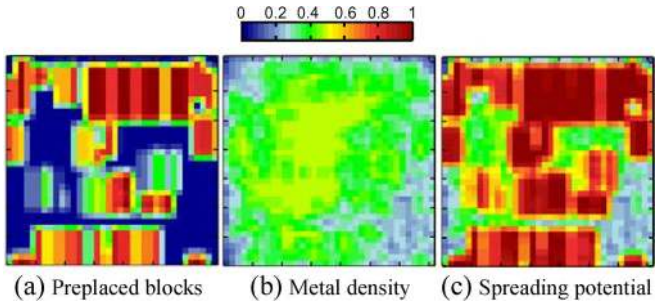

Fig. 5. Metal-density-aware base potential generation. (a) The preplaced block density. (b) The predicted metal density. (c) The base potential considering both (a) and (b).

new base potential to compute the maximum allowable block area $D_b^{m,\max}$

$$D_b^{m,\max} = t_{\text{density}}\left(w_b h_b - P_b^m\right). \tag{15}$$

As a result, the placement problem becomes

$$\min \quad W(V,E) + \lambda \sum_{\forall b} \left(D_b(V) - D_b^{m,\max}\right)^2. \tag{16}$$

We can adjust κ in (13) according to the total available whitespace of the design. The total maximum allowable block area in a placement region must be large enough to contain all movable blocks, i.e.,

$$\sum_{\forall b} D_b^{m,\max} \geq \text{area\_of\_all\_movable\_blocks}. \tag{17}$$

If we set κ larger, we may have a more uniform metal-density result, but the resulting wirelength may be worse. This parameter controls the tradeoff between the wirelength and the metal-density variation. The effects of adjusting κ will be reported in Section IV.

Fig. 5 shows an example of computing the metal-density-aware base potential. Fig. 5(a) and (b) shows the preplaced block density and the predicted metal density, respectively. Summing up the two density values using (13), we can obtain the resulting base potential as shown in Fig. 5(c).

D. Base Potential Smoothing

A smooth objective function helps the gradient method to find a desired solution. Thus, we need to smooth the base potential to achieve better solutions. We apply the two-stage smoothing technique [9], *Gaussian smoothing* followed by *level smoothing* to smooth metal-density-aware base potential.

We use Fig. 6 to explain our smoothing method. First, Gaussian smoothing is applied to the configuration of Fig. 6(a), and avoid the dramatic change in the landscape to obtain the configuration of Fig. 6(b). Then, level smoothing is applied to reduce the potential levels to obtain the configuration of Fig. 6(c).

Gaussian smoothing works as a low-pass filter, which can smooth the local potential change. The 2-D Gaussian has

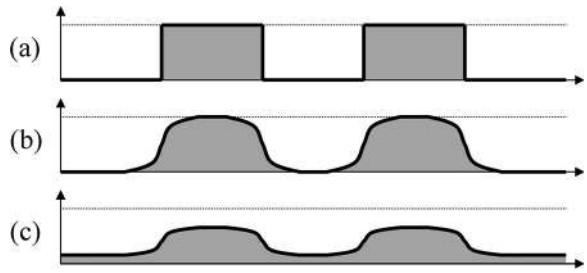

Fig. 6. Two-step smoothing example. (a) Original density. (b) After Gaussian smoothing. (c) After level smoothing.

the form

$$G(x,y) = \frac{1}{2\pi\sigma^2} e^{-\frac{x^2+y^2}{2\sigma^2}} \tag{18}$$

where σ is the standard deviation of the distribution. Applying convolution $(*)$ to the Gaussian function G with the base potential P

$$S(x,y) = G(x,y) * P(x,y) \tag{19}$$

we can obtain a smoother base potential S. The value σ defines the smoothing range. A larger σ leads to a more smooth potential. In global placement, the smoothing range gradually decreases so that the smoothed potential approaches the exact density gradually.

After the Gaussian smoothing, we apply another landscape smoothing function [17] to reduce the potential levels. As a result, the final smoothed based potential $\tilde{P}$ is given by

$$\tilde{P}(x,y) = \begin{cases} \overline{S} + \left(S(x,y) - \overline{S}\right)^{\delta} & \text{if } S(x,y) \geq \overline{S} \\ \overline{S} - \left(\overline{S} - S(x,y)\right)^{\delta} & \text{if } S(x,y) < \overline{S} \end{cases} \tag{20}$$

where $\overline{S}$ is the average value of $S(x,y)$, and $\delta \geq 1$. We normalize S so that every S is between 0 and 1 to ensure $|S(x,y) - \overline{S}| < 1.0$. Smoothing potential levels reduces the height of high potential regions so that movable blocks can spread to the whole placement region smoothly.

In summary, there are three parameters for generating smoothing metal-density-aware base potential. These three parameters are controlled empirically as follows.

1) κ controls the strength of the metal-density-aware forces by allocating whitespace for the metal-density-aware base potential. The amount of allocated whitespace gradually increases to the user-specified whitespace ratio during the placement.
2) σ controls the range of the Gaussian smoothing. The smoothing range starts from 15% of the chip width and gradually decreases to around 1% of the chip width.
3) δ controls the degree of level smoothing. It decreases from 5 to 1. When $\delta = 1$, there is no level smoothing.

E. Placement Flow

Fig. 7 shows our placement flow. Our MDD placement is based on a multilevel analytical placement framework. First, we iteratively cluster blocks to obtain the hierarchy. The cluster

Multilevel Metal-Density Driven Placement

Input: a circuit hypergraph
Output: desired block positions

```
01. Create the clustering hierarchy;
02. Initialize block positions;
03. do
04.     Initialize the bin structure and λ;
05.     do
06.         Update smoothing parameters;
07.         // Find min W(V,E) + λ Σ(D_b(V) − D_b^{m,max})^2;
08.         do
09.             Compute the conjugate gradient direction;
10.             Update current block positions;
11.             Estimate wire and metal density;
12.             Update base potential;
13.         until (the minimal value is found);
14.         Increase λ by 2;
15.     until (spreading enough);
16.     Decluster blocks;
17. until (all clusters are declustered);
18. Legalize the placement;
19. return block positions;
```

Fig. 7. Our MDD placement flow.

positions are initialized by solving the minimum quadratic wirelength, which is widely used in quadratic placement.

There are three loops in the placement flow.

1) The first loop is the multilevel loop (in lines 3–17). The bin dimension is initialized so that the number of bins is proportional to the number of clusters in the current level. After finding the placement of the current level, the circuit hierarchy is declustered once.
2) The second loop is the block spreading loop (in lines 5–15). The smoothing parameters κ, σ, and δ are updated in this loop. Then, the value of λ_m in (8) gradually increases inside the loop to spread blocks to the desired positions.
3) The third loop is to find the minimal value of (8) by the CG method (in lines 8–13). Since all clusters/blocks are moving inside this loop, we need to update the metal-density map (line 10) and the corresponding base potential (line 11) inside this loop.

The placement progress continues until all clusters are declustered and the value of (8) cannot be further reduced. Then, we legalize the placement by removing all overlaps and report the final result.

F. Extension of Handling Multiple Metal Layers

In modern VLSI designs, there are usually multiple metal layers. Our method can be extended to optimize multiple metal layers directly. First, a fast 3-D global router is needed to find the number of tracks used for each edge of the bin in each layer. Based on the track usage, we can use (9) and (10) to compute the wire density for each layer. Then, (14) can be modified as

$$M_b = \sum_{\forall l} w^l \left(M_b^l - \min_{\forall b} M_b^l \right) \tag{21}$$

where M_b^l is the metal density of bin b in layer l and w^l is the weight of the layer l. Because it is important to have smaller metal-density variation for lower layers [16], we can set higher weights for lower layers than those of upper layers. After computing the new M_b, the new base potential P_b^m and the maximum allowable block area $D_b^{m,\max}$ can be computed by

$$P_b^m = \min(P_b + \kappa M_b, w_b h_b) \tag{22}$$

$$D_b^{m,\max} = t_{\text{density}} \left(w_b h_b - P_b^m \right). \tag{23}$$

Then, the multilayer MDD placement problem can be solved by finding the minimum value of

$$\min \quad W(V,E) + \lambda \sum_{\forall b} \left(D_b(V) - D_b^{m,\max} \right)^2. \tag{24}$$

TABLE II
BENCHMARK STATISTICS

Circuit	Placement Mov #	Placement Fixed #	Placement Net #	Placement Util. (%)	Routing Track #	Routing B.P.† (%)
adaptec1	211k	543	221k	57	35	50
adaptec2	254k	566	266k	44	35	20
adaptec3	451k	723	467k	33	30	50
adaptec4	495k	1329	516k	27	30	50
adaptec5	842k	646	868k	49	50	20

† macro block porosity

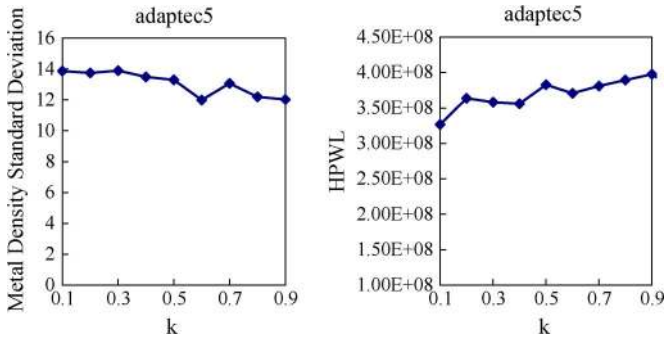

Fig. 8. Metal-density standard deviation and HPWL versus κ for adaptec5.

IV. EXPERIMENTAL RESULTS

We implemented the proposed algorithm in C++ by augmenting the placer NTUplace3 [9]. All the experiments were performed on a 2.2-GHz AMD Opteron machine. The adaptec benchmarks are taken from the ISPD'05/06 placement contest [1], [2].[1] The circuit information is shown in Table II. The number of movable blocks ranges from 211k to 842k, and the number of nets ranges from 221k to 868k. The design utilization rate ranges from 27% to 57%. We follow the routing configurations used in the ISPD 2007 routing contest [3]. Six metal layers are assumed, and only 20% wire tracks are available for routing in metal layers 1 and 2. The size of the global routing tile in terms of track numbers (Track#) and

[1]We did not take bigblue or newblue suites because several circuits are still unroutable (including bigblue4, newblue3, newblue4, and newblue7), according to the results from ISPD Placement Contest 2008 [4]. The most important reason is that the positions of fixed pins in some circuits are not reasonable. For example, in newblue3, there are many fixed pins in a routing cell, and the track usage near that routing cell has huge overflows. These overflows result in unreasonable copper thickness estimation. Therefore, we did not use bigblue and newblue suites.

TABLE III
COMPARISONS OF OUR PLACER USING DIFFERENT MODES FOR THE ADAPTEC BENCHMARKS

	Wirelength-Driven (WLD)											
	Placement		Routing				CMP (Hori. Layer)			CMP (Vert. Layer)		
Circuit	HPWL (× e7)	CPU (min)	WL (× e7)	WL/ HPWL	Over-flow	CPU (min)	Dummy	Cu-Avg	Cu-Std	Dummy	Cu-Avg	Cu-Std
adaptec1	8.15	14	11.87	1.46	0	711	5984	0.95	3.16	6034	0.95	3.09
adaptec2	9.02	15	12.38	1.37	2758	2279	13567	0.96	3.84	13644	0.96	4.03
adaptec3	22.35	32	26.27	1.18	938	140	45432	0.96	7.48	43843	0.96	7.78
adaptec4	20.02	29	22.38	1.12	31	1839	51258	0.96	7.81	50322	0.96	7.73
adaptec5	36.09	76	47.36	1.33	26672	2386	16766	0.96	5.73	16462	0.96	5.70
Comp.	0.81	0.76	0.89	1.29	—	33.42	1.06	1.00	1.12	1.06	1.00	1.11
	Cell-Density Driven (CDD)											
	Placement		Routing				CMP (Hori. Layer)			CMP (Vert. Layer)		
Circuit	HPWL (× e7)	CPU (min)	WL (× e7)	WL/ HPWL	Over-flow	CPU (min)	Dummy	Cu-Avg	Cu-Std	Dummy	Cu-Avg	Cu-Std
adaptec1	9.20	15	12.12	1.32	0	130	5929	0.95	3.09	5986	0.95	3.14
adaptec2	10.32	17	13.08	1.27	0	208	13166	0.96	3.50	13248	0.96	3.83
adaptec3	27.42	28	31.19	1.14	28	1119	43575	0.96	7.24	42096	0.96	7.44
adaptec4	22.61	52	24.67	1.09	0	30	49078	0.96	7.36	48174	0.96	7.18
adaptec5	38.90	67	49.62	1.29	875	1788	15972	0.96	4.58	15560	0.96	4.54
Comp.	0.92	0.90	0.96	1.22	—	4.67	1.02	1.00	1.03	1.02	1.00	1.03
	Metal-Density Driven (MDD)											
	Placement		Routing				CMP (Hori. Layer)			CMP (Vert. Layer)		
Circuit	HPWL (× e7)	CPU (min)	WL (× e7)	WL/ HPWL	Over-flow	CPU (min)	Dummy	Cu-Avg	Cu-Std	Dummy	Cu-Avg	Cu-Std
adaptec1	9.41	17	11.54	1.23	0	42	5914	0.95	3.02	5927	0.95	3.03
adaptec2	11.63	23	13.63	1.17	0	28	12913	0.96	3.36	12952	0.96	3.69
adaptec3	30.35	38	34.10	1.12	0	121	42253	0.96	7.06	40525	0.96	7.24
adaptec4	26.40	35	28.69	1.09	0	28	46481	0.96	7.05	45741	0.96	7.03
adaptec5	39.82	110	48.73	1.22	0	707	16198	0.96	4.52	15687	0.96	4.45
Comp.	1.00	1.00	1.00	1.17	—	1.00	1.00	1.00	1.00	1.00	1.00	1.00

macroblock porosity (Blk.) is shown in the last two columns of Table II. The block porosity defines the remaining amount of routing resource above macroblocks in metal layers 3 and 4. Three experiments were conducted. In the first experiment, we studied the tradeoff between HPWL and metal-density standard deviation by adjusting the parameter κ described in Section III-C. In the second experiment, we compared our MDD placement with two other placement methods. For this experiment, BoxRouter was used to perform global routing,[2] and Cu thickness variation was evaluated by the predictive CMP model [11]. In the last experiment, we further used two recent state-of-the-art routers, NTUgr [4] and BoxRouter-2008 [4], which were the second and the fourth places of the 2008 ISPD Global Routing Contest to perform global routing and evaluate the CMP variations.

A. Tradeoff Between HPWL and Metal-Density Variation

Since κ controls the force strength to even the metal density implicitly in (13), we can adjust the force strength by controlling κ. Fig. 8 shows the resulting HPWL and the metal-density standard deviation using different κ's for the circuit adaptec5. We only show the results of adaptec5 since all other circuits have the same trend.[3] The x-axis is normalized by the amount of whitespace used. For example, the number 0.9 means that κ is adjusted to use 90% whitespace for metal-density-aware base potential. From the figure, when κ is larger, the resulting metal-density standard deviation is smaller but the HPWL is longer. The resulting metal-density standard deviation can be reduced by 15%, while HPWL is increased by 18% when 90% whitespace is used for metal-density-aware spreading forces. The results also show that the resulting metal-density variation depends on the amount of available whitespace. If there is not enough whitespace for the design, our MDD placement algorithm may have only minor improvement.

B. Comparison Between Different Placement Algorithms

Since there is no previous work on CMP-aware placement, we compared three different placement modes based on our placer, the WLD, CDD, and MDD modes. The WLD placement optimizes wirelength alone with the target cell density $u = 1.0$. For the CDD placement, we set the target cell density to its design utilization rate to evenly spread blocks to the whole chip region. The MDD placement algorithm is described in Section III.[4] The parameter κ is set to use 90% whitespace for the metal-density-aware base potential. Table III gives the placement, routing, and CMP results on the adaptec benchmarks. "HPWL" is the HPWL after placement, while "WL" is the total wirelength after global routing. "WL/HPWL" is the ratio of WL and HPWL, which stands for the wirelength increase after global routing. "Overflow" is the number of total routing overflows after global routing. The overflow is defined

[2]We used the default parameters for BoxRouter, which may spend more runtime to achieve fewer overflows. Note that BoxRouter completed the routing for most circuits with zero overflows in the ISPD'07 routing contest [3].

[3]The curves in Fig. 8 are not monotonic because nonlinear optimization cannot guarantee the optimal solution and results in slight quality difference.

[4]Although there are six metal layers in the circuits, the probabilistic routing model can only predict the track usages for horizontal/vertical directions. Therefore, we applied the two-layer model in Section III-C instead of the multilayer model in Section III-F for our experiments.

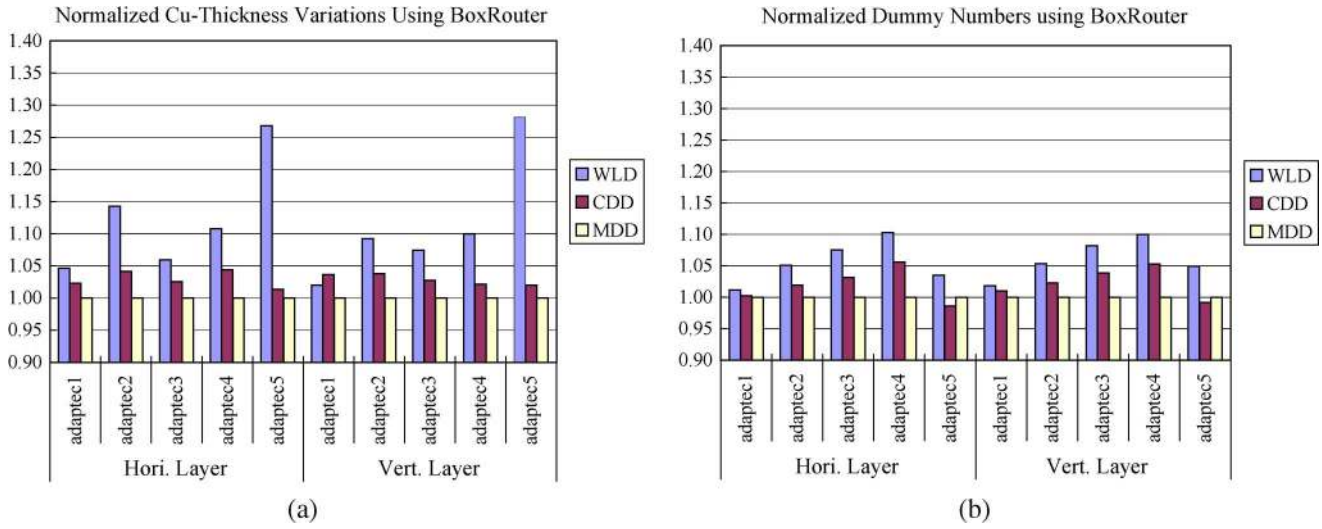

Fig. 9. CMP results using BoxRouter. (a) Normalized Cu thickness variations. (b) Normalized dummy numbers.

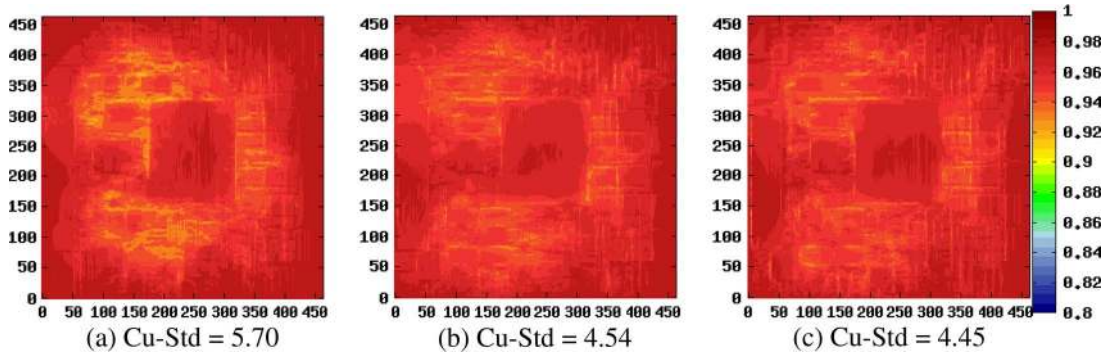

Fig. 10. Normalized Cu thickness map in the vertical routing layer for adaptec5 using (a) WLD placement, (b) CDD placement, and (c) MDD placement.

as the sum of the number of tracks that exceeds the routing capacity for each edge of the global routing tiles. "Dummy" is the number of dummy fills based on the predictive CMP model. "Cu-Avg" and "Cu-Std" are the average and standard deviation of the normalized copper thickness, respectively.

CMP. The average Cu thicknesses are similar for the three placement modes. Compared with WLD's variation, CDD averagely reduces 13% variations of the Cu thickness, and MDD can further reduce 3% more, 11%–12% in total, variations. In addition to Cu thickness variation reduction, the total number of dummy fills for MDD is 2% less than CDD's and 6% less than WLD's. It is important to have fewer dummy fills because it not only can increase circuit performance by reducing coupling capacitance but also can save manufacturing cost by decreasing its mask data volume. From the experimental results, we can see that cell density bears some correlation with metal density, but cell density still cannot address metal density well. Compared with CDD placement, the metal-density one can further reduce about 4%–23% Cu thickness variations. Fig. 9(a) and (b) shows the resulting normalized Cu thickness variations and normalized total numbers of dummy fills, respectively.

Wirelength. The MDD's HPWL is 8% longer than CDD's and 19% longer than WLD's. After global routing, the MDD's WL is 4% longer than CDD's and 11% longer than WLD's. However, it should be noted that since there are still some overflows in CDD's and WLD's routing results, it is not fair to simply compare the WL, as each overflow can cause significant overheads in final (detailed) wirelength. For the ratio of WL/HPWL, MDD incurs only a 17% increase, while CDD and WLD incur 22% and 29% increases in wirelength, respectively. The difference in wirelength increases is mainly because of routing detours, implying that there are more detours in CDD's and WLD's routing results than in MDD's.

CPU time. The CDD placement time is 14% more than the WLD one since it takes more time to spread block to the whole chip. The MDD placement time is the longest, 24% more than WLD's; the major placement time penalty comes from the computation for the metal density. However, the routing time of MDD is the smallest, 4.67× faster than CDD, and 33.42× faster than WLD. If we consider both placement and routing, MDD used the least runtime since routing time dominates the total runtime.

Routability. A placement with better routability usually has fewer routing overflows, less routing time, and less wirelength increase. All placements obtained by MDD do not have any overflow, while only three (one) placements obtained by CDD (WLD) have no overflow. MDD also has the smallest routing

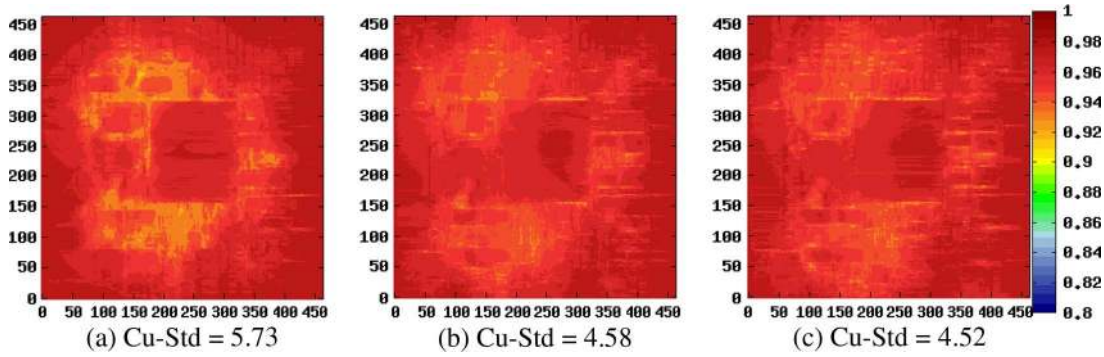

Fig. 11. Normalized Cu thickness map in the horizontal routing layer for adaptec5 using (a) WLD placement, (b) CDD placement, and (c) MDD placement

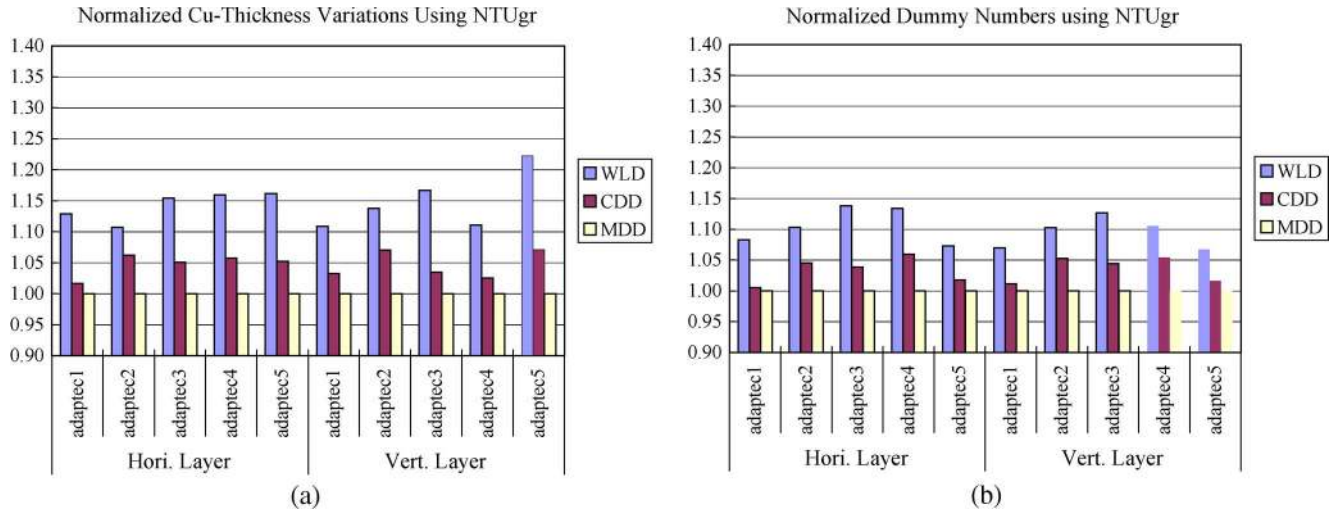

Fig. 12. CMP results using NTUgr. (a) Normalized Cu thickness variations. (b) Normalized dummy numbers.

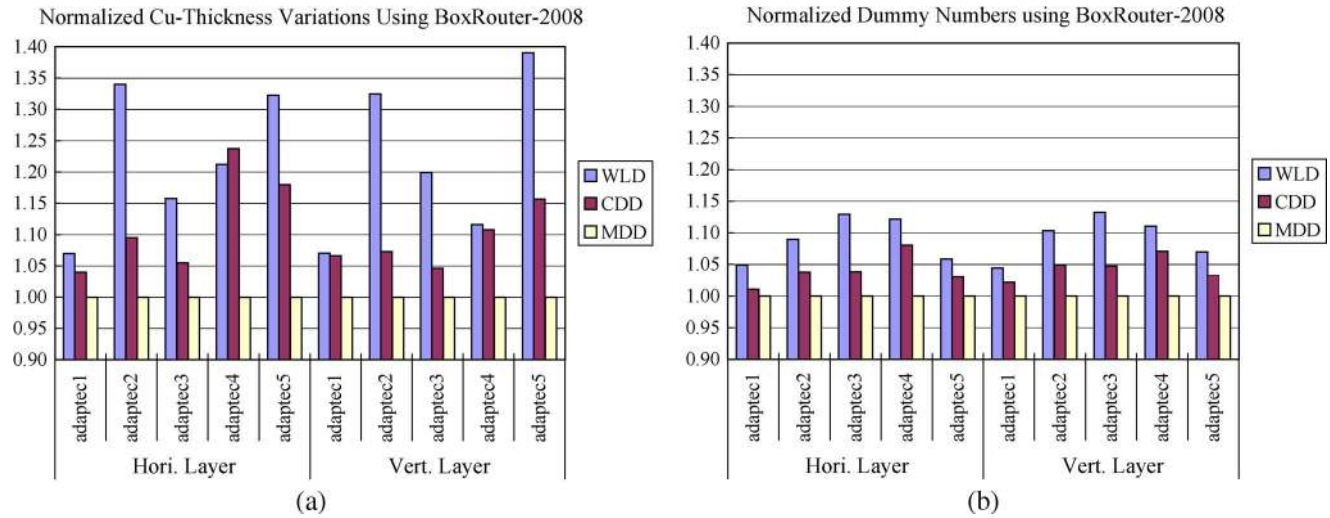

Fig. 13. CMP results using BoxRouter-2008. (a) Normalized Cu thickness variations. (b) Normalized dummy numbers.

time and wirelength increase, implying that MDD's placement results have higher routability. We also found that pure WLD placement usually generates nonroutable results for modern circuit designs. Controlling the cell density can result in better routability, but MDD placement has the best routability among the three modes because there are fewer high wire-density regions in its resulting placement.

The aforementioned results all show that MDD placement leads not only to more uniform metal-density distribution but also better routability. Figs. 10 and 11 show the respective resulting normalized Cu thickness maps in the vertical and horizontal routing layers for adaptec5, using the three placement modes. The standard deviation of the topography variations is shown in the figures.

C. Results Using Other Routers

We also routed our placement results using two state-of-the-art routers, NTUgr [4] and BoxRouter-2008 [4], which were the second and fourth places of the ISPD-2008 Routing Contest. Figs. 12 and 13 show the respective resulting normalized Cu thickness variations and normalized total number of dummy fills for NTUgr and BoxRouter-2008.

For the results of NTUgr, the Cu thickness variation for MDD can be reduced by 15% (5%) on average and the total number of dummy fills can be reduced by 10% (3%) on average, compared with WLD's (CDD's) results. For the results of BoxRouter-2008, the Cu thickness variation for MDD can be reduced by 22% (11%) on average and the total number of dummy fills can be reduced by 9% (4%) on average, compared with WLD's (CDD's) results. The reduction of the thickness variations and the number of dummy fills are consistent for all circuits, no matter which router is used. These results show that our MDD placement for reducing CMP variation is general and is applicable to general routers.

V. Conclusion

Metal density is an important issue for manufacturability of nanometer circuit designs. We have presented the first MDD placement to reduce CMP variation and improve routability. Experimental results have shown that the proposed MDD placement algorithm reduces the copper thickness variation by 12%–22% and dummy fills by 6%–10%, compared with the WLD placement. In addition, the results generated by our MDD placement algorithm lead to higher routability.

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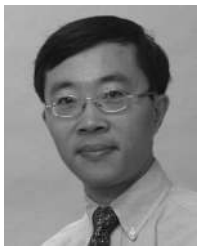

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