

Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology

Yee-Chia Yeo,^{a)} Tsu-Jae King, and Chenming Hu

Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, California 94720

(Received 31 July 2002; accepted 20 September 2002)

The dependence of the metal gate work function on the underlying gate dielectric in advanced metal-oxide-semiconductor (MOS) gate stacks was explored. Metal work functions on high- κ dielectrics are observed to differ appreciably from their values on SiO₂ or in vacuum. We applied the interface dipole theory to the interface between the gate and the gate dielectric of a MOS transistor and obtained excellent agreement with experimental data. Important parameters such as the slope parameters for gate dielectrics like SiO₂, Al₂O₃, Si₃N₄, ZrO₂, and HfO₂ were extracted. In addition, we also explain the weaker dependence of n^+ and p^+ polysilicon gate work functions on the gate dielectric material. Challenges for gate work function engineering are highlighted. This work provides additional guidelines on the choice of gate materials for future MOS technology incorporating high- κ gate dielectrics. © 2002 American Institute of Physics.
[DOI: 10.1063/1.1521517]

I. INTRODUCTION

Aggressive scaling of gate length L_G and gate oxide thickness in complementary metal-oxide-semiconductor (CMOS) transistors for higher performance and circuit density aggravates the problems of polysilicon (poly-Si) gate depletion, high gate resistance, high gate tunneling leakage current, and boron penetration from the p^+ -doped poly-Si gate into the channel region.¹ To reduce the high gate resistance and gate depletion problems, the active dopant density in the poly-Si gate material must be increased. In fact, the active dopant density must be greater than $1.87 \times 10^{20} \text{ cm}^{-3}$ at $L_G = 25 \text{ nm}$ CMOS technology generation for the poly-Si gate depletion layer to be less than 25% of the equivalent SiO₂ thickness $t_{\text{ox,eq}}$.¹ This presents a great difficulty since the active poly-Si dopant density at the gate-dielectric interface saturates at $6 \times 10^{19} \text{ cm}^{-3}$ and $1 \times 10^{20} \text{ cm}^{-3}$ for p^+ - and n^+ -doped poly-Si, respectively.² Insufficient active dopant density in the gate results in a significant voltage drop across the gate depletion layer, and increases the equivalent gate oxide thickness, as illustrated in Fig. 1. In effect, it reduces the gate capacitance in the inversion regime and hence the inversion charge density, or leads to a lower effective gate voltage, thus compromising device performance. As a result, there is immense interest in metal gate technology.³ A metal gate material not only eliminates the gate depletion and boron penetration problems, but also greatly reduces the gate sheet resistance. One approach is to employ a metal with midgap work function for both N- and P-MOS field-effect transistors (FET's).⁴ The drawback is that the threshold voltages $|V_{\text{TH}}|$ would be too large for a reasonable channel doping concentration; counterdoping the channel to reduce V_{TH} degrades transistor short-channel and turn-off characteristics.^{2,4} Hence, an approach analogous to the estab-

lished dual-doped poly-Si gate technology, i.e., a dual-work-function metal gate technology, would be preferred.³

The major challenge is to find two metals with suitable work functions and a way to integrate them into a CMOS process. Metal gates with work functions corresponding to the conduction and valence band edges of Si are desired for the optimal design of bulk-Si N- and P-MOSFET's, respectively.⁵ The energy band alignment between the metal gate and the gate dielectric is very important, because it determines the effective metal gate work function $\Phi_{m,\text{eff}}$, which affects the transistor threshold voltage and optimum current drive.⁵ An accurate understanding of the metal-dielectric interface is essential for the design of transistors with metal gates. However, there has been very little work to study this important interface.^{6,7} In the selection of metal gate materials, a common assumption is that the effective work function of a metal on a gate dielectric is the same as that in vacuum. This has been experimentally observed to be incorrect.⁶ In this paper, the physics of the interface between the gate electrode and the gate dielectric is investigated, and the dependence of the gate work functions on the gate dielectric material is explained. Section II briefly reviews the physics of the metal-semiconductor or metal-dielectric interface. Section III applies the interface dipole theory⁸ to the metal-dielectric interface to explain the experimental observations and extract important material parameters that characterize the gate dielectrics. Fundamental differences between the metal-dielectric and the poly-Si-dielectric interfaces are also noted. Section IV summarizes this work and provides guidelines for the selection of metal gate materials for integration in a CMOS process.

II. THEORETICAL BACKGROUND: INTERFACE DIPOLE THEORY

According to the Schottky model,⁹ when a metal and a semiconductor or a dielectric form an interface, there is no charge transfer across the interface and the barrier height for

^{a)}Electronic mail: yeo@IEEE.org

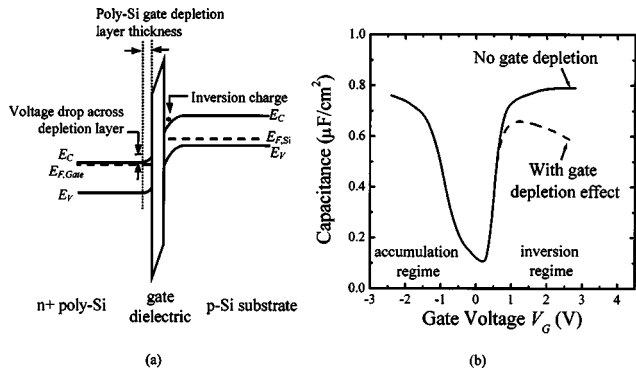


FIG. 1. (a) The energy band diagram of a N-MOS device showing the depletion layer in the poly-Si gate. (b) The poly-Si gate depletion effect decreases the gate capacitance in the inversion regime, as evident in the capacitance-voltage plot.

the electrons is given by the difference between the work function of the metal in vacuum $\Phi_{m,vac}$ and the electron affinity of the semiconductor χ . However, it was observed experimentally that the Schottky model is not generally obeyed. Bardeen then proposed the well-known surface state model to explain this observation.¹⁰ Bardeen's model postulates a high density of surface states of the order of 1 per surface atom at a well-defined energy relative to the conduction band edge of the semiconductor, and these states act to pin the metal Fermi level. However, arguments presented by Heine¹¹ showed that semiconductor surface states do not exist in the fundamental gap for most metal-semiconductor interfaces, except possibly those in Bardeen's time where metal-semiconductor contacts were made by pressing the metal against the semiconductor, each coated with an oxide film. This interfacial oxide film sustains a potential difference to account for the difference between the theoretical Schottky barrier height and experimental observation, and is an essential feature of Bardeen's model. Modern metal-semiconductor interfaces are comprised of materials in intimate atomic contact, and therefore render Bardeen's surface state model inapplicable.

Heine¹¹ was the first to point out that the wave functions of electrons in the metal tail or decay into the semiconductor in the energy range where the conduction band of the metal overlaps the semiconductor band gap. These resulting states in the forbidden gap are known as *metal-induced gap states*¹² or simply *intrinsic states*. The existence of metal-induced gap states at the metal-semiconductor or metal-dielectric interface was also predicted by Louie and Cohen¹² using self-consistent pseudopotential calculations of the electronic structure of material interfaces. Recently, metal-induced gap states were experimentally observed by Muller *et al.* using electron energy loss spectroscopy.¹³ These states are predominantly donorlike close to E_v , and mostly acceptorlike near E_c (Fig. 2). The energy level in the band gap at which the dominant character of the interface states changes from donorlike to acceptorlike is called the charge neutrality level E_{CNL} .⁸ Charge transfer generally occurs across the interface due to the presence of intrinsic interface states. Charging of these interface states creates a dipole that tends to drive the band lineup toward a position that would give zero dipole

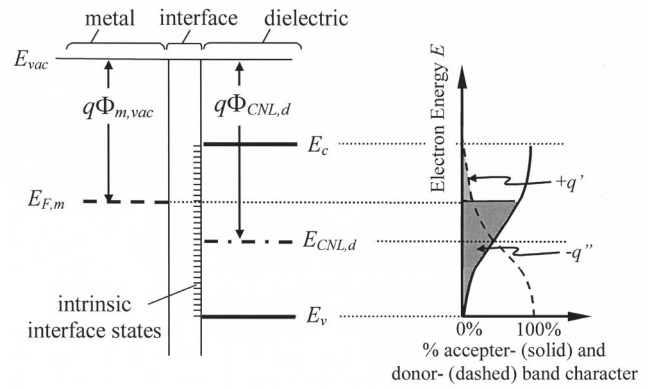


FIG. 2. Energy band diagram (left) and charging character of interface states (right) for the metal-dielectric interface. In general, the character of interface states becomes more acceptor- (donor)like toward the conduction (valence) band, as indicated by the solid (dashed) line. Filling an acceptorlike interface state empty results in a negative charge, while leaving a donorlike interface state empty results in a positive charge. Hence, the shaded area represents the total negative charge on the dielectric side, while the light-gray region represents the total positive charge on the dielectric side.

charge. Figure 2 illustrates the case where the metal Fermi level $E_{F,m}$ is above the charge neutrality level in the dielectric $E_{CNL,d}$, creating a dipole that is charged negatively on the dielectric side. This interface dipole drives the band alignment so that $E_{F,m}$ goes toward $E_{CNL,d}$ and the effective metal work function, $\Phi_{m,eff}$ therefore differs from the vacuum metal work function $\Phi_{m,vac}$. This work function change is proportional to the difference between $E_{CNL,d}$ and $E_{F,m}$, or, equivalently, the difference between $\Phi_{m,vac}$ and $\Phi_{CNL,d}$ [$= (E_{vac} - E_{CNL,d})/q$]. Thus, $\Phi_{m,eff}$ is given by

$$\Phi_{m,eff} = \Phi_{CNL,d} + S(\Phi_{m,vac} - \Phi_{CNL,d}), \quad (1)$$

where S is a slope parameter that accounts for dielectric screening and depends on the electronic component of the dielectric constant ϵ_∞ .^{14,15} With larger dielectric screening, the slope parameter S becomes smaller, as shown in Figs. 3(a) where the slope parameters for a variety of materials are documented. The slope parameter S obeys an empirical relationship given by

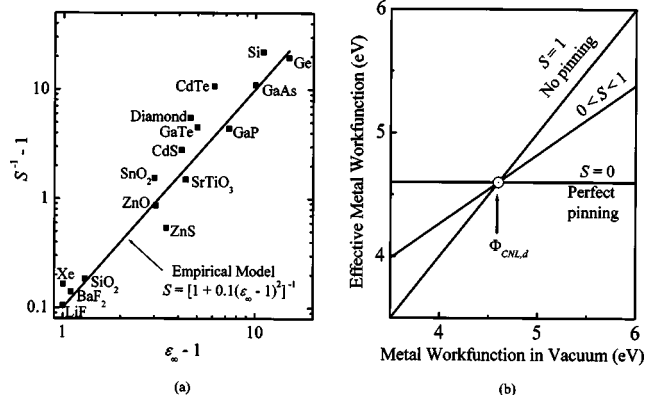


FIG. 3. (a) Variation of the slope parameter S with electronic constant ϵ_∞ . The relationship is empirically modeled by Ref. 15. Materials with large ϵ_∞ have small S . (b) A smaller S leads to a higher degree of pinning of the metal Fermi level $E_{F,m}$ to the charge neutrality level $E_{CNL,d}$ of the dielectric.

TABLE I. Experimental data on metal work functions and conduction band barrier heights at metal-dielectric interfaces.

Metal/dielectric	Work function (eV)	Barrier height (eV)	Measurement method	Reference
Mg	3.66		Photoelectric effect	16
Mg/Al ₂ O ₃	3.6	2.6	Internal photoemission	7
Mg/SiO ₂	3.45	2.5	Internal photoemission	7
Mg/ZrO ₂	4.15	2.6	Internal photoemission	7
Ta (polycrystalline)	4.25		Thermionic emission	17
Ta/SiO ₂	4.2		MOS capacitor V_{FB}	18
Al	4.28			19
Al/Al ₂ O ₃	3.9	2.9	Internal photoemission	7
Al/SiO ₂	4.14		MOS capacitor V_{FB}	6
Al/Si ₃ N ₄	4.06		MOS capacitor V_{FB}	6
Al/ZrO ₂	4.25	2.7	Internal photoemission	7
W	4.63		Field emission	20
W/SiO ₂	4.6–4.7	3.65–3.75	Fowler-Nordheim tunneling	21
Mo(110)	4.95		Photoelectric effect	22
Mo/SiO ₂	5.05		MOS capacitor V_{FB}	23
Mo/Si ₃ N ₄	4.76		MOS capacitor V_{FB}	3
Mo/HfO ₂	4.95		MOS capacitor V_{FB}	24
Pt	5.65		Photoelectric effect	25
Pt/SiO ₂	5.59		MOS capacitor V_{FB}	6
Pt/HfO ₂	5.23		MOS capacitor V_{FB}	26
Pt/ZrO ₂	5.05		MOS capacitor V_{FB}	27
Ni(110)	5.04		Photoelectric effect	16
Ni/Al ₂ O ₃	4.5	3.5	Internal photoemission	7
Ni/ZrO ₂	4.75	3.25	Internal photoemission	7
Au	5.31–5.47		Photoelectric effect	16
Au/Al ₂ O ₃	5.1	4.1	Internal photoemission	7
Au/ZrO ₂	5.05	3.5	Internal photoemission	7
Hf(polycrystalline)	3.95		Photoelectric effect	16
Hf/SiO ₂	4.0		MOS capacitor V_{FB}	28

$$S = \frac{1}{1 + 0.1(\epsilon_{\infty} - 1)^2}. \quad (2)$$

Materials with a smaller S tend to pin the metal Fermi level more effectively to $E_{CNL,d}$, as illustrated in Fig. 3(b). The maximum value for S is unity, which corresponds to no pinning of the metal Fermi level.

III. EXPERIMENTAL DATA AND EXTRACTION OF MATERIAL PARAMETERS

Table I summarizes the experimental work function data for metals in vacuum and metals on dielectrics such as SiO₂, Al₂O₃, ZrO₂, HfO₂, and Si₃N₄. The work function of a metal is a measure of the minimum energy required to extract an electron from the surface of the metal. It is commonly measured in vacuum by making use of phenomena such as the photoelectric effect or thermionic emission. In general, it differs for each facet of a monocrystalline sample.^{16,19,22} Partial crystalline orientation of film specimens can account for observed differences in some cases, since anisotropies of up to ~0.5 eV exist for the different crystal facets. Given that the work function measurement is also dependent on the cleanliness of the metal surface, data reported in the literature often cover a considerable range, and Table I documents the

typical values for a reasonably clean surface. For the measurement of a metal work function in a metal-dielectric system, the most common method is an extraction of the flat-band voltage from the capacitance-voltage characteristics of a metal-dielectric-semiconductor capacitor.^{23,29} Internal photoemission may also be used to extract the barrier height at the interface of a metal-dielectric system,⁷ and the metal work function may be deduced from the barrier height and the electron affinity of the dielectric. The electron affinities of SiO₂, Al₂O₃, and ZrO₂, are 0.95, 1.0, and 2.5 eV, respectively.³⁰

The experimental data (symbols) are plotted in Fig. 4 to illustrate the varying degrees of pinning of metal work functions toward $E_{CNL,d}$ of gate dielectrics such as SiO₂, Al₂O₃, ZrO₂, HfO₂, and Si₃N₄. A fit of Eq. (1) to the experimental data not only reveals the good agreement between the interface dipole theory and measured data, but also yields the first extraction of $E_{CNL,d}$ and S for dielectrics like ZrO₂, HfO₂, and Si₃N₄. The extracted $(E_{CNL,d} - E_v)$ values obtained in this work are compared with theoretical values³⁰ in Table II, showing reasonable agreement. It should be noted that theoretical values of $E_{CNL,d}$ are derived from electronic band structures.³¹ In achieving self-consistency in electronic band structure calculations, the local density approximation,³²

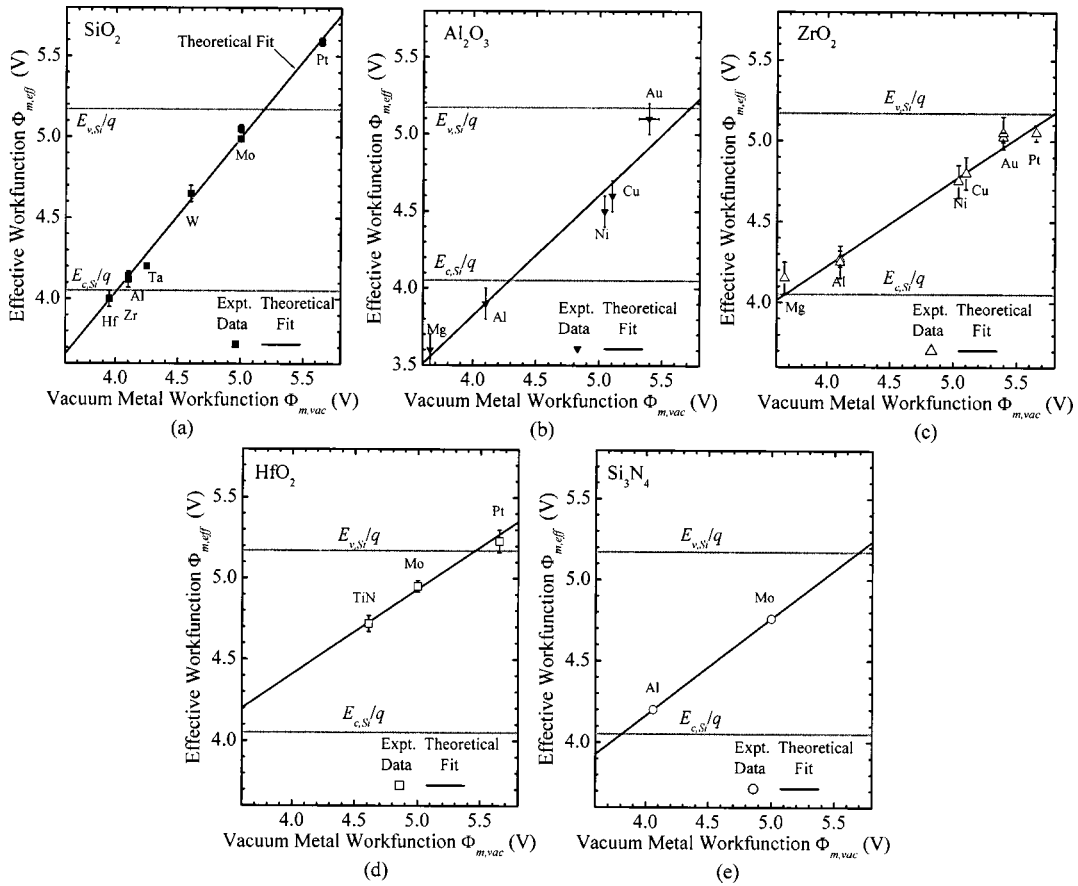


FIG. 4. Effective work functions of metals on various dielectrics such as (a) SiO₂, (b) Al₂O₃, (c) ZrO₂, (d) HfO₂, and (e) Si₃N₄ versus their work functions in vacuum. Good agreement is observed between experimental data (symbols) and the theoretical fit (lines) based on the interface dipole theory.

which results in an underestimation of the band-gap energy, is often employed. Thus, theoretically derived values of $E_{CNL,d}$ with reference to the conduction or valence bands should be used with caution. For this reason, our experimental extraction of $(E_{CNL,d} - E_v)$ should be more accurate and useful.

Since metal gates with work functions near the conduction and valence band edges of Si are ideal for the optimum performance of bulk N- and P-MOSFET's, respectively,⁵ the desired effective metal work function should be ~4.05 V for

the N-MOSFET and ~5.17 V for the P-MOSFET. Consider ZrO₂ for example. Figure 4(c) suggests that in order to obtain $\Phi_{m,eff}$ of 4.05 V (or 5.17 V) for a N-MOS (or P-MOS) device, a metal with an even smaller (or larger) $\Phi_{m,vac}$ has to be used. In fact, the selection of metal gate materials to achieve the desired effective work functions depends on the choice of the gate dielectric materials. As a result, research work on metal gate technology should be performed in close conjunction with work on alternative gate dielectrics.³ This dependency is examined in Fig. 5 where the required $\Phi_{m,vac}$

TABLE II. Comparison of theoretical and experimental slope parameters and charge neutrality levels for several gate dielectrics.

	E_G (eV)	ϵ_∞	Theory	Empirical model	Experimental (this work)	
			$E_{CNL} - E_v$ (eV)	S	$E_{CNL} - E_v$ (eV)	S
Si	1.12		0.36 ^a			
Ge	0.66		0.18 ^a			
SiO ₂	9	2.25	4.5	0.86 ^d	5.04	0.95
Al ₂ O ₃	8.8	3.4	5.5 ^b	0.63 ^d	6.62	0.69
Si ₃ N ₄	5.3	3.8	2.6 ^c	0.56 ^d	2.79	0.59
HfO ₂	6.0	4	3.7 ^b	0.53 ^d	3.64	0.52
ZrO ₂	5.8	4.8	3.6 ^b	0.41 ^d	3.82	0.52

^aTaken from Ref. 8.

^bTaken from Ref. 30; electron band structures obtained using tight-binding method.

^cCalculated from band structures obtained using the self-consistent orthogonalized linear combination of atomic orbitals method (Ref. 32).

^dDetermined from empirical model: $S = [1 + 0.1(\epsilon_\infty - 1)^2]^{-1}$.

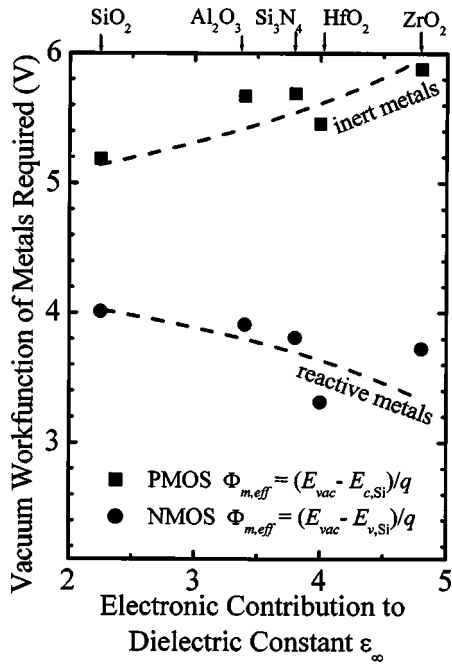


FIG. 5. Selection of metals to obtain effective work functions of 4.05 and 5.17 V for five different gate dielectrics. The data points are calculated from our experimentally extracted $\Phi_{CNL,d}$ and S . The trend lines are shown in dashes.

to achieve $\Phi_{m,eff}=4.05$ V for a N-MOS (solid circles) and $\Phi_{m,eff}=5.17$ V for a P-MOS (solid squares) device is plotted as a function of ϵ_{∞} for five different dielectrics. The data points in Fig. 5 are obtained using the extracted values of $E_{CNL,d}$ and S (Table II). For a high- κ gate dielectric, a high-work-function inert metal must be used as the P-MOS gate electrode. High-work-function metals such as platinum are resistant to chemical or plasma etching, so gate patterning would be particularly challenging. On the other hand, a low-work-function metal must be used as the N-MOS gate electrode. Low-work-function metals such as magnesium and hafnium are extremely reactive, and this might introduce extrinsic interface states due to defects arising from an interfacial reaction. Defect-related extrinsic interface states should be distinguished from intrinsic interface states. Any large deviation of the measured effective work functions from the linear trend in Fig. 4 may be attributed to the existence of extrinsic interface states. We have carefully eliminated data that show evidence of an interfacial reaction. To avoid the need for either an inert or reactive metal gate, a possible solution is to introduce at least a monolayer of SiO_2 at the metal-dielectric interface to achieve a large S . Nevertheless, this approach leads to a lower effective dielectric permittivity for the gate dielectric stack and compromises gate leakage current and power consumption.

It is worthwhile to compare the metal gate technology with the well-established dual-doped poly-Si technology on the issue of electrode work function dependence on the choice of gate dielectric materials. It has recently been shown that poly-Si on HfO_2 and SiO_2 has about the same work function.³³ The important characteristic that differentiates the poly-Si-dielectric interface from the metal-dielectric

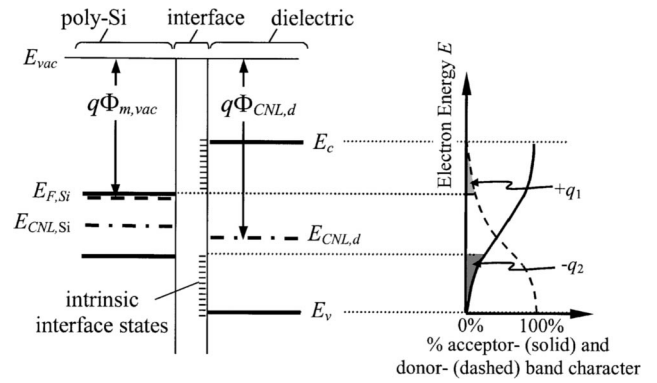


FIG. 6. Energy band diagram (left) and charging character of interface states (right) for silicon-dielectric interfaces. The shaded area represents the total negative charge on the dielectric side, while the gray region represents the total positive charge on the dielectric side.

interface is the absence of interface states at energies where the band gaps of both materials overlap (Fig. 6). The band lineup at the poly-Si-dielectric interface is thus driven by a smaller dipole charge. Mathematically, the effective work function of n^+ or p^+ poly-Si, $\Phi_{Si,eff}$, is determined by the alignment of $E_{CNL,Si}$ and $E_{CNL,d}$,

$$\Phi_{Si,eff} = \Phi_{Si} + (S - 1)(\Phi_{CNL,Si} - \Phi_{CNL,d}). \quad (3)$$

In Eq. (3), Φ_{Si} is the work function of n^+ or p^+ poly-Si in vacuum, and $\Phi_{CNL,Si}$ is the charge neutrality level in Si. Using Eqs. (1) and (3), the theoretical effective work functions of n^+ poly-Si ($\Phi_{Si}=4.05$ V) and a metal with $\Phi_{m,vac}=4.05$ V on different high- κ dielectrics are compared in Fig. 7. It shows that the n^+ poly-Si gate is less vulnerable to Fermi pinning compared to the metal gate with $\Phi_{m,vac}=4.05$ V. This is also true for p^+ poly-Si ($\Phi_{Si}=5.17$ V) and a metal with $\Phi_{m,vac}=5.17$ V.

IV. CONCLUSION

The metal-dielectric interface in advanced MOS gate stacks was examined. Metal work functions on high- κ di-

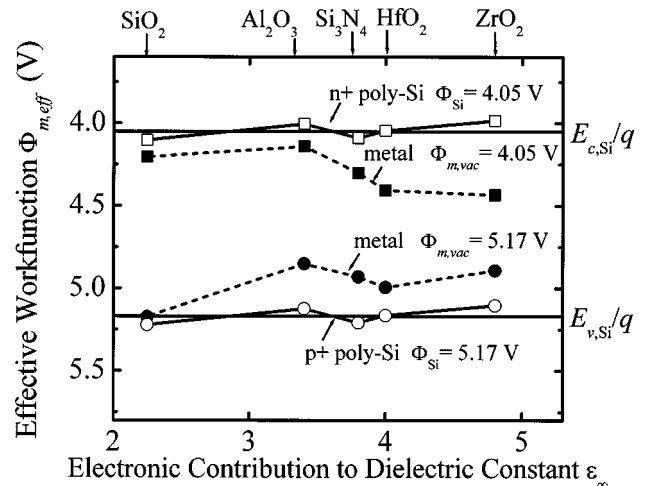


FIG. 7. Metal Fermi levels tend to be pinned to E_{CNL} of the dielectric. This tendency increases with ϵ_{∞} . Poly-Si or poly-SiGe gates do not suffer appreciably from this effect.

electrics were observed to differ appreciably from their values on SiO₂ or in vacuum. This dependence of metal gate work functions on the underlying gate dielectric was explained using the interface dipole theory. Excellent agreement with experimental data was obtained. Important parameters such as the slope parameters for SiO₂, Al₂O₃, Si₃N₄, ZrO₂, and HfO₂ were extracted. To achieve the desired dual-metal gate work functions on high- κ gate dielectrics for optimum device performance, candidate metals need to have vacuum work functions smaller (or larger) than 4.05 V (or 5.17 V) for the N-MOS (or P-MOS) transistors. A monolayer of SiO₂ at the interface could relax this requirement. Additional guidelines were provided for the choice of gate materials for future CMOS technology incorporating high- κ gate dielectrics. The effective work functions of n^+ and p^+ poly-Si gates show less dependence on the gate dielectric material. This weaker dependence on the gate dielectric material was explained.

ACKNOWLEDGMENTS

Y.-C.Y. acknowledges financial support from a NUS OGS Award, Singapore, and an IEEE Electron Device Society Graduate Student Fellowship Award.

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