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Metal oxide semiconductor thin-film transistors for flexible electronics

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The field of flexible electronics has rapidly expanded over the last decades, pioneering novel applications, such as wearable and textile integrated devices, seamless and embedded patch-like systems, soft electronic skins, as well as imperceptible and transient implants. The possibility to revolutionize our daily life with such disruptive appliances has fueled the quest for electronic devices which yield good electrical and mechanical performance and are at the same time light-weight, transparent, conformable, stretchable, and even biodegradable. Flexible metal oxide semiconductor thin-film transistors (TFTs) can fulfill all these requirements and are therefore considered the most promising technology for tomorrow's electronics. This review reflects the establishment of flexible metal oxide semiconductor TFTs, from the development of single devices, large-area circuits, up to entirely integrated systems. First, an introduction on metal oxide semiconductor TFTs is given, where the history of the field is revisited, the TFT configurations and operating principles are presented, and the main issues and technological challenges faced in the area are analyzed. Then, the recent advances achieved for flexible n-type metal oxide semiconductor TFTs manufactured by physical vapor deposition methods and solution-processing techniques are summarized. In particular, the ability of flexible metal oxide semiconductor TFTs to combine low temperature fabrication, high carrier mobility, large frequency operation, extreme mechanical bendability, together with transparency, conformability, stretchability, and water dissolubility is shown. Afterward, a detailed analysis of the most promising metal oxide semiconducting materials developed to realize the state-of-the-art flexible p-type TFTs is given. Next, the recent progresses obtained for flexible metal oxide semiconductor-based electronic circuits, realized with both unipolar and complementary technology, are reported. In particular, the realization of large-area digital circuitry like flexible near field communication tags and analog integrated circuits such as bendable operational amplifiers is presented. The last topic of this review is devoted for emerging flexible electronic systems, from foldable displays, power transmission elements to integrated systems for large-area sensing and data storage and transmission. Finally, the conclusions are drawn and an outlook over the field with a prediction for the future is provided. *Published by AIP Publishing.*
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TABLE OF CONTENTS

I. INTRODUCTION

Electronics today is facing a disruptive evolution, advancing from heavy, bulky, and rigid devices to light-weight, soft, and flexible appliances. Emerging new applications like smart labels[1] and intelligent packaging,[2] wearable[1–4] and textile integrated systems,[5–7] seamless and embedded patch-like electronics,[8,9] epidermal devices,[10–16] artificial skins for robots,[17–19] imperceptible[20–22] biomimetic[23] and transient[24–26] medical implants, as well as advanced surgical tools[13,15,27,28] promise to revolutionize our daily life. To enable all these applications, electronic devices have to become flexible, light-weight, transparent, conformable, stretchable, and even biocompatible and biodegradable. Flexible thin-film transistors (TFTs) are able to fulfill all these requirements and are thus becoming increasingly important to realize next-generation electronic device platforms. Among the state-of-the-art flexible TFT technologies, metal oxide semiconductors are especially suitable, owing to their high optical transparency,[29] good electrical performance [electron carrier mobility of $\geq 10\,cm^2\ V^{-1}\ s^{-1}$ even if processed at room temperature (RT)],[29] as well as excellent mechanical properties (large bendability down to 25 μm radii and good insensitivity to strain).[23,30] Table I provides a summary and a comparison of the most important device properties for the established flexible TFT technologies: amorphous silicon (a-Si),[31,32] organic semiconductors,[14,33] low temperature poly-crystalline silicon (LTPS),[34,35] and metal oxide semiconductors. As evident from Table I, metal oxide semiconducting technology presents several advantages typical of a-Si and organic materials, such as low cost, low process complexity and temperature, and large-area scalability, but at the same time yields a larger carrier mobility.[36] Compared with LTPS, metal oxide semiconductors present slightly lower carrier mobility, but also larger scalability, smaller manufacturing cost, as well as process complexity and temperature.[36] Furthermore, metal oxide semiconductor TFTs show a larger resistance to mechanical strain if compared with LTPS devices.[30] This is why metal oxide semiconductors are considered the most prominent candidate for next-generation flexible high-resolution active matrix organic light emitting diode (AMOLED) display backplanes,[38–41] as well as the most suitable technology to fuel the realization of tomorrow's ubiquitous electronics. Main aim of this review is to report the recent advances obtained in the field of flexible metal oxide semiconductor TFTs: from single devices (Sections II and III), large-area circuits (Section IV) up to entirely integrated systems (Section V). Before reviewing the state-of-the-art of flexible metal oxide semiconductor technology in the Sections II–V, in this section an introduction on the topic is given. First, in Sec. I A, a historical overview on TFTs based on metal oxide semiconductors is presented. Subsequently, in Sec. I B, the operating principle of TFTs together with the available device configurations are reported. Finally, in Sec. I C, the main issues and technological challenges faced in the field are analyzed.

A. Historical perspective

TFTs find their origin back in the 1930 when the field-effect transistor (FET) was proposed and patented by Lilienfeld.[42–44] In these reports, Lilienfeld described the concept of a device in which the current flow is controlled by the application of a transversal electric field. Even if TFTs and FETs share the same operating principle, the first TFT was realized only in 1962 by Weimer at RCA laboratory.[45] In his work, Weimer used a vacuum technique (evaporation) and high-precision shadow masking to deposit and structure a gold (Au) source/drain (S/D) electrodes, a micro-crystalline cadmium sulfide (CdS) n-type (electron conducting) semiconductor, a silicon monoxide gate dielectric, and an Au gate contact on an insulating glass substrate (Fig. 1). Interestingly, Weimer already showed a preliminary evaluation of thin-film circuits, such as flip-flops, AND, and NOR gates. His proceeding of IRE "The TFT - a new Thin-Film Transistor" draws worldwide attention,[45] opening the way to a new field of study. Few years later in 1964, the first TFT with a metal oxide semiconductor was demonstrated by Klasens and Koelmans.[46] The device was manufactured by photolithographic techniques and comprised aluminum (Al) electrodes, anodized aluminum oxide (Al_2O_3) gate dielectric, evaporated n-type tin oxide (SnO_2) semiconductor, and source/drain contacts on a glass substrate. For the first time, the transparency of substrate, semiconductor, and gate dielectric allowed realizing a self-aligned (SA) lithographic lift-off process, where the source/drain contacts were defined by exposing the photoresist to ultraviolet (UV) light penetrating from the back of the substrate. In this way, the opaque Al gate electrode could act as a shielding layer for the UV light.[46] Subsequently, TFTs with single crystal lithium-doped zinc oxide (ZnO:Li) hydrotermically grown from solution,[47] as well as SnO_2 deposited from vapor phase reaction, were presented.[48] Nevertheless, none of these two devices outperformed the results shown by Klasens and Koelmans. After a few decades of silence, in 1996 metal oxide semiconductors gained new attention as active layers in ferroelectric memory TFTs.[49,50] The pioneering work of

TABLE I. Comparison between metal oxide semiconductors and other established flexible TFT technologies.[8,35–37]

	Microstructure	Carrier mobility ($cm^2\ V^{-1}\ s^{-1}$)	Manufacturing cost	Process complexity	Process temperature (°C)	Large-area scalability	Device type
Metal oxide semiconductors	Mainly amorphous	10–100	Low	Low	RT to 350	High	Mainly n-type
Amorphous silicon	Amorphous	1	Low	Low	150–300	High	N-type
Low temperature poly-crystalline silicon	Poly-crystalline	50–100	High	High	350–500	Low	N- and p-type
Organic semiconductors	Mainly poly-crystalline	0.1–10	Low	Low	RT to 250	High	Mainly p-type

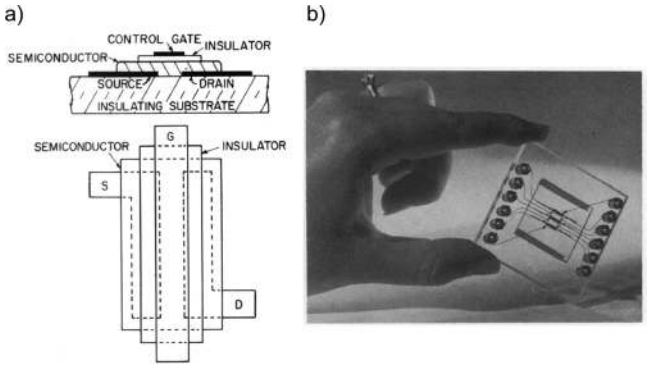

FIG. 1. (a) Device cross-section, top view and (b) photograph of the first thin-film transistor (TFT) reported in 1962. Reproduced with permission from P. Weimer, Proc. IRE **50**, 1942 (1962). Copyright 1962 Institute of Electrical and Electronic Engineers.

Prins *et al*. demonstrated the first fully transparent and metal oxide-based TFT with antimony-doped SnO_2 (SnO_2:Sb) semiconductor grown by pulsed layer deposition (PLD) (Fig. 2).[49] At the same time, Seager *et al*. showed the first indium oxide (In_2O_3) non-volatile memory TFT with ferroelectric gate dielectric.[50] Following the success of these works, from 2003 metal oxide semiconductors gained an increasingly interest. The majority of the attention was initially directed to zinc oxide (ZnO) TFTs,[51–59] resulting in an electron mobility above $1\,cm^2\,V^{-1}\,s^{-1}$.[51,52,54,55,57–59] Such values highlighted the suitability of this technology as a replacement for a-Si, commonly employed in TFT display backplanes. In this context, Hoffman, Norris, and Wager reported fully transparent ZnO TFTs yielding a carrier mobility of $2.5\,cm^2\,V^{-1}\,s^{-1}$ and current on/off ratio of 10^7.[51] In this case, the ZnO layer was deposited by ion-beam sputtering (IBS) and annealed between 600 and 800 °C. A few months later, Carcia *et al*. presented TFTs with ZnO radio-frequency (RF) sputtered at room temperature exhibiting similarly good performance.[52] At the same time, also Norris *et al*. showed the first TFT with spin coated ZnO active layer, yielding a satisfactory carrier mobility of $0.2\,cm^2\,V^{-1}\,s^{-1}$.[60] Subsequently, Fortunato *et al*. reported fully transparent TFTs with ZnO RF sputtered at room temperature presenting an electron mobility of $20\,cm^2\,V^{-1}\,s^{-1}$,[58] whereas Carcia, McLean, and Reilly demonstrated how semiconductor engineering during ZnO sputtering can lead to TFTs with a carrier mobility as high as $42\,cm^2\,V^{-1}\,s^{-1}$.[59] Additionally, also TFTs with other binary metal oxide semiconductors like In_2O_3 and SnO_2 were reported, yielding also good performance.[61,62] Main breakthrough in the field was achieved in 2003 by Nomura *et al*. who demonstrated a multicomponent indium gallium zinc oxide (IGZO) single-crystalline active layer epitaxially grown at 1400 °C on an yttria-stabilized zirconium (YSZ) substrate.[63] The resulting TFT presented an electron mobility of $80\,cm^2\,V^{-1}\,s^{-1}$ and a current on/off ratio of 10^6, demonstrating that high-performance TFTs can be realized with metal oxide semiconductors. Continuing their work, in 2004 Nomura *et al*. reported transparent TFTs with amorphous IGZO layers grown at room temperature by PLD on flexible polyethylene terephthalate (PET) foils (Fig. 3).[29] The results were impressive (especially considering the low temperature process): an electron mobility

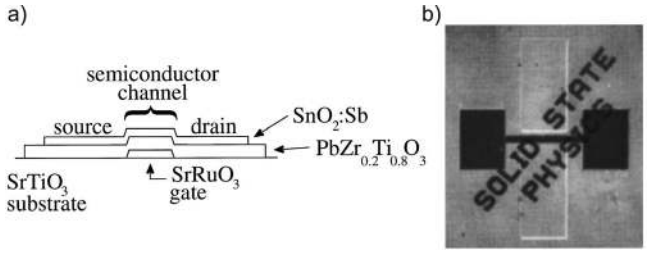

FIG. 2. (a) Device cross-section and (b) photograph of the first fully transparent metal oxide-based TFT reported in 1996. Reproduced with permission from Appl. Phys. Lett. **68**, 3650 (1996). Copyright 1996 AIP Publishing LLC.

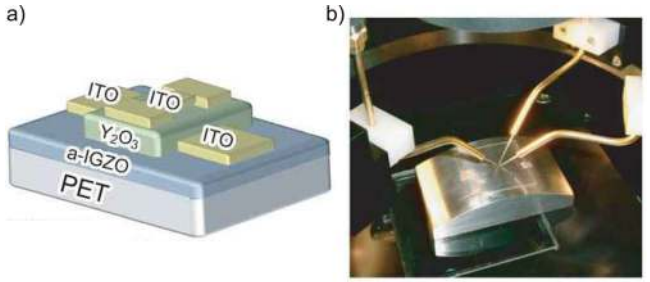

FIG. 3. First flexible TFT with indium gallium zinc oxide (IGZO) active layer reported in 2004: (a) cross-section and (b) photograph of TFT bent to 30 mm tensile radius. Reproduced with permission from Nomura *et al*., Nature **432**, 488 (2004). Copyright 2004 Nature Publishing Group.

of $9\,cm^2\,V^{-1}\,s^{-1}$ and a current on/off ratio of 10^3. Furthermore, first mechanical bending tests of the devices at 30 mm radius were demonstrated. Nomura's report paved the way to an impressive number of publications on metal oxide semiconductor TFTs. In the following years, several multicomponent metal oxide semiconductors, ranging from zinc tin oxide (ZTO),[64,65] indium zinc oxide (IZO)[66] to IGZO (the most common),[67–69] were investigated. From 2005, also the first reports on hole transporting (p-type) metal oxide semiconductors appeared. First, Chang *et al*. demonstrated p-type behavior in gallium oxide (Ga_2O_3) nanowire (NW) TFTs,[70] followed by other works on p-type tin monoxide (SnO),[71,72] cuprous oxide (Cu_2O),[73,74] and nickel oxide (NiO)[75] devices all presenting low carrier mobility and high process temperatures. Remarkably, in 2007 Ju *et al*. showed the first flexible and solution-processed metal oxide semiconductor TFTs based on ZnO and In_2O_3 NWs.[76] From 2008, tremendous advances were made in the field of flexible devices, from IGZO TFTs on cellulose fiber-based paper,[77] stretchable and transparent ZnO TFTs,[78] complementary inverters based on n-type IGZO and p-type SnO TFTs with and on paper,[79] ultraflexible and transparent IGZO TFTs,[80] three-dimensionally (3D) conformable IGZO TFTs and circuits,[81] water soluble IGZO TFTs,[82] to mechanically active biomimetic IGZO TFTs.[23] Nowadays, the state-of-the-art flexible IGZO TFTs yield excellent electrical performance with carrier mobility values up to $84\,cm^2\,V^{-1}\,s^{-1}$ (Ref. 83) and current on/off ratio above 10^{10},[84] depending on the semiconductor composition and device configuration.

B. TFT configuration and operation

In this subsection, the most common TFT configurations are presented, followed by a short explanation of the basic TFT operating principle.

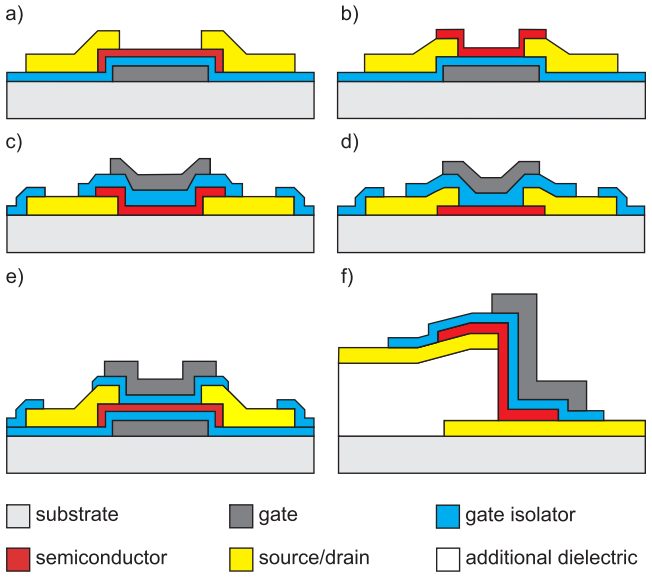

FIG. 4. Most common device configurations: (a) bottom-gate (BG) staggered TFT, (b) BG coplanar TFT, (c) top-gate (TG) staggered TFT, (d) TG coplanar TFT, (e) double-gate (DG) TFT, and (f) vertical TFT (VTFT).

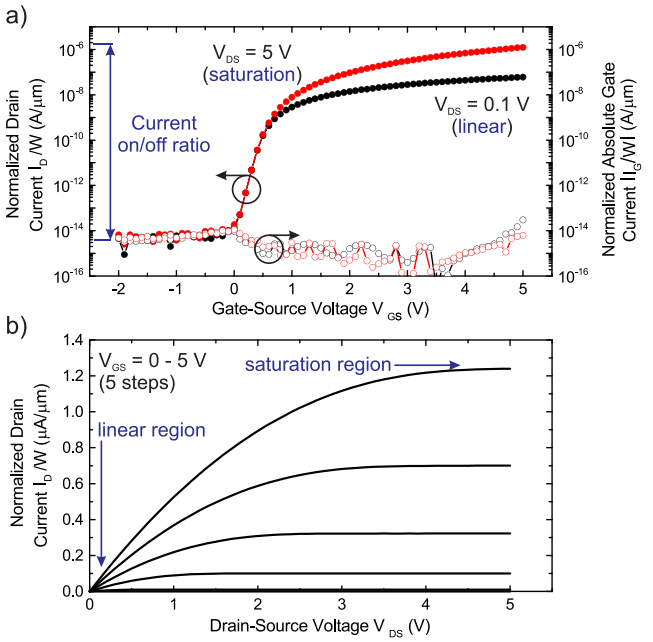

FIG. 5. Typical current-voltage characteristics of an n-type metal oxide semiconductor TFT (channel length L = 30 μm): width (W) normalized transfer (a) and output (b) curves.

1. TFT configuration

TFTs are three terminal field-effect devices, whose working principle is similar to those of metal oxide semiconductor field-effect transistors (MOSFETs) used in conventional Silicon (Si) electronics.[85] However, in MOSFET technology, the substrate is a single crystal Si wafer (representing also the active layer) and device functionality is added through a large variety of complex, high temperature (>1000 °C) and expensive processes (e.g., diffusion/implantation of dopants, lithography, and etching).[86] On the other hand, TFTs are fabricated typically on insulating substrates (glass and plastic), on which all the device layers are grown at lower temperature (<650 °C) by vacuum- or solution-processing deposition techniques. Given the different manufacturing processes, the active layers of TFTs are typically poly-crystalline or amorphous materials, which are both characterized by a reduced charge carrier transport (if compared with single-crystal Si).[36,87] Like in MOSFETs, TFT functionality is achieved through the following components: a dielectric layer inserted between the semiconductor and a transversal gate contact, together with two source/drain electrodes directly in contact with the semiconductor. Current modulation between source/drain is achieved through the semiconducting layer by the capacitive injection of carriers close to the dielectric/semiconductor interface (the so-called field-effect).[85] Even if both MOSFETs and TFTs rely on the field-effect to modulate the conductance of the active layer, in TFTs this is achieved by an accumulation layer (and not an inversion region like in MOSFETs). TFTs can be fabricated using a wide range of device configurations. Most peculiar planar TFT structures are: bottom-gate (BG) (Figs. 4(a) and 4(b)) and top-gate (TG) (Figs. 4(c) and 4(d)) architectures, depending on whether the gate electrode is deposited before or after the active layer. BG and TG devices can be either staggered or coplanar, depending if the source/drain contacts are on the opposite or on the same side of the semiconductor/dielectric interface.[85] BG structures, especially staggered (Fig. 4(a)), have been widely used for a-Si TFTs, as well as in most display prototypes due to easier processing and enhanced performance.[36,88] Nevertheless, BG structures require an additional layer (passivation) that protects the back channel from air exposure and therefore hinders undesired instability effects.[36,88] TG structures, especially coplanar (Fig. 4(d)), are mainly used for LTPS technology. With such a configuration indeed, the semiconductor can be deposited and crystallized at high temperatures without any damage to other materials/interfaces that are realized in successive steps.[34] In TG TFTs, the gate dielectric can also act as a passivation layer, reducing thus the number of patterning steps.[29,88] To improve the static (DC) performance, double-gate (DG) TFT structures (Fig. 4(e)) can be employed.[89,90] In DG TFTs, an additional gate is utilized to effectively control a larger portion of the semiconductor channel. Recently, the quest for small device footprint and nanoscaled channel lengths has led to the development of alternatives to planar geometries, such as vertical TFTs (VTFTs) (Fig. 4(f)) or quasi-vertical TFTs (QVTFTs), where the channel is not anymore defined by a photolithographic patterning step, but rather by the thickness of a device layer.[91,92] In the most common VTFT structures, the channel is formed on a multi-layer stack of source-dielectric-drain (Fig. 4(e)).[91–93] Nevertheless, alternative VTFT configurations with the channel defined by the gate or the semiconductor thickness have also been proposed and realized.[94–96]

2. TFT operation

The most important DC performance parameters are extracted from the current-voltage (I-V) characteristics in compliance with the gradual channel approximation.[97] As shown in the transfer I_D-V_{GS} (Fig. 5(a)) and output I_D-V_{DS} (Fig. 5(b)) curves, there are two main operating regimes: linear and saturation. For small values of the drain-source

voltage V_{DS} ($V_{DS} \ll V_{GS} - V_{TH}$, where V_{GS} is the gate-source voltage and V_{TH} is the threshold voltage), the device operates in linear regime and the drain current I_D is approximated by the simplified Shichman - Hodges FET model[98]

$$I_{D,lin} = \frac{W \cdot \mu \cdot C_{ox}}{L} \cdot (V_{GS} - V_{TH}) \cdot V_{DS}, \tag{1.1}$$

where W is the channel width, μ is the channel mobility, C_{ox} is the specific capacitance of the gate dielectric per unit area, and L is the channel length. When $V_{DS} \geq V_{GS} - V_{TH}$, the device operates in saturation regime and I_D equals

$$I_{D,sat} = \frac{W \cdot \mu \cdot C_{ox}}{2 \cdot L} \cdot (V_{GS} - V_{TH})^2. \tag{1.2}$$

Equations (1.1) and (1.2) can be used to extract the TFT DC parameters: carrier mobility, threshold voltage, current on/off ratio, sub-threshold swing (SS), and contact resistance.[97]

a. Carrier mobility. This parameter describes the efficiency of charge carrier transport in a material, which affects directly the maximum drain current and the operating frequency (the so-called transit frequency f_T) of a device.[99] In a material, μ depends on several scattering mechanisms (e.g., lattice vibrations, impurities, and grain boundaries).[99,100] The most common way to characterize the intrinsic mobility of a bulk material is to extract the Hall mobility (μ_H) from the Hall effect.[100] The mobility in a TFT is typically different from the intrinsic mobility of its semiconductor, since charge transfer is now limited to a narrow region close to the gate dielectric/semiconductor interface and further sources of scattering (e.g., Coulomb scattering from dielectric charges and interface states, and surface roughness scattering) need to be considered.[100] According to Schroder,[100] several TFT mobilities can be extracted: the effective mobility μ_{eff}, the field-effect mobility μ_{FE}, and the saturation mobility μ_{sat}. Most common mobilities are μ_{FE} (also known as linear mobility μ_{lin})

$$\mu_{FE} = \mu_{lin} = \frac{L}{W \cdot C_{ox} \cdot V_{DS}} \cdot \frac{dI_D}{dV_{GS}}, \tag{1.3}$$

and

$$\mu_{sat} = \frac{2 \cdot L}{W \cdot C_{ox}} \cdot \frac{d^2 I_D}{dV_{GS}^2} = \frac{2 \cdot L}{W \cdot C_{ox}} \cdot \left(\frac{d\sqrt{I_D}}{dV_{GS}}\right)^2. \tag{1.4}$$

b. Threshold voltage. The threshold voltage V_{TH} corresponds to the gate-source voltage at which a conductive channel is formed at the dielectric/semiconductor interface.[97] In n-type TFTs, if V_{TH} is positive/negative, the devices are designated to operate in enhancement/depletion mode.[51] There are several methods used to extract V_{TH}.[101] If not explicitly specified, the most employed methodology is represented by the linear extrapolation of the I_D-V_{GS} plot (linear regime) or $I_D^{1/2}$-V_{GS} plot (saturation regime).[101]

c. Current on/off ratio. The current on/off ratio I_{ON}/I_{OFF} is extracted from the transfer curve (Fig. 5(a)), dividing the maximum with the minimum drain current (typically in saturation regime).[97] A value of 10^6 or higher is desirable for digital circuits.[102] Nevertheless, smaller I_{ON}/I_{OFF} can also result in successful switching operation.[103] For analog circuits, a current on/off ratio of $>10^4$ is typically sufficient.[80]

d. Sub-threshold swing. Another important parameter is the sub-threshold swing (SS), which is a measure of how efficiently the transistor can turn on and off. SS is directly related to the quality of the interface dielectric/semiconductor.[97] The sub-threshold swing is defined as the inverse of the maximum slope of the I_D-V_{GS} plot and indicates the gate-source voltage needed to increase the drain current by one decade

$$SS = \left(\frac{dV_{GS}}{d\log_{10}(I_D)}\bigg|_{max}\right). \tag{1.5}$$

A low sub-threshold swing <100 mV/dec (together with a threshold voltage close to 0 V) is desirable to reduce the power consumption and the operating voltage in circuit applications.[102,104]

e. Contact resistance. Beside the above mentioned parameters, a less cited (but still important) parameter is given by the contact resistance (R_C) between the source/drain electrodes and the semiconductor. Controlling the contact resistance is especially important in short-channel devices ($L \lesssim 5\ \mu$m), since a high R_C value can lead to the degradation of both the device μ_{FE} and f_T.[105,106] In a TFT, the contact resistance depends on the source/drain electrodes,[107,108] the interface metal/semiconductor,[107] the source/drain to gate contact area,[106,108] as well as specific contact treatments (plasma, temperature, etc.) performed.[109] A well-known and utilized indirect method to extract R_C is the transmission-line method (TLM), which requires the linear I_D-V_{GS} curves of a series of TFTs with different channel lengths.[108] More specifically, R_C can be extracted from the total TFT resistance (R_T)

$$R_T = r_{CH} \cdot L + R_C, \tag{1.6}$$

where r_{CH} is the channel resistance per unit channel length.[108] By fitting the experimental values of the R_T-L plot for different V_{GS} with a linear curve, the total contact resistance can be estimated. Alternatively, the R_C can also be extracted from the ratio of two linear I_D-V_{GS} measurements taken on the same device (at two different V_{DS}), as explained by Campbell *et al.*[110]

f. Overlap capacitance. Besides the contact resistance, also the overlap capacitance C_{OV} between the gate contact and the source/drain electrodes is an important parameter, since it directly influences the TFT's transit frequency.[97] C_{OV} can be extracted from the capacitance-voltage (C-V) characteristics (Fig. 6), from which the total gate capacitance C_G can be estimated

$$C_G = C_{GS} + C_{GD} = C_{ox} \cdot W \cdot (L + L_{OV,TOT}), \tag{1.7}$$

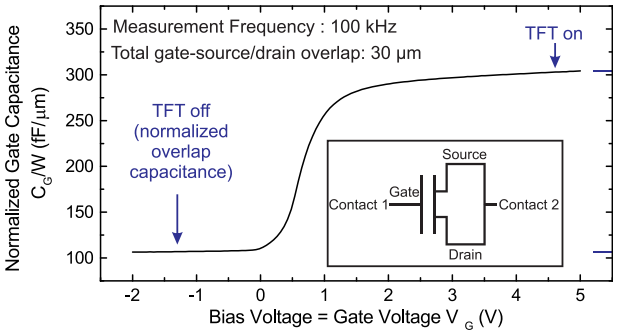

FIG. 6. Typical width normalized capacitance-voltage (C-V) characteristics of an n-type metal oxide semiconductor TFT (channel length $L = 30\,\mu m$) measured at 100 kHz. Inset: used measurement configuration.

where C_{GS} is the gate-source capacitance, C_{GD} is the gate-drain capacitance, and $L_{OV,TOT}$ is the total overlap length between the gate and the source/drain electrodes ($L_{OV,TOT} = L_{OV,S} + L_{OV,D}$).[97] The overlap capacitance $C_{OV} = C_{ox} \cdot W \cdot L_{OV,TOT}$ and can be extracted from the C-V plot (Fig. 6) as the minimum C_G value.

g. Transit frequency. The most important small signal (AC) parameter of a TFT is the transit frequency (f_T), which quantifies the speed of the device.[97] The f_T is given by the following formula:[111]

$$f_T = \frac{1}{2 \cdot \pi} \cdot \frac{g_m}{C_G} \propto \frac{\mu \cdot (V_{GS} - V_{TH})}{L \cdot (L + L_{OV,TOT})}, \tag{1.8}$$

where g_m is the transconductance ($g_m = \frac{dI_D}{dV_{GS}}$) calculated in the saturation regime. A first value of the transit frequency can be estimated from the g_m and C_G values extracted from the I_D-V_{GS} and C_G-V_{GS} data, respectively. A more precise value of the transit frequency can be calculated by measuring the TFT's S-parameters, i.e., by applying a low voltage RF voltage on top of the V_{GS} bias and subsequently measuring the $I_{DS,sat}$ of the devices.[112] From the device S-parameter measurement, the corresponding small signal current gain H_{21} can be calculated as a function of the frequency. The f_T is then given by the value where H_{21} equals 1 (see Fig. 13 for a practical example).[113,114]

C. Present issues and challenges

From 2003 onwards with the work of Hosono,[29,63] Wager,[51,60] Carcia,[52,59] and Fortunato,[57,58] metal oxide semiconductor TFTs have gained an increasingly interest, especially in view of their application in optical display backplanes. At the beginning, the attention has been mainly focused on the realization of metal oxide semiconductor TFT yielding high carrier mobility, as well as good stability under bias and illumination stress. In particular, the influence of semiconductor composition, passivation layer, gate dielectric, and source/drain electrodes on the device performance and stability have been extensively investigated, as reported in several reviews.[36,88,115] The enormous progresses achieved in the last ten years in these areas have directed current research efforts towards new directions and challenges.[36,88] In particular, the possibility to replace vacuum-processing techniques with higher throughput continuous processes is especially attractive in view of novel large-area and cost-effective applications, such as foldable and printable displays, disposable smart labels, and intelligent packaging.[87,116] To this aim, solution-processing techniques, especially spray pyrolysis (SP) or digitally controlled on-demand deposition methods like ink-jet printing, are gaining an increasing interest.[87] Another open issue is represented by the development of metal oxide semiconductor TFTs with good p-type conduction. Even if notable advances have been made in this direction, p-type metal oxide semiconductor devices can hardly yield performance levels similar to their n-type counterpart.[36,87] As explained later in this review, this is due to the specific charge transport characteristics of metal oxide semiconductors.[115,117] Due to the scarce availability of good p-type devices, the majority of the reported metal oxide semiconductor-based circuits are thus unipolar, employing only n-type TFTs. Even if complex large-area and high TFT count digital and analog electronic circuits have been demonstrated by employing only n-type metal oxide semiconductor TFTs, the development of a complementary technology based on both n- and p-type devices is essential to realize compact and low-power circuits.[118] To this purpose, research on complementary circuits based on hybrid metal oxide/organic or fully metal oxide semiconducting materials has expanded.[36]

All of the above mentioned topics apply for both rigid and flexible metal oxide semiconductor TFTs. Nevertheless, in the case of flexible substrates, the solution of the previously listed issues is even more challenging, due to the generally more complicated processing conditions (i.e., low temperature fabrication, substrate dimensional instability during TFT fabrication, and circuit integration). Furthermore, in the case of flexible TFTs, special care needs to be taken also on the mechanical properties of the devices (e.g., induced strain, maximum strain resistance, influence of strain on the TFT performance, and role of mechanical fatigue). Additionally, novel device features such as transparency, conformability, stretchability, biocompatibility, and biodegradability (with their related challenges) need also to be taken into account. In this review, we tackle all of the above mentioned issues and challenges, focusing only on devices fabricated on flexible substrates. To date and to the best of our knowledge, no report has specifically targeted this topic. We are only aware of a book chapter dealing with flexible solution-processed metal oxide semiconductor TFTs,[119] as well as two review articles, respectively, on the mechanical and electronic properties of flexible TFTs (all technologies)[30] and on p-type metal oxide semiconductor materials and devices (rigid and flexible).[120] For this reason, this paper presents the recent progresses in the field of flexible TFTs and circuits, based on both n- and p-type metal oxide semiconductors grown by vacuum- and solution-processing techniques. Main aim of this review is to underline the process/material/device/circuit requirements that are specific to flexible substrates compared with rigid ones and provide at the same time guidelines for the realization of flexible devices with good electrical and mechanical

properties, using metal oxide semiconductor technology. The reviews are structured as follows:

- In Section II, the state-of-the-art flexible n-type metal oxide semiconductor TFTs are presented. First, in Sec. II A, a short overview of the available metal oxide semiconductors is given. Then, in Sec. II B, flexible devices based on vacuum-processed metal oxide semiconductors are reviewed. Finally, in Sec. II C, flexible TFTs with novel solution-deposited metal oxide semiconductors are reported.
- Section III deals with the recent progresses in the field of flexible p-type metal oxide semiconductor TFTs. As for Section II, also in this case first a brief overview on the available materials is given Sec. III A; then in Sec. III B, flexible devices based on vacuum-processed metal oxide semiconductors are reviewed; finally in Sec. III C, solution-processed flexible TFTs are analyzed.
- Section IV reviews the state-of-the-art flexible circuits based on metal oxide semiconductors. Section IV A provides a basic explanation of the possible configurations, as well as of the basic operating principle of both digital and analog circuits. Then, in Sec. IV B, flexible unipolar digital and analog electronic circuits based on metal oxide semiconductors are presented. Finally, in Sec. IV C, flexible complementary metal oxide semiconductor-based circuits are reviewed.
- Section V deals with novel flexible electronic systems based on metal oxide semiconductor TFTs.
- In Section VI, the conclusions are drawn and an outlook over the field is given.

In order to provide a broad overview of the field, the first subsections of each section (II A, III A, and IV A) reference reports on both rigid and flexible substrates. However, the main subsections of this review (II B, II C, III B, III C, IV B, and IV C) deal only with flexible TFTs and circuits based on metal oxide semiconducting materials. We have done an exhaustive literature review on the topic and have tried to include all the relevant works until the submission of this review (April 2016). If there is some work not referenced, we apologize the authors in advance.

II. N-TYPE METAL OXIDE SEMICONDUCTOR TFTs

In this section, flexible n-type metal oxide semiconductor TFTs are presented. In particular, in Sec. II A, binary and multicomponent metal oxide semiconducting compounds are reported, together with a short explanation on the theory of these materials. Then in Sec. II B, a detailed description of the recent progresses obtained for flexible vacuum-processed metal oxide semiconductor TFTs is given, with a special focus on materials, fabrication techniques, electrical performance, and bendability. Finally, in Sec. II C, novel solution-processing methods to realize flexible metal oxide semiconductor TFTs are shown.

A. N-type metal oxide semiconductors

The first reported metal oxide semiconductors were binary compounds, such as SnO_2, ZnO, In_2O_3, and Ga_2O_3, in either a pure composition or with an impurity dopants. These binary materials are characterized by wide band gap $E_g > 3$ eV and large transmission in the visible range (above 80%).[115,121] The resulting films are n-type semiconducting, yielding a high carrier concentration (N) in the order of $10^{16}\,cm^{-3}$–$10^{21}\,cm^{-3}$, which is attributed to native donors, e.g., oxygen (O_2) vacancies and/or metal atoms.[115,121] Additionally, even if these films present an amorphous phase, they yield large $\mu_{FE} > 10\,cm^2\ V^{-1}\ s^{-1}$,[115] due to their unique electronic structure.[117] Indeed, in contrast to covalent semiconductors like Si, metal oxide semiconductors are valence compounds with a strong degree of ionicity within their chemical bonding.[87,117] In metal oxide semiconductors, charge transfer occurs from the metal orbitals (*s*) to the oxygen orbitals (2*p*). The conduction band minimum (CBM) is indeed formed by highly dispersive unoccupied metal orbitals, whereas the valence band maximum (VBM) is constituted by fully occupied and localized oxygen orbitals.[87,117] Those vacant metal orbitals are spherical (i.e., non directional) and exhibit large spatial spread.[115,117] As a consequence, electron transport can easily occur through the direct overlap of the metal orbitals in neighboring metal cations.[87,115,117] This explains why the majority of existing metal oxide semiconductors yield n-type conductivity, and hole transport is intrinsically hindered by a larger effective mass.[87] By employing binary metal oxide semiconducting materials (SnO_2, ZnO, In_2O_3, and Ga_2O_3) as active layers in TFTs, large differences in carrier mobility and current on/off ratios can be achieved. For example, In_2O_3 TFTs can lead to high μ_{FE} up to $100\,cm^2\ V^{-1}\ s^{-1}$, but at the same time also large I_{OFF} (due to high $N > 10^{18}\,cm^{-3}$).[36,122] Ga_2O_3 films possess large resistivity (due to low carrier density and large density of empty traps), resulting thereby in poor device performance ($\mu_{FE} = 0.05\,cm^2\ V^{-1}\ s^{-1}$).[36,123] Similar to In_2O_3, SnO_2 TFTs can reach higher carrier mobility, as well as larger off current.[62] The best-known and most performing binary metal oxide semiconductor is ZnO, which can lead to high μ_{FE} and I_{ON}/I_{OFF}.[36,88] However, most binary metal oxide semiconductors (especially ZnO) tend to form poly- or nano-crystalline structures, which lead to the creation of grain boundary defects and therefore non-uniform TFT performance over larger areas.[88,115] Compared with binary compounds, multicomponent metal oxide semiconductors, in general, result in better TFT performance.[36,115] In multicomponents, a stable amorphous phase can be achieved by mixing two or more metal cations with different ionic charges and sizes, whereas the incorporation of a stabilizer metal cation can be used to better control the carrier concentration.[117] For example, IZO presents a stable amorphous phase, which results in TFTs with good uniformity and μ_{FE}. Nevertheless, the high $N > 10^{17}\,cm^{-3}$ leads to high I_{OFF} and low I_{ON}/I_{OFF}.[36,115,124] Given the stronger bonds of gallium (Ga) with O_2, indium gallium oxide (IGO) leads to a lower carrier density, but at the same time also smaller μ_{FE}.[36] To realize an amorphous oxide semiconductor with large μ_{FE} and I_{ON}/I_{OFF}, in 2004 Nomura *et al.* proposed the introduction of Ga into IZO, developing IGZO, the most widely used metal oxide semiconductor nowadays.[29] IGZO

TFTs allow $\mu_{FE} \gg 10\,cm^2\,V^{-1}\,s^{-1}$ with $N < 10^{17}\,cm^{-3}$.[29,115] Alternatives to Ga doping in IZO have also been developed, using tin (Sn), hafnium (Hf), and zirconium (Zr).[88,125–127] At the same time, indium-free (and therefore cheaper) multicomponent metal oxide semiconductors (employing, for example, Sn, Al, or Zr) have also been demonstrated.[64,88] Finally, also other multicomponent materials like ZnON have been recently reported.[128–131]

1. Metal oxide semiconductors for flexible TFTs

Not all of the above mentioned metal oxide semiconducting materials have been employed as active layers in flexible TFTs.

a. Vacuum-processed metal oxide semiconductors. In the case of flexible vacuum-processed metal oxide semiconductor TFTs, amorphous IGZO is the most widely used material.[23,29,38,41,69,77,79–81,84,90,92,96,106,113,114,132–174] Flexible IGZO TFTs exhibit μ_{FE} up to $76\,cm^2\,V^{-1}\,s^{-1}$, depending on the stoichiometric composition employed. Also, c-axis aligned crystalline (CAAC) IGZO TFTs on plastic foils have been demonstrated.[39,175,176] Crystalline ZnO is the second most used metal oxide semiconductor in flexible TFTs, with μ_{FE} up to $50\,cm^2\,V^{-1}\,s^{-1}$.[59,78,177–183] Other metal oxide semiconducting materials used are: IZO with μ_{FE} up to $60\,cm^2\,V^{-1}\,s^{-1}$,[173,184–187] gallium zinc oxide (GZO) with μ_{FE} up to $20.7\,cm^2\,V^{-1}\,s^{-1}$,[188] and ZTO with μ_{FE} up to $14\,cm^2\,V^{-1}\,s^{-1}$.[64] Despite being considered a conductor, in general, thin layers of indium tin oxide (ITO) can also be used, yielding a μ_{FE} of $28.6\,cm^2\,V^{-1}\,s^{-1}$.[189]

b. Solution-processed metal oxide semiconductors. Most used solution-processed semiconductors are crystalline In_2O_3 and ZnO. For In_2O_3 TFTs, μ_{FE} up to $120\,cm^2\,V^{-1}\,s^{-1}$ have been reported,[76] including neat layers, nanoparticle (NP), or nanowire (NW) films, as well as blends of In_2O_3 and polyvinylpyrrolidon (PVP).[76,145,190–192] In the case of ZnO, the highest μ_{FE} values reached are of $7\,cm^2\,V^{-1}\,s^{-1}$.[193–195] Other solution-deposited metal oxide semiconductors include IZO with μ_{FE} around $4\,cm^2\,V^{-1}\,s^{-1}$,[196,197] ZTO with μ_{FE} of $0.04\,cm^2\,V^{-1}\,s^{-1}$,[198] and IGO with μ_{FE} of $0.4\,cm^2\,V^{-1}\,s^{-1}$.[199] Furthermore, solution-processed IGZO TFTs have shown excellent results with extremely high μ_{FE} values up to $84\,cm^2\,V^{-1}\,s^{-1}$,[83] either in the form of neat IGZO or in blends of IGZO and graphene nanosheets.[83,200,201]

B. Flexible n-type vacuum-processed TFTs

In this subsection, the recent advances in the field of flexible n-type vacuum-processed metal oxide semiconductor TFTs are reviewed. In particular, the materials and the fabrication techniques employed are first presented. Then, the electrical performance and the mechanical properties of the resulting devices are discussed. Finally, additional features such as dissolubility, mechanical activity, stretchability, and transparency are tackled.

1. Materials

The materials needed for the fabrication of flexible n-type vacuum-processed TFTs include flexible substrates, conducting materials to realize the source/drain and gate electrodes, dielectric materials for buffer, passivation and/or insulating layers, and most importantly metal oxide semiconducting active layers.

a. Substrates. In contrast to standard Si MOSFET technology, the substrate used for the realization of TFTs is, in general, not a part of the active device itself, since it only provides a surface for the fabrication process. Nevertheless, the substrate, especially if flexible, has a significant influence on the final TFT properties, as well as on the manufacturing process. The key requirements concerning the substrate are:

(I) The surface has to be compatible with standard thin-film fabrication technology, which calls for roughness values in the nanometer regime.
(II) The melting or glass transition temperature (T_m or T_G) of the substrate has to be high enough to be compatible with the chosen fabrication process.
(III) The substrate has to be bendable enough (in line with the mechanical requirements of the final devices) and at the same time has to provide sufficient stability for the manufacturing process.
(IV) The deformation of the substrate caused by temperature gradients, mechanical load, as well as absorption or desorption of gasses or liquids during the fabrication has to be smaller than the minimum device feature size.
(V) Vacuum-processing techniques call for small outgassing rates, compatible with the available deposition tools.
(VI) Concerning a future mass production and commercialization, the substrates should be at least potentially available in large quantities and sizes, as well as cheap.
(VII) Furthermore, the substrate needs to be resistant to the chemicals used during the fabrication process, especially photoresists and developers.
(VIII) Finally, specific applications require substrates which are transparent, light-weight, conformable, stretchable, biocompatible, and even biodegradable.

All these requirements have led to the evaluation of a large variety of different substrates. Due to their properties and their availability, polymers are the natural choice and the most commonly used substrate materials. Among the different polymers, polyimide (PI) foils with thicknesses (t_S) between 5 μm and 125 μm are the most frequently utilized substrates,[135,145,152,157,158,160,165,172,177,180,184,188,189] together with PI and nano silica.[142,144] This is because of the numerous advantages of PI (commercially known as Kapton®), like a small coefficient of thermal expansion (CTE) of 12×10^{-6} K, a small humidity expansion coefficient (HEC) (9×10^{-6}%RH), a high T_G of ≈360 °C, and a surface roughness in the nanometer range.[114,155] Since standard PI exhibits a yellowish to brownish color, other polymeric substrates have been introduced to benefit from their transparency in the visual wavelength range. These materials, which

are, in general, also cheaper and more easily available, include PET,[29,69,96,165,171,180,184,188] polyethylene naphthalate (PEN),[38,40,41,134,136,139,149,153,158,163,166–168,173,181,202] polyetheretherketone (PEEK),[203] polycarbonate (PC),[154,157] polypropylene (PP) based synthetic paper,[204] parylene,[80,141] polyethersulfone (PES),[178] water-soluble polyvinyl alcohol (PVA),[82] as well as polydimethylsiloxane (PDMS).[78,132,147,205–207] In particular, PDMS is also stretchable and biocompatible, but at the same time hard to process using standard fabrication techniques.[78,132,147,205] An alternative to polymers is constituted by metal foils, such as Al foils,[156] and stainless steel substrates.[148] The main benefit of metal foils is the high T_m (above 1000 °C in the case of stainless steel).[155] Nevertheless, metallic substrates are conductive and thus require additional insulating buffer layers, which further increase weight and decrease flexibility. Other typologies of supports include flexible and transparent glass substrates (with high temperature resistance),[160,174] glass-fabric reinforced composites,[93,169] cheap and biodegradable cellulose fiber-based paper,[77,79,189,208] as well as nontoxic biological paper like beeswax.[186] Additionally, also standard tracing paper (STP) and lab paper samples (LPS) have been employed. Finally, mechanically active multilayer substrates using a highly cross-linked hydrogel swelling layer and a stiff PI have been shown.[23]

b. Barrier layers. Before starting the effective TFT fabrication, often buffer or encapsulation layers are deposited on top of the substrate itself. Although there are numerous examples of flexible n-type vacuum-processed metal oxide semiconductor TFTs manufactured without barrier layers, there are several reasons why an encapsulation of the substrate is beneficial, including:

(I) The need to electrically insulate a conductive substrate (e.g., Al or stainless steel).
(II) A reduction of the substrate surface roughness by the deposition of a smoothing layer.[41]
(III) A reduction of the absorption and desorption of solvents during the fabrication process by decreasing the effective humidity expansion coefficient (HEC).
(IV) An improvement of the adhesion between the substrate and the device layers.
(V) A reduction of the substrate outgassing in low pressure environments to speed up the pumping steps during the deposition process.
(VI) A decrease of the substrate permeability by decreasing the effective water vapor transmission ratio (WVTR).

Typical adhesion or buffer layers are made of silicon nitride (SiN_x),[92,106,113,114,140,143–146,150,151,173,182,183] silicon oxide (SiO_x),[78,82,135,148,154,157,168,170,181,205] and photoresist sandwiched between SiN_x and SiO_x.[158] Organic materials,[78,82,136,148,154,157,168,170,181,205] in particular, SU8,[153] or PVP is especially well-suited as smoothing layers.[152,172] A direct comparison of the influence of different buffer layers (50 nm SiO_x, 50 nm SiN_x, or 50 nm SiN_x in combination with 10 nm or 100 nm AlO_x) on the performance of TG IGZO TFTs on PI substrate is given by Ok *et al.*, as shown in Fig. 7.[155] The buffer layer with the smallest WVTR = 0.033 g/(cm^2 day) is given by 50 nm SiN_x + 100 nm AlO_x. As shown by Ok *et al.*, this buffer layer is able to reduce the carrier trapping at water related defects and results in the best device performance and stability (Fig. 7). Consequently, several groups have published the use of multi-layers which can potentially combine the advantages of different materials. These layer stacks include organic TR-8857-SA7 with Al_2O_3,[139,202,204] undefined organic layers in combination with Al_2O_3,[93,167] as well as SiO_2.[40] The most complex published structure is a $SiO_2/SiN_x/SiO_2/SiN_x/SiO_2$ sandwich layer (also used to engineer the strain in the stack)[133,164] and other multi-stacked SiO_2/SiN_x barrier layers.[137,177] Finally, 3 nm thick SiO_2 has been used as insulating encapsulation of conductive metal substrates.[148]

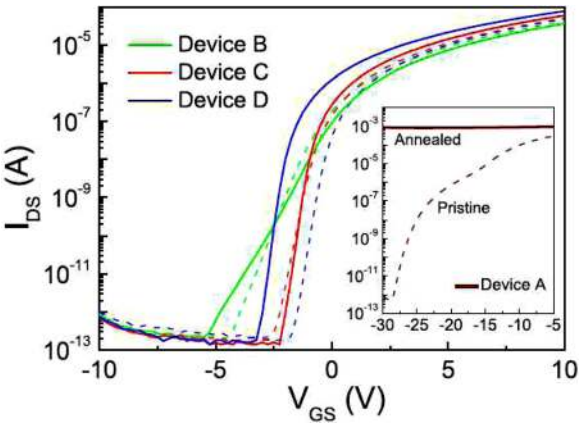

FIG. 7. Transfer characteristics of flexible IGZO TFTs with 50 nm silicon nitride (SiN_x)/10 nm aluminum oxide (AlO_x) (Device B), 50 nm SiN_x/100 nm AlO_x (Device C), or 50 nm silicon oxide (SiO_x) (Device D) barrier layers on PI substrate. The inset shows a TFT (Device A) with a 50 nm SiN_x buffer layer. All measurements are for pristine (dashed line) and 250 °C-annealed TFTs (solid line). Reproduced with permission from Appl. Phys. Lett. **104**, 063508 (2014). Copyright 2014 AIP Publishing LLC.

c. Gate dielectrics. Together with the metal oxide semiconductor, also the gate dielectric plays a fundamental role. This is mainly due to the following reasons:

(I) As visible from Equation (1.1), the drain current I_D is directly proportional to $C_{ox} = \frac{\epsilon_R}{t_{ox}}$, where ϵ_R and t_{ox} are, respectively, the dielectric constant and the thickness of the gate dielectric. For low-voltage TFT operation, thin gate dielectric materials with high ϵ_R are desirable.
(II) The insulation properties, correlated with the specific resistance and the pinhole density (and therefore the layer deposition quality) of the dielectric material, define the gate leakage of the device (the so called gate current I_G).
(III) The quality of the interface between the gate dielectric and the semiconductor can strongly influence the carrier mobility, as well as the stability of the TFT, by determining the interface trap density.

The most widely used gate dielectric is aluminum oxide in different forms, such as Al_2O_3,[23,41,59,80,81,93,96,145,147,162,169,178,179,183,202] AlO_x,[155] and also anodized Al_2O_3 on Al gates.[153,168] Additionally, anodic neodymium-doped AlO_x (AlO_x:Nd) on aluminum

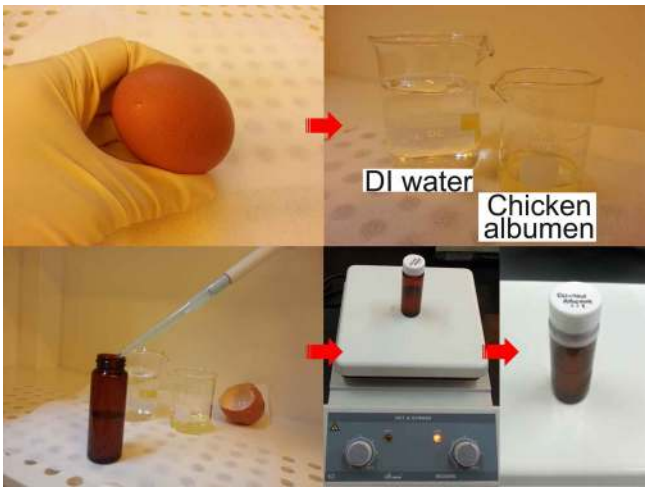

FIG. 8. Chicken albumen ferroelectric gate dielectric: preparation procedure for diluted chicken albumen solution. Reproduced with permission from Kim *et al.*, Appl. Mater. Interfaces **7**, 4869 (2015). Copyright 2015 American Chemical Society.

neodymium (AlNd) gates has been used.[158] The advantages of aluminum oxide are comparably high ϵ_R around 9.5, low pinhole density if deposited by atomic layer deposition (ALD), and, especially in combination with IGZO, a good interface quality. Employed materials with a higher ϵ_R include hafnium oxide (HfO_2),[177,180,181] hafnium lanthanum oxide (HfLaO),[170] titanium oxide (TiO_2),[154] and yttrium oxide (Y_2O_3).[29,69] The drawback of these dielectrics is a scarcer availability, a worst interface quality, as well as a reduced compatibility with the TFT fabrication process. At the same time, silicon oxide (either SiO_2[40,78,133,137,138,148,163,164,166,173,174,188,205] or SiO_x) is a more established material but results in a reduced specific gate dielectric capacitance C_{ox} ($\epsilon_R \approx 3.9$).[82,156] Even if a direct comparison between SiO_2 and SiN_x by Lim *et al.* showed that IGZO TFTs with SiN_x dielectric exhibit slightly better performance than those with SiO_2,[171] SiN_x is only rarely used in the community.[134,142,159,160] Besides metal oxide dielectrics, also organic materials have been used as gate dielectric, such as layers made from olefin polymers,[38] or cross-linked PVP (c-PVP).[165] To this regard, a direct comparison of c-PVP and SiO_2 showed that both materials have a comparable ϵ_R and result in flexible IGZO TFTs with similar performance parameters,[165] although the thick c-PVP layer ($t_{ox} = 280$ nm) reduces C_{ox} if compared with the thinner SiO_2 ($t_{ox} = 170$ nm). A third class of gate dielectrics is ferroelectric materials, in particular, poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)].[132,136,149,167] P(VDF-TrFE) can be reversibly polarized and hence used for the fabrication of non-volatile memory TFTs. Interestingly, recently also chicken albumen ferroelectric gate dielectrics have been demonstrated, as shown in Fig. 8.[204] A fourth class of gate dielectric materials is constituted by solid electrolytes (e.g., phosphorus (P)-doped SiO_2), which are characterized by high specific gate dielectric capacitance per unit area (C_{ox}) and therefore low-voltage device operation.[184,189] This improvement is generally ascribed by a redistribution of mobile ions with the applied voltage. Fig. 9 illustrates how P-doped SiO_2

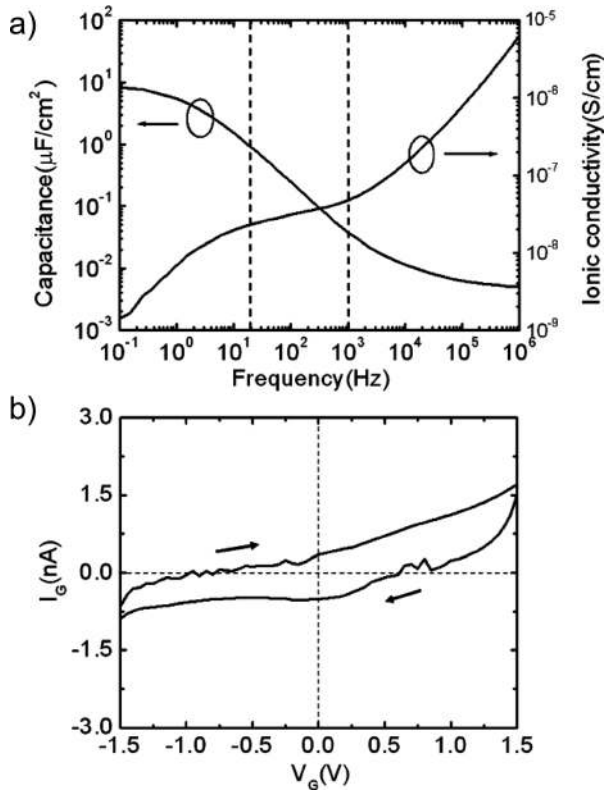

FIG. 9. Phosphorus-doped SiO_2 solid electrolyte dielectric: (a) total gate capacitance (C_G) and ionic conductivity, as well as (b) leakage current (I_G) through the electrolyte. Reproduced with permission from Jiang *et al.*, IEEE Electron Device Lett. **33**, 65 (2012). Copyright 2012 Institute of Electrical and Electronic Engineers.

gate dielectrics allow achieving high C_{ox} values of up to 13 μF cm^{-2}. To combine the advantageous properties of different dielectric materials, a variety of hybrid and multi-layer materials have been utilized as gate dielectrics for flexible n-type vacuum-processed metal oxide semiconductor TFTs. These include: TiO_2 with HfO_2,[157] PVP-Al_2O_3,[152] or PVP with methylcyclohexane (pp-MCH) and Al_2O_3,[172] SiN_x with SiO_x,[135,144] tri-layer stacks like TiO_2 sandwiched between SiO_2 or TiO_2 sandwiched between HfO_2,[154] as well as P(VDF-TrFE) with Al_2O_3.[146] Finally, an interesting approach is constituted by the use of a paper substrate as gate dielectric.[77,79,186,208] Although the paper thickness is as high as 75 μm, a C_{ox} value of 4×10^{-4} F m^{-2} was achieved.[79] This is because the dielectric properties are determined by an arbitrary serial and parallel combination of discrete fiber capacitors within the paper substrate. The large choice concerning possible dielectrics results in a big variety of published C_{ox} values ranging from 1.2×10^{-4} F m^{-2} measured for an organic layer[165] up to 1.3×10^{-1} F m^{-2} for a solid electrolyte.[184] Finally, ZnO was sandwiched between two layers of Al_2O_3 to create a charge trapping layer in the gate dielectric, leading to non-volatile memory TFTs.[139]

d. Contacts. This class of materials includes metals and other conductors employed to fabricate gate and source/drain electrodes. Since the gate contact of a TFT (and in general of a FET) does not need to conduct a significant amount of current, the material is, in general, selected to achieve a high

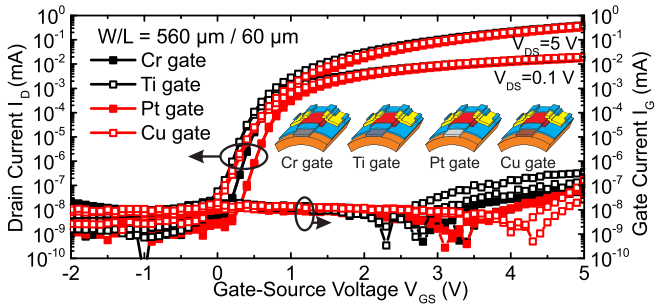

FIG. 10. Transfer characteristics of flexible IGZO TFTs fabricated using different gate metals: chrome (Cr), titanium (Ti), copper (Cu), and platinum (Pt), all exhibiting similar electrical performance. Reproduced with permission from Münzenrieder *et al.*, in *Proc. of Eur. Solid-State Device Res. Conf.* (*ESSDERC*) (2013), pp. 362–365. Copyright 2013 Institute of Electrical and Electronic Engineers.

compatibility with the TFT fabrication process. This issue was also addressed by a direct comparison between different gate metals like chromium (Cr), titanium (Ti), copper (Cu), and platinum (Pt).[84] Fig. 10 displays the corresponding transfer characteristics showing that although the work function of the various gate metals is different, their influence on the electrical performance of IGZO TFTs is minor.[84] Consequently, a variety of different metals: silver (Ag),[189] Al,[59,132,149,153,174,178,202,204] Au,[38,136,167] Cr,[23,81,84,113,140,141,143,150,151,179,182,183] Cu,[84,92,145,146] molybdenum (Mo),[41,82,132,137,138,148,163,164,166,173] nickel (Ni),[152,172] Pt,[84] Ti,[84,90,106,114,144,147,169] as well as AlNd,[156,158,168] molybdenum titanium (MoTi),[155] and tantalum nitride (TaN) metal alloys have been used as gate contacts.[154,157,170] Especially for BG TFTs, the adhesion of the gate contact to the flexible substrate appears to be the main concern. To this aim, Cr and Ti show good results, whereas Cr often suffers from a high built-in strain.[90] Multi-layer metals offer, in general, a compromise between good adhesion and high conductivity, especially in the case of Ti/Au,[23,96,181] Ti/Cu,[135] Cr/Au,[174] or Ti/Au/Ti gate stacks.[162] Besides metals and metal alloys, ITO,[29,69,78,80,135,139,165,177,180,184,188,205] IZO,[77,79,133,160,208] In_2O_3,[171] and aluminum zinc oxide (AZO) have been used to fabricate transparent gate contacts.[93,134] Furthermore, dual-layers of metal and ITO[40] or IZO have also been employed.[142] As regards source/drain electrodes, the material has to provide a high conductivity and at the same time a small contact resistance with the active layer. Moreover, also other properties like adhesion or transparency need to be considered. These requirements resulted in the use of different metals: Al,[77,149,152,154,157,165,170,172,179,208] Au,[38,167] Cu,[147] Mo,[41,82,137,138,148,164,168] palladium (Pd),[145] and Ti,[90,93,144,169] whereas Mo and Ti seem to exhibit the lowest specific contact resistance R_C. At the same time, a big variety of multi-layer contacts have been developed to combine the advantageous properties of different materials; recent examples are: Ti/Au,[59,69,81,84,113,140,141,143,146,150,151,181–183] Ni/Au,[79] Mo/Al,[166,173] Cr/Au,[114] Mo/AlNd,[156] Cr/Au/Cr,[92] Mo/Al/Mo,[153] Ti/Au/Ti,[162] or Ti/IZO.[142] Regarding transparent source/drain contacts, only ITO[29,78,80,106,139,155,158,177,180,188,189,202,204,205] and IZO have been used.[160,171,184] Finally, contacts based on Ti (drain) and graphene (source) in combination with a VTFT structure have been published.[96]

e. Passivation layers. The performance of BG TFTs can be improved by depositing a final back channel passivation layer. This can lead to the following advantages:

(I) An increase of the environmental and electrical stability of the TFTs by a reduced interaction between semiconductor and atmosphere (in particular, less interaction of the active layer with oxygen and water).
(II) An encapsulation of the TFTs from a mechanical point of view.
(III) A protection of the devices during post-processing steps like the fabrication of additional devices, such as organic light emitting diodes (OLEDs) or touch screens.

To simplify the fabrication process, it is quite common to passivate the device using the same material already used for the gate dielectric. Furthermore, Al_2O_3 passivation layers are widely used because of the low oxygen transmission rate (OTR) of $\approx 1.26 \times 10^{-4}$ mol/(m^2 day) and WVTR rate of $\approx 6.61 \times 10^{-2}$ mol/(m^2 day) (both measured for a 8 nm thick Al_2O_3 layer on PET).[90] Al_2O_3 passivation layers result in BG metal oxide semiconductor TFTs with significantly improved stability, compared with unpassivated devices.[80,81,84,113,114,140,143,150,151,179] For similar reasons, also SiO_2,[164,166,168,173] SiO_x,[133,156] and TiO_2 have been used.[157] Additionally, organic layers such as photoresist,[103,153] SU8,[78,158,205] tetratetracontane,[152] and polychloroprene in combination with Al_2O_3 have been utilized to passivate flexible n-type vacuum-processed metal oxide semiconductor TFTs.[23]

2. Fabrication techniques

The fabrication of flexible n-type vacuum-processed metal oxide semiconductor TFTs employs standard semiconductor fabrication tools. Nevertheless, the large variety of available substrates with different physical and chemical properties has led to the use of a wide range of different techniques. These include several approaches to handle the flexible substrates, as well as to deposit and structure the various device layers.

a. Substrate preparation. The choice of the substrate is important, since it limits the maximum allowed temperature, as well as the typology of chemicals that can be used during the fabrication process. At the same time, the mechanical properties of the flexible support also determine the way how the substrate can be handled. Up to now, free-standing flexible substrates have been widely employed.[93,96,134,145,154,156,157,165,172,178,180,184,188,189,209] Free-standing foils are a natural choice for the fabrication of flexible devices because they are compatible with large-scale substrates and future roll-to-roll processes. Furthermore, the mechanical robustness of free-standing foils results in an insensitivity against mechanical shocks. At the same time, free-standing substrates also present the following drawbacks:

(I) They have to be sufficiently thick and stable to be mechanically handled with tweezers.

(II) They can suffer from expansion caused by temperature gradients or by the absorption of solvents.
(III) They have to be temporarily attached to a rigid carrier at least during the use of standard photolithographic tools.

One way to simplify the use of photolithographic tools like mask aligners or spinners is to bond the flexible foil to a glass or silicon wafer for the complete fabrication process.[40,41,132,136,139,153,158–160,163,166–170,173,174,202,204] This can either be done using native adhesion forces or utilizing an additional adhesive. Alternatively, a flexible foil can also be mechanically fixed on particularly designed holders using metallic clamps.[162] In alternative to flexible substrates manufactured independently from the TFTs, it is also possible to create the flexible substrate by covering a host substrate with a polymer using either evaporation,[80,81,141] spin, slot or blade coating techniques.[23,39,133,135,137,142,144,147,155,161,164,179] The advantages of these fabrication techniques based on a rigid support are a high compatibility with the standard fabrication processes on Si or glass wafers, a reduction of the expansion of the substrate during the manufacturing process, as well as the possibility to realize devices on very thin ($\approx$1 μm) substrates. After the TFT fabrication is completed, the flexible foils or thin deposited polymer layers carrying the devices can be separated from the rigid support using: (1) mechanical peeling,[38,142,155,158,161,164,166,168,179] (2) a low adhesion releasing layer,[133,144] (3) a supporting laser,[137] or (4) a sacrificial layer between the host carrier and the polymer.[78,80,81,141,147] To this regard, a direct comparison of different releasing methods by Lin *et al.* showed that mechanical peeling of the flexible substrate from the hosting carrier wafer can lead to deformation and cracking of the TFTs in case of high adhesion forces between the polymer and the carrier.[144] To increase the mechanical stability or to realize electronic devices on alternative surfaces, thin flexible substrates have also been transferred and attached to a new carrier like PI or organic tissues.[38,39,78,80,81,141] Finally, it is also possible to fabricate TFTs directly on a rigid carrier coated with a sacrificial layer and subsequently transfer only the devices onto a flexible substrate.[38,78,82,205] In addition to the different handling possibilities, the substrate preparation typically includes a heat treatment step prior to the device fabrication itself. In the case of fabrication on free-standing plastic foil or foil bonded to a host substrate, the substrate is backed at high temperatures (around 200 °C) for several hours, to remove trapped residualliquids.[84,90,92,106,113,114,132,143,145,146,151,152,170,172,182,209] This step allows also pre-shrinking flexible substrates which are not permanently attached to a rigid support.

b. Deposition methods. Besides the standard criteria used for thin-film deposition techniques on Si or glass wafer (e.g., homogenous and dense layers), there are extra requirements which are especially important for the realization of flexible devices. These include:

(I) Low temperatures, compatible with the thermal resistance of the employed flexible substrates.
(II) A sufficient adhesion of the deposited materials to the substrate, in order to prevent a possible delimitation of the layers, especially when the substrate is bent.
(III) Finally, the strain built in the deposited materials has to be small enough to allow good mechanical properties (e.g., bendability) of the final devices.

The predominant technique to deposit n-type vacuum-processed metal oxide semiconductors is sputtering. RF and RF-magnetron sputtering have been used to deposit IGZO,[23,80–82,96,132,134–136,139,145,147,152,155,156,202,208] IZO,[184] GZO,[188] and ZnO.[59,78,177,178,180] Furthermore, IGZO was also deposited by DC sputtering[133,137,153,160,168] and pulsed DC sputtering.[40] The advantages of sputtering are the large availability of sputter tools, the low temperature (typically room temperature) deposition, as well as the good adhesion and dense structure of the final layers. Additionally, sputter tools offer several opportunities to optimize the layer properties, by adjusting the power and/or the sputtering pressure. Also, reactive sputtering using different concentrations of Argon (Ar) and O_2 has been used to adjust the oxygen content in the metal oxide semiconducting active layer.[41,59,69,79,133,134,136,142,144,149,154–157,159,170] An even better control of the stoichiometric composition of IGZO is possible by using co-sputtering techniques based on an IZO and a Ga_2O_3 target.[158] Among all the n-type metal oxide semiconductors, ZnO is the only one that can be deposited by ALD,[93,139,182,183] plasma enhanced atomic layer deposition (PEALD),[179] and PLD.[29,181] Even if ALD has the advantage that the layers are conformal, the process is slow and less prone to variations of the chemical composition.

The deposition of insulating layers to realize gate dielectrics, passivation, or barrier layers aims at a high ϵ_R, a low pinhole density, and a good sidewall coverage. This is why conformal deposition techniques are particularly well-suited: ALD[23,41,80,81,139,140,145–147,152,155,162,172,178,183,202,204,209] and PEALD of Al_2O_3,[179] ALD of HfO_2,[177] as well as plasma-enhanced chemical vapor deposition (PECVD) of SiO_2,[78,82,133,135,137,144,148,156,164,165,171,173,188,205] SiN_x,[134,135,142,144,159,160,171] SiO_2:P,[184,189] but also organic pp-MCH.[172] These depositions are, in general, done at temperatures between 150 °C and 200 °C. Sputtering also results in comparably conformal layers and has therefore been used to deposit Y_2O_3,[69] SiO_2,[40,174] and HfO_2,[180] whereas PLD has only been employed to grow Y_2O_3.[29] Although evaporation of metal oxides requires high temperatures, different dielectrics (Al_2O_3,[59] HfLaO,[170] SiO_2,[154] TiO_2,[154,157] and HfO_2) have been deposited by electron-beam evaporation.[157] Besides the mentioned vacuum-deposition techniques, high-quality Al_2O_3[153,168] or Al_2O_3:Nd gate dielectrics have also been grown anodizing a metallic gate.[158] Finally, organic layers, in particularly PVP,[152,165,172] chicken albumen,[204] or P(VDF-TrFE), have been spin coated.[132,136,146,149,167]

As regards the deposition techniques of conductive materials, we have to distinguish between metals and transparent metal oxide conductors. Metals are typically deposited using e-beam evaporation,[23,80–82,106,136,145–147,152,174,208,209] thermal evaporation,[149,152,157,165,167,178,179,202,204] or sputtering.[96,135,137,144,148,153–158,166,168,170,173,174,189] Among these

techniques, the most common is evaporation, due to the non-conformal shape of the resulting layers that is beneficial for subsequent lift-off processes. Non metallic but transparent metal oxide conductors have been fabricated by sputtering (ITO,[78,80,106,135,139,155,158,165,188,189,202,204,205] In_2O_3,[171] AZO,[134] and IZO[77,79,133,160,171]), by e-beam evaporation (ITO[177]) or by PLD (ITO[29]). It is worth mentioning that also graphene monolayers grown by chemical vapor deposition (CVD) and transferred to a flexible PET substrate can be employed, as reported by Liu *et al.*[96]

Some of the presented deposition procedures (e.g., from Li and Jackson[179] or Cherenack and Tröster[182]) are designed in a way that the semiconductor and the gate dielectric can be deposited with the same tool.[179,182] In this way, it is possible to avoid the surface contamination caused by breaking the vacuum and transferring the sample to another tool. However, there is no clear evidence in literature that breaking the vacuum necessarily leads to a degenerated device performance.

c. Layer structuring. As for the structuring of layers on rigid wafers, patterning of thin-films on flexible substrates is mainly done by etching and lift-off processes. However, the definition of flexible structures needs to be adapted to the mechanical and chemical properties of the substrates. Since the most common substrates, in particular, PI foils, are resistant to standard photolithographic chemicals, UV lithography is widely used.[40,81,82,96,147,152,153,155–157,160,161,163,168,179,204] Employing etching and lift-off processes allows realizing flexible structures with lateral feature size down to 1 μm.[106] If the chosen substrate is not resistant to chemicals (e.g., photoresists, developers, and/or strippers) and if feature sizes $\gg 1\,\mu$m are sufficient, shadow masking can be used.[59,132,135,162,165,170,172,189,208] Shadow mask structuring does not require any photoresist baking step and allows therefore preventing unintended annealing of the devices, as well as undesired thermal load of the substrate leading to subsequent expansion. The problem of substrate expansion is illustrated by the fact that a 7.6 cm × 7.6 cm large PI substrate undergoes an expansion of $\approx 25\,\mu$m (in each direction) during a 150 °C TFT fabrication process.[114] Due to this expansion, tolerances of $\approx 10\,\mu$m on the photolithographic masks are necessary, limiting thus the minimum feature sizes that can be achieved. In particular, special care needs to be taken during the alignment of the source/drain contacts to the gate electrode, which can result in large total overlap lengths $L_{OV,TOT}$ and therefore low transit frequency f_T (see Equation (1.8)). The problem of source/drain contacts misaligned with respect to the gate electrode is practically shown in Fig. 11 for a flexible IGZO TFT. A solution to misalignment caused by thermally induced substrate expansion is constituted by self-aligned lithography. Due to the transparency of the majority of flexible substrates, the photoresist can be structured using back-side exposure and predefined opaque patterns (e.g., metallic BG contacts).[106,114,209] In this way, there is no need for tolerances on the photolithographic masks and feature sizes down to 0.5 μm are possible.[209] Fig. 11 displays a direct comparison of TFTs fabricated using standard and self-aligned lithography. Furthermore, by using

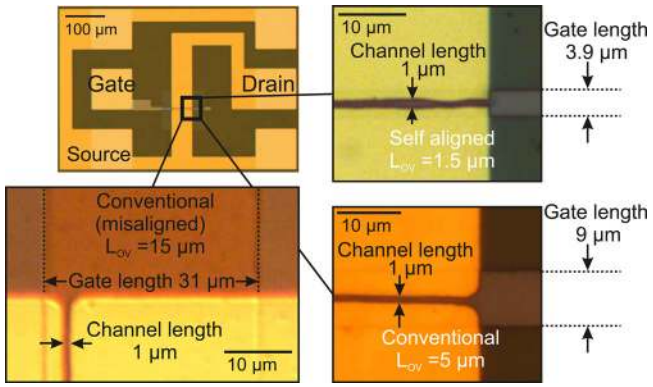

FIG. 11. Micrographs of flexible IGZO TFTs fabricated on free-standing PI foil using standard or self-aligned (SA) lithography to align and structure the source/drain (S/D) contacts relative to the BG. Misalignment due to substrate deformation calls for tolerances limiting the minimum feature size, whereas self-alignment enables smaller TFTs. Reproduced with permission from Appl. Phys. Lett. **105**, 263504 (2014). Copyright 2014 AIP Publishing LLC.

a TG configuration with metallic gate contacts, it is also possible to self-align SiO_2 gate dielectric to Mo gate electrodes in an RIE process.[137] This approach has the additional advantage that the RIE plasma increases the conductivity of the active layer (IGZO) in the contact areas.[137] Similarly, TG IGZO devices with highly conductive IGZO source/drain electrodes self-aligned to Mo gate contacts can be realized by PECVD-growing a SiN_x after the TG patterning.[138] Here, this SiN_x layer allows increasing the conductivity of IGZO in the contact area (not covered by the TG electrode) and thereby forming SA S/D electrodes.[138]

d. Device configuration. For flexible n-type vacuum-processed metal oxide semiconductor devices, the four main TFT configurations (see Sec. I B) have been employed:

(I) The most common TFT geometry is the BG,[40,80–82,147,152,153,156,160,161,163,166,168,174,179,208] either coplanar (Fig. 4(a)) or staggered (Fig. 4(b)). Some groups have also reported BG TFTs employing a continuous conductive bottom gate (either a metallic substrates or a metallic deposited layer).[180,184,189]

(II) TG structures (Figs. 4(c) and 4(d)) have also been utilized,[29,38,59,136,142,144,146,147,149,155,159,167,178,202,204] especially in combination with fragile gate dielectrics that does not survive extensive processing and/or chemicals [e.g., P(VDF-TrFE)].

(III) DG TFTs (Fig. 4(d)) have been used to improve the TFT DC performance, as well as the device environmental stability.[90,106]

(IV) Finally, also flexible VTFTs (Fig. 4(e))[92,93,96] and QVTFTs with short channel lengths (down to 300 nm (Ref. 145)) and reduced device footprint have been presented.

3. Electrical properties

One of the main reasons why flexible metal oxide semiconductor TFTs have received an increasingly amount of attention in the last years is their electrical performance,

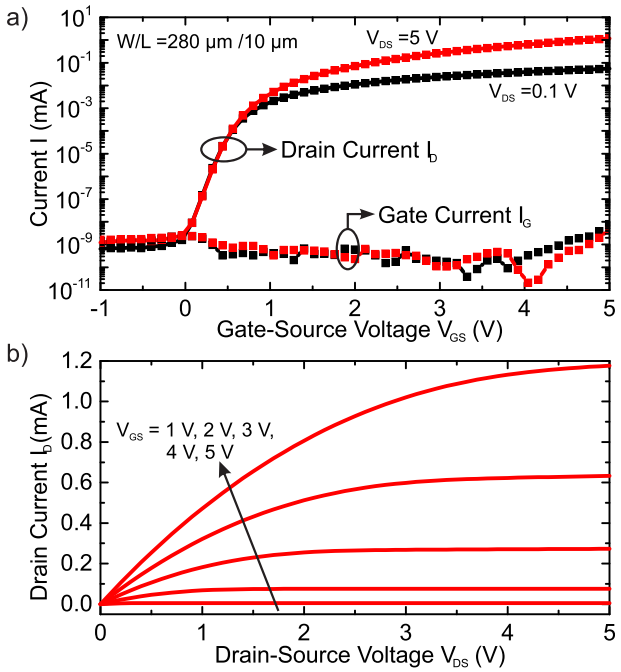

FIG. 12. Typical transfer (a) and output (b) characteristic of a flexible IGZO TFT. Reproduced with permission from Münzenrieder *et al.*, IEEE Trans. Electron Devices **59**, 2153 (2012). Copyright 2012 Institute of Electrical and Electronic Engineers. Performance parameters extracted from the shown data are: field-effect mobility $\mu_{FE} = 15.1\,\mathrm{cm^2\ V^{-1}\ s^{-1}}$, threshold voltage $V_{TH} = 1.0\,\mathrm{V}$, sub-threshold swing (SS) = 102 mV/dec, and current on/off ratio $I_{ON}/I_{ON} = 9.5 \times 10^8$, resulting in a specific transconductance g_m/W (at $V_{GS} = 5\,\mathrm{V}$) of $2.02\,\mathrm{S\ m^{-1}}$.

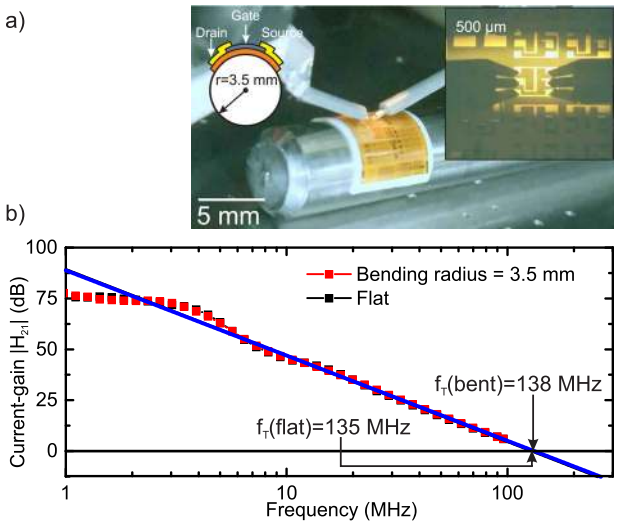

FIG. 13. Frequency characterization of the fastest flexible metal oxide semiconductor TFT: (a) photograph of a bent device contacted with ground-signal-ground (GSG) probes and connected to a network analyzer; (b) frequency-dependent small signal current gain (H_{21}) extracted from S-parameter measurements, with corresponding extracted transit frequency f_T. Reproduced with permission from Münzenrieder *et al.*, IEEE Trans. Electron Devices **60**, 1 (2013). Copyright 2013 Institute of Electrical and Electronic Engineers.

which is superior to other flexible TFT platforms, especially organic and a-Si technologies (see Table I). A typical transfer and output characteristic of a flexible n-type vacuum-processed metal oxide semiconductor TFT (in this case based on IGZO) are plotted in Fig. 12. The DC performance parameters of the shown device are given in the figure caption. The best DC performance parameters ever reported for flexible n-type vacuum-processed metal oxide semiconductor devices include: a μ_{FE} of $76\,\mathrm{cm^2\ V^{-1}\ s^{-1}}$,[154] a SS as low as 69 mV/dec,[90] and an I_{ON}/I_{OFF} up to 2×10^{10}.[84] Furthermore, a wide range of positive and negative threshold voltage values have been presented, illustrating that it is possible to realize both enhancement and depletion mode TFTs.[152,168] Even if the AC performance of flexible TFTs is an important parameter (e.g., for analog integrated circuits), the transit frequency is rarely measured and reported. As explained in Section I B and shown in Fig. 13, the transit frequency f_T can be directly measured by extracting the small signal current gain H_{21} of the devices.

A few direct measurements of the transit frequency of flexible n-type vacuum-processed metal oxide semiconductor TFTs resulted in values in the MHz regime,[113,114,209,210] with the highest f_T value of 135 MHz reported for a flexible self-aligned IGZO TFT (Fig. 13).[114] The demonstrated frequency values show that metal oxide semiconductor TFTs can already be used for applications like flexible radio-frequency identification (RFID) tags or amplitude modulation (AM) radios.

a. Device optimization. Numerous techniques have been proposed to improve the electrical performance of flexible n-type vacuum-processed metal oxide semiconductor TFTs, ranging from material and process engineering to device structure modifications. Table II presents an overview of the performance of recently published flexible n-type vacuum-processed metal oxide semiconductor TFTs. Each of the devices shown in Table II yields at least one of the best performance parameters ever reported for flexible n-type vacuum-processed metal oxide semiconductor TFTs.

These results have been possible thanks to several optimization approaches:

(I) The probably simplest way to influence the device performance is to expose the TFTs to high temperatures either during or after the fabrication process. Annealing at or around 200 °C is a common way,[40,82,132,134–137,152,153,155,156,158,160,165,168,208] whereas temperatures above 260 °C[159] are not possible due to the limited thermal resistance of the majority of the (polymeric) substrates. Nevertheless, flexible glass and metal substrates allow higher annealing temperatures of 300 °C,[156,160] 330 °C,[205] and even 400 °C.[174] An investigation of the influence of annealing on e-beam evaporated TiO_2 gate dielectrics showed that for annealing temperatures below 200 °C, the I_G only weakly depends on the temperature but decreases by approximately one order of magnitude if the annealing temperature is increased to 300 °C.[154] Besides traditional post-deposition annealing of thin-films, also the deposition of metal oxide semiconductors at high temperatures influences the performance. Fig. 14 shows TFTs based on IGZO deposited at elevated temperatures.[168] In this case,

TABLE II. Set of performance parameters extracted from recently demonstrated flexible n-type vacuum-processed metal oxide semiconductor TFTs. Each line includes the best performance parameter ever reported (highlighted in **bold**).

	Mobility ($cm^2\ V^{-1}\ s^{-1}$)	Threshold voltage (V)	Sub-threshold swing (mV/dec)	Current on/off ratio	Transit frequency (MHz)	Channel length (μm)	Substrate thickness (μm)	Bending radius (mm)	Strain (%)	Bending cycles
IGZO TFT with stacked titanium oxide gate dielectric[154]	**76**	0.5	129	1×10^3	…	32	….	15	0.43	…
DG IGZO TFT[90]	8.5	0.95	**69**	2×10^9	…	10	50	5	0.55	…
BG IGZO TFT[84]	15.3	1	126	$\mathbf{2 \times 10^{10}}$	…	60	50	1.9	1.4	1
SA IGZO TFT[114]	7.5	0	130	2×10^9	**135**	0.5	50	3.5	0.72	1
Quasi-vertical IGZO TFT[145]	0.2	1.5	400	1×10^4	1.5	**0.3**	50	5	0.48	1
IGZO TFT on mechanically active substrate[23]	17	0.6	165	…	…	15	**0.7**	**0.025**	…	1
IGZO TFT with hybrid buffer layer[202]	15.5	4.1	200	5×10^9	…	…	125	3.3	**1.89**	10.000
IGZO TFT on island structures[137]	14	…	…	1×10^7	…	4	17	1	…	**100.000**

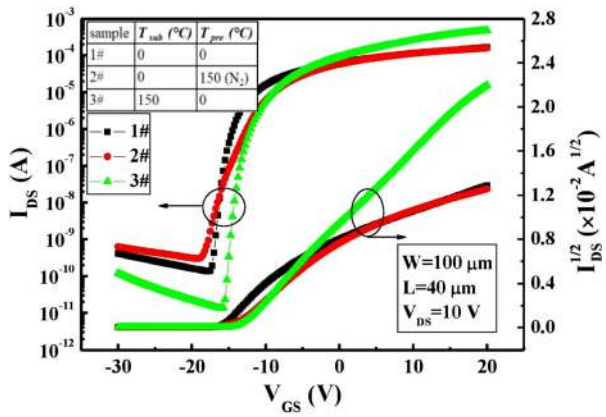

FIG. 14. Transfer characteristics of flexible IGZO TFTs fabricated without annealing (1#), with post annealing at 150 °C (2#), and with IGZO deposited at 150 °C (3#). Reproduced with permission from Xiao *et al.*, in *12th IEEE Int. Conf. on Solid-State Integr. Circuit Technol.* (*ICSICT*) (2014), pp. 1–3. Copyright 2014 Institute of Electrical and Electronic Engineers.

sputtering of IGZO at 150 °C results in slightly higher μ_{FE} compared with untreated or post-annealed (at 150 °C) TFTs.

Nevertheless, while increased temperatures definitely improve the performance[168] and the stability of single TFTs,[153,160] there is no clear trend showing that annealed TFTs always exhibit better performance (e.g., higher μ_{FE}) than non-annealed one. One explanation could be the fact that TFTs are often exposed to an indirect annealing at elevated temperatures during the fabrication process (e.g., during the deposition of passivation layers at high temperatures around 150 °C).[113,179] The same trend also applies for room temperature fabricated devices with unspecified temperatures employed during the photolithographic steps.[29,77,154,181,188] Even TFTs fabricated by shadow masking by Erb *et al.* with at least two elevated temperature steps during and after the IGZO deposition resulted in reasonable μ_{SAT} and I_{ON}/I_{OFF} of 4.6 $cm^2\ V^{-1}\ s^{-1}$ and 1×10^5, respectively.[162] A more uncommon approach was used by Park *et al.*, who significantly increased the μ_{FE} of ZnO TFTs (from 0.2 $cm^2\ V^{-1}\ s^{-1}$ to 1.5 $cm^2\ V^{-1}\ s^{-1}$) by using microwave annealing at a frequency of 2.45 GHz and a power of 700 W for 15 min.[178]

(II) Another effective way to improve the TFT performance and stability is the optimization of the semiconductor that can be realized by adjusting the oxygen content in the sputter atmosphere and/or employing dual-layer semiconductors. Flexible GZO TFTs, for example, exhibit an optimized current on/off ratio if an O_2 content of 25% is used during the semiconductor deposition.[188] A study by Nag *et al.* showed how TFTs with dual-layers of IGZO with different thicknesses and different amounts of O_2 allow precisely controlling the charge carrier density.[41] In this case, it was demonstrated that TFTs with dual-layers (7 nm IGZO with 0% O_2/15 nm IGZO with 5% O_2) result in enhanced performance, if compared with devices with 20 nm single-layer of IGZO.[41] At the same time, if compared with single-layer TFTs, dual-layer IGZO devices exhibit also improved stability, as displayed in Fig. 15.[41] Dual-layers of IZO deposited in gradient O_2 ambient have been used to fabricate semiconducting (4% or 7% O_2) and low resistance IZO layers (0% O_2).[184] The resulting flexible TFTs (Fig. 16) show a strong dependency of the μ_{FE} and V_{TH} on the sputtering conditions. Finally, Marrs *et al.* demonstrated flexible dual-layer TFTs (with IGZO at the interface with the dielectric and with highly doped IZO close to the source/drain contacts) yielding improved stability and effective mobility.[173]

(III) Also, the choice of the gate dielectric plays a key role in the TFT optimization, by directly influencing the specific gate dielectric capacitance (and therefore also the drain current and the sub-threshold swing) of the device. One possibility to improve C_{ox} is the use of multi-layer gate dielectrics with good interface quality, such as HfO_2/TiO_2, PVP/TiO_2, SiO_2/SiN_x, and $HfO_2/TiO_2/HfO_2$.[144,152,154,157] Another approach to increase the C_{ox} while keeping the advantageous interface properties of Al_2O_3 is the use of thin (10 nm) Al_2O_3 grown by ALD.[90] Additionally, ferroelectric gate dielectrics, either P(VDF-TrFE),[149,167] Al_2O_3 in combination with chicken albumen[204] (see Fig. 8), or Al_2O_3/P(VDF-TrFE) stacks,[146] can be used to generate a gate hysteresis of up to several volts in the TFT transfer characteristics. Fig. 17 displays the

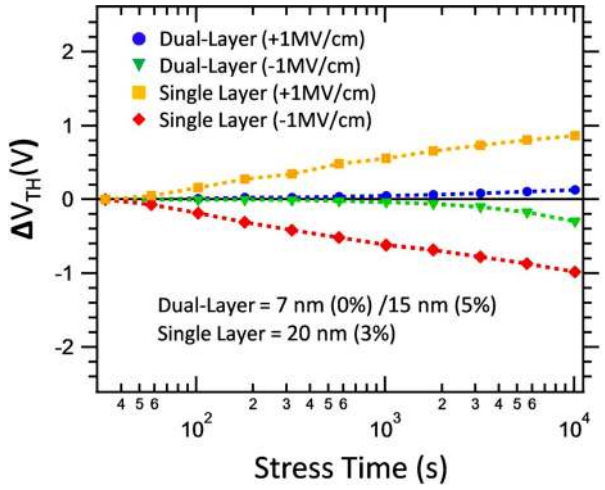

FIG. 15. Threshold voltage shift (ΔV_{TH}) caused by positive and negative gate bias stress for TFTs with a single-layer [20 nm in 3% oxygen (O_2)] or dual-layer (7 nm in 0% O_2/15 nm in 5% O_2) IGZO semiconductor (W/L = 140 μm/5 μm). Reproduced with permission from Nag *et al.*, J. Soc. Inf. Disp. **21**, 129 (2013). Copyright 2013 John Wiley and Sons.

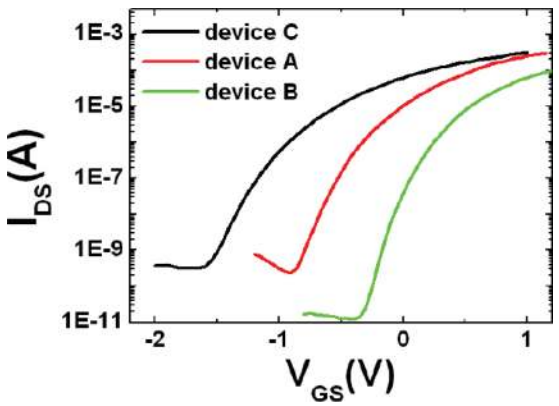

FIG. 16. Transfer characteristics of TFTs with different indium zinc oxide (IZO) active layers: device A (30 nm IZO in 4% O_2 + 30 nm IZO in gradually decreasing O_2 ambient), device B (30 nm IZO in 7% O_2 + 30 nm IZO in gradually decreasing O_2 ambient), and device C (30 nm IZO in pure Ar ambient). Reproduced with permission from Zhou *et al.*, IEEE Electron Device Lett. **34**, 888 (2013). Copyright 2013 Institute of Electrical and Electronic Engineers.

transfer curve of a flexible IGZO TFT with Al_2O_3/P(VDF-TrFE) gate dielectric, showing how the gate hysteresis allows realizing a non-volatile 1-bit memory element.[146]

(IV) The use of a suitable passivation layer can lead to TFTs with enhanced stability, as well as performance. A direct comparison of TFTs with and without a TiO_2 passivation layer has been reported by Hsu *et al.*[157] Hsu *et al.* showed that a TiO_2 capping layer on BG IGZO TFTs increases the μ_{FE} from 10 cm^2 V^{-1} s^{-1} to 61 cm^2 V^{-1} s^{-1}. Such improvement has been attributed to the larger electron accumulation caused by the higher electric field under the high-ϵ_R TiO_2 capping layer.

(V) Even if the barrier layer has no direct impact on the TFT performance, its barrier and surface properties can influence the final device. TFTs with SiO_2, SiN_x, or SiN_x in combination with AlO_x (10 nm or 100 nm) buffer layer have been compared by Ok *et al.*[155] In their work, Ok *et al.* showed that SiN_x/AlO_x dual-layer barriers yield better water and hydrogen diffusion barriers and therefore improved device performance, if compared with TFT with single buffer layers (SiN_x or SiO_2).[155] Similarly, flexible IGZO TFTs fabricated on PEN using 3 μm organic TR-8857-SA7 + 50 nm Al_2O_3 dual-layer result in superior performance compared with those manufactured on PET with a single 3 μm thick TR-8857-SA7 layer or without buffer layer.[202]

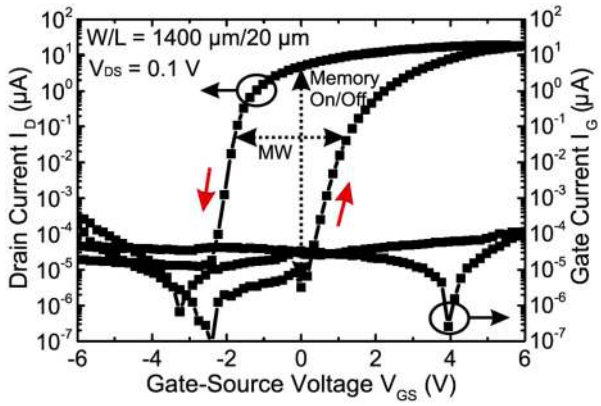

FIG. 17. Hysteretic transfer characteristic of a flexible IGZO TFT with an Al_2O_3/poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] multilayer hybrid gate dielectric. Reproduced with permission from Petti *et al.*, IEEE Trans. Electron Devices **61**, 1085 (2014). Copyright 2014 Institute of Electrical and Electronic Engineers.

(VI) Finally, the device geometry can be adjusted to achieve significant improvements in the electrical performance. First, it is worth mentioning that BG TFTs (Figs. 4(a) and 4(b)) provide a generally better performance if compared with TG devices (Figs. 4(c) and 4(d)). Indeed, the average μ_{FE} of all the flexible n-type vacuum metal oxide semiconductor BG TFTs cited in this subsection is 16.6 cm^2 V^{-1} s^{-1}, while the corresponding value for TG devices is only 12.7 cm^2 V^{-1} s^{-1}. Although this comparison is not entirely valid since the values are not normalized for the different channel materials, these two average numbers highlight the better interface quality of BG TFTs, compared with TG ones. On the other side, DG architectures (Fig. 4(e)) exhibit by a factor of ≈2 larger effective gate area,[90,106] which results in a total gate capacitance increased by the same factor, as shown in Fig. 18.

The increased gate capacitance C_G leads to a larger transconductance g_m, as demonstrated in Fig. 18(b), where flexible DG and BG IGZO TFTs are compared. Since g_m and C_G increase simultaneously, there is no significant effect on the TFT AC performance (see Equation (1.8)).[106] Nevertheless, DG structures also influence the threshold voltage, and the increased C_G enabled the smallest published SS of 69 mV/dec.[90] DG architectures present also an increased effective gate to source/drain overlap and hence reduced R_C from

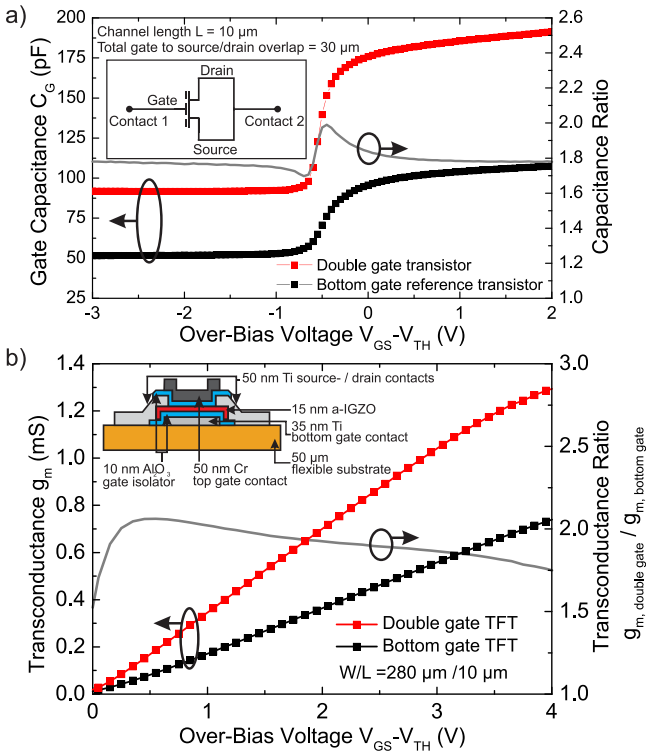

FIG. 18. Flexible DG IGZO TFTs: (a) total gate capacitance (C_G), and ratio between the C_G of a DG TFT and the corresponding BG reference TFT and (b) transconductance (g_m) of DG and BG TFTs for different values of the over-bias voltage (V_{GS}-V_{TH}). The insets in (a) and (b) show the measurement setup and the DG device cross-section, respectively. Reproduced with permission from Münzenrieder *et al.*, Solid-State Electron. **84**, 198 (2013). Copyright 2013 Elsevier.

205 kΩ μm to 165 kΩ μm (if compared with the corresponding BG TFT reference structures).[106] Furthermore, the μ_{FE} of DG TFTs can be either reduced (because of more interface scattering caused by additional process steps, and therefore less clean interfaces) or increased (because of less interface scattering caused by the reduced lateral electric field) if compared with the corresponding BG TFTs.[106] Which of these effects is dominant varies across literature. To realize fast and flexible TFTs, devices with small feature sizes (especially short channel lengths) need to be fabricated. Since the realization of short channels on flexible substrates can be challenging, two alternative concepts based on vertical device geometries have been developed: flexible metal oxide semiconductor VTFTs (Fig. 4(f))[92,93,96] and QVTFTs.[145] Both device structures are characterized by the fact that the channel is oriented out of the plane with respect to the substrate.[145] This is realized by depositing an insulating layer between the source and the drain contacts (the so called spacer), whose thickness defines the channel length. Thereby, channels as short as 300 nm are possible.[145] Unfortunately, VTFTs and QVTFTs often suffer from a bad interface quality, a high contact resistance, and a large overlap capacitance.[92,145] Therefore, only transit frequencies below 1.5 MHz have been possible with such vertical structures.[92,145] Nevertheless, VTFTs have great potential for applications where a small footprint is required. Flexible n-type vacuum-processed metal oxide semiconductor TFTs with both short channels and small overlap capacitance have been manufactured using self-alignment techniques. In particular, flexible

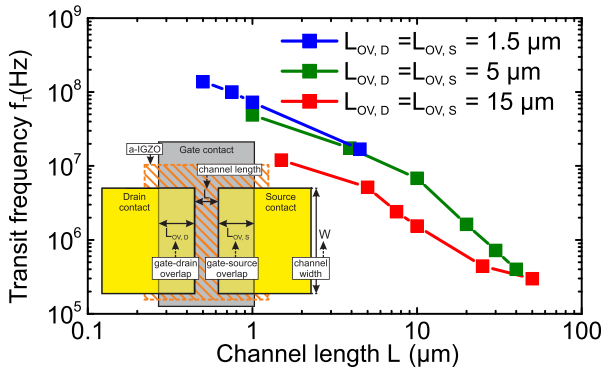

FIG. 19. Transit frequency f_T of flexible IGZO TFTs with different values of channel length (L) and total overlap length between gate and source/drain (L_{OV}) fabricated by conventional (L_{OV} of 15 μm and 5 μm) and self-aligned (L_{OV} of 1.5 μm) lithography. The inset displays the geometrical parameters. Reproduced with permission from Appl. Phys. Lett. **105**, 263504 (2014). Copyright 2014 AIP Publishing LLC. Reproduced with permission from Münzenrieder *et al.*, IEEE Trans. Electron Devices **60**, 1 (2013). Copyright 2013 Institute of Electrical and Electronic Engineers.

self-aligned IGZO TFTs (L = 500 nm and $L_{OV,S} = L_{OV,D} = L_{OV}$ = 1.55 μm) have enabled the realization of the highest f_T of 135 MHz (see Fig. 13) ever reported for flexible metal oxide semiconductor devices.[114,209] The same self-alignment approach has been also used to fabricate flexible DG IGZO TFTs with two self-aligned gates (L = 7.5 μm and L_{OV} = 1 μm), yielding an f_T of 5.6 MHz.[106] The influence of the channel scaling, together with the use of different source/drain to gate overlaps, is shown in Fig. 19. The graph displays the transit frequency (extracted from S-parameter measurements) of flexible IGZO TFTs fabricated with conventional lithography (L_{OV} of 15 μm and 5 μm) and self-alignment (L_{OV} = 1.5 μm). The positive effect of the reduced device dimensions is evident. At the same time, Fig. 20 shows how the overlap length-dependent contact resistance of TFTs limits the impact of further channel scaling on the device f_T. Therefore, significantly higher frequency values call for a reduction of the specific contact resistance.[209]

b. Modeling. Besides the optimization of the electrical properties itself, it is also important to model the TFT behavior prior to the fabrication.

Device modeling is not only essential for the design and simulation of complete circuits but it also allows predicting the influence of TFT scaling, as well as of any device layout modification. Flexible IGZO TFTs have been modeled using I-V data measurements and artificial neural networks (ANNs), such as multi-layer perceptron (MLP), radial basis functions (RBFs), and least squares-support vector machine (LS-SVM).[211] Among these ANN approaches, MLP seems to be the most suitable methodology since it provides the best trade-off between accuracy and complexity.[211] Nevertheless, these ANN-based techniques have only been used to simulate the static and quasi-static behavior of TFTs with L ≥ 10 μm.[211] One possibility to simulate both DC and AC performance of TFTs with channel lengths down to 6 μm was presented by Zysset *et al.*, who proposed a level 61 HSpice model (AIM Spice level 15 model).[212] The drawback of the model presented by Zysset *et al.* is that no testing on

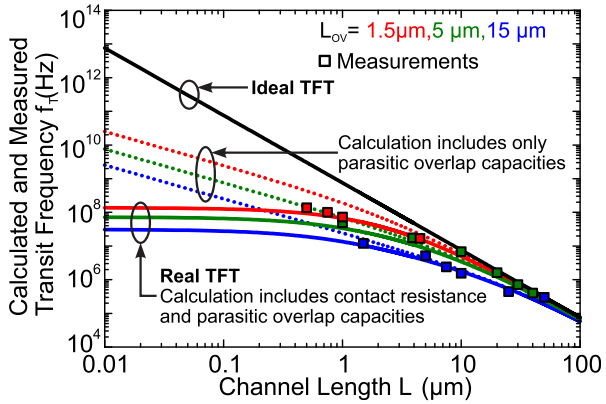

FIG. 20. Channel and overlap length-dependent calculation of the transit frequency of flexible IGZO TFTs (verified by S-parameter measurements): the calculation for a real TFT includes the influence of the parasitic overlap capacitance (C_{OV}) and the contact resistance (R_C), as compared with the ideal case (no C_{OV} and R_C considered). The extrapolation to short channel lengths shows the dominant influence of contact resistance on the TFT transit frequency. Reproduced with permission from Appl. Phys. Lett. **105**, 263504 (2014). Copyright 2014 AIP Publishing LLC.

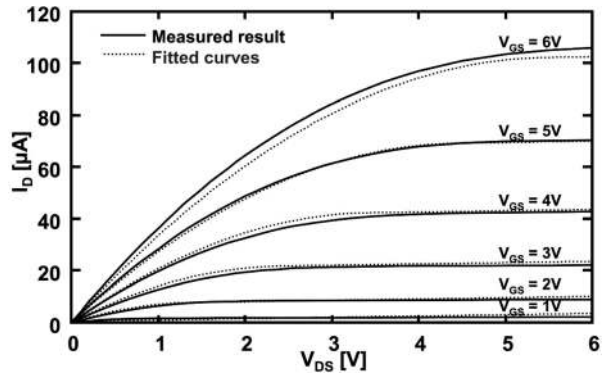

FIG. 21. Flexible IGZO TFTs: measured output characteristic (average of four TFTs with W/L = 50 μm/50 μm) and corresponding curve simulated with a HSpice level 3 model. Reproduced with permission from Perumal *et al.*, IEEE Electron Device Lett. **34**, 1391 (2013). Copyright 2013 Institute of Electrical and Electronic Engineers.

the channel scaling has been provided. A more complete model was presented by Perumal *et al.*, who reported the simulation of flexible IGZO TFTs based on a level 3 HSpice template.[213] Fig. 21 demonstrates the successful simulation of the TFT DC performance parameters. Additionally, also the AC performance parameters, including the S-parameters of flexible IGZO TFTs, have been simulated.[213] Finally, an analytical model including also the contact resistance and the gate dielectric capacitance of flexible IGZO TFTs has been reported.[106] This model has been used to analyze the influence of scaling (channel and overlap length) on the TFT transit frequency (see Fig. 20), allowing also a prediction on the scalability of current flexible IGZO TFT technology. In this model, flexible TFTs with channels as short as 0.5 μm have been simulated.[106]

4. Mechanical properties

A complete set of performance parameters of flexible TFTs cannot be limited to the electrical characteristics but needs to deal also with the mechanical properties. To fully describe the mechanical properties of flexible n-type vacuum-processed metal oxide semiconductor TFTs, issues like induced strain, maximum strain resistance, influence of strain on the electrical properties, as well as role of mechanical fatigue need to be thoroughly addressed.

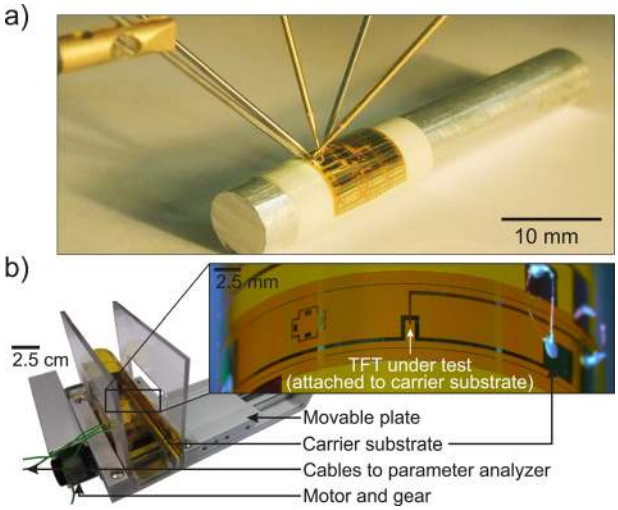

FIG. 22. (a) Flexible TFT substrate attached to a metallic rod using double-sided tape and contacted with standard probe tips. Reproduced with permission from Münzenrieder *et al.*, IEEE Trans. Electron Devices **59**, 2153 (2012). Copyright 2012 Institute of Electrical and Electronic Engineers. (b) Automated custom-built bending tester with a mounted flexible device; in this case, the TFT is permanently connected to a parameter analyzer. Reproduced with permission from Münzenrieder *et al.*, in *Proc. of Eur. Solid-State Device Res. Conf.* (*ESSDERC*) (2013), pp. 362–365. Copyright 2013 Institute of Electrical and Electronic Engineers.

a. Bendability. Bending is the most common technique employed to induce strain in flexible TFTs. This is mainly because bent thin-film devices enable many applications such as rollable displays, smart labels, seamless and embedded patch-like systems, electronic textiles, and implantable electronic devices for medical equipment. While rollable displays, smart labels, as well as embedded patch-like systems can be realized using flexible TFTs with minimum bending radii in the centimeter range, smart electronic textiles call for much smaller radii in the sub-millimeter regime.[214] On the other side, medical applications need thin-film devices that can adapt to the human body, e.g., to a human hair which exhibits a radius of ≈50 μm. Flexible n-type vacuum-processed metal oxide semiconductor TFTs, especially based on IGZO active layers, bent to different radii have been characterized by many research groups.[39,80,96,132–135,139,152–161,179–181,184,204,208,215] As illustrated in Fig. 22(a), mechanical bending tests are, in general, performed by winding the flexible TFTs substrate around cylindrical rods. At the same time, some research groups have also developed automated bending testers like the one shown in Fig. 22(b), which can be used to perform multiple bending and re-flattening cycles,[133,137,139,152,153,161,179,215] as well as to characterize the TFTs at arbitrary bending radii while the devices are connected to a parameter analyzer.[150] The approach based on the bending tester allows carefully controlling the applied strain during the entire measurement and in some cases also ensures a permanent and reliable contact between the TFTs and the characterization equipment.

Independently of the measurement setup, flexible n-type vacuum-processed metal oxide semiconductor TFTs can be bent down to 50 μm in the case of tensile (outward) bending[80] and down to 25 μm for compressive (inward) bending.[23] Nevertheless, it has to be mentioned that because of difficulties in contacting the devices while being inward bent, bending in compressive direction is not very common. As visible from Table II, the maximum strain values do not only depend on the minimum bending radii, but also on the device layers and thicknesses. Since the calculation of the mechanical strain in a multilayer system can be complex, different equations have been used to estimate numerical values of the strain induced by bending. One of the most common approximation is the following:[216]

$$\epsilon = \left(\frac{1}{R} \pm \frac{1}{R_0}\right) \times \frac{t_S + t_D}{2} \times \frac{\frac{Y_D}{Y_S}\left(\frac{t_D}{t_S}\right)^2 + 2\frac{Y_D}{Y_S}\frac{t_D}{t_S} + 1}{\frac{Y_D}{Y_S}\left(\frac{t_D}{t_S}\right)^2 + \frac{Y_D}{Y_S}\frac{t_D}{t_S} + \frac{t_D}{t_S} + 1}, \tag{2.1}$$

where R is the bending radius, R_0 is the initial bending radius caused by the built-in strain (has to be added if the built-in strain is in the opposite direction as the induced strain, elsewhere subtracted), t_D and t_D are, respectively, the thicknesses of the substrate and of the device, and Y_S and Y_D are the Young's moduli of the substrate and the device, respectively. The highest strain values at which flexible n-type vacuum-processed metal oxide semiconductor TFTs have been able to operate include 1.89%,[139,202] (tensile direction) and −0.6% (compressive direction).[146] In addition to one-time bending tests, also the TFT resistance to mechanical fatigue caused by repeated bending and re-flattening cycles has been investigated. In particular, tensile bending cycles up to 100.000 have been reported,[137,152] while repeated compressive bending tests have been limited to 24 cycles.[151] While the majority of the published bending measurements have only confirmed the functionality of the devices at a given bending radius or after repeated bending cycles, other more sophisticated experiments have focused on the influence of strain on the electrical TFT performance. In the majority of the cases (for IGZO TFTs), bending results in a increase of the drain current under tensile bending and in a decrease of the drain current under compressive strain. At typical tensile strain of ≈0.5%, the I_D changes are caused by an increase of the μ_{FE} by ≈2.5% and by a decrease of the V_{TH} by ≈20–200 mV. At the same time, compressive strain of ≈0.5% causes μ_{FE} and V_{TH} changes around ≈ −2% and ≈10–150 mV, respectively.[84,90,144,148,150,151,156,172] The opposing effect of tensile and compressive bending on the DC performance of flexible IGZO TFTs is visualized in Fig. 23. Furthermore, also the influence of repeated cycles of bending and re-flattening on the characteristics of flexible IGZO TFTs (measured while flat) has been analyzed.[151] The effect of long-term bending depends on the repetition duration.[151] Nevertheless, bending cycles nearly always lead to a decreased I_D, probably due to the formation of micro-cracks on a short time scale (already after 24 bending cycles).[151] However, also cyclic tensile/compressive bending results in

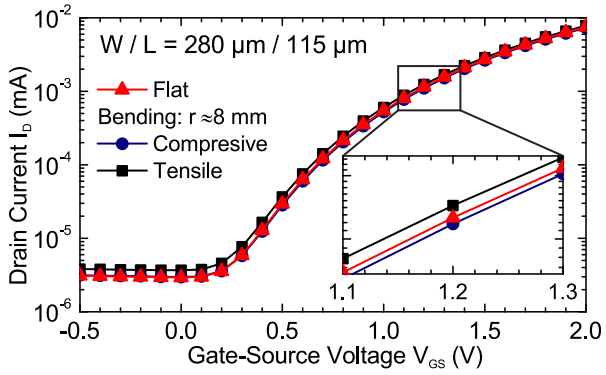

FIG. 23. Transfer characteristic of a flexible IGZO TFT measured while flat and subsequently bent in tensile and compressive direction. The inset displays an enlargement on the strain-induced shifts. Reproduced with permission from Münzenrieder *et al.*, IEEE Trans. Electron Devices **58**, 2041 (2011). Copyright 2011 Institute of Electrical and Electronic Engineers.

parameter shifts similar to those observed for tensile/compressive one-time tests (see Fig. 23).[143,151,152,179] The observed threshold voltage and mobility shifts induced in flexible IGZO TFTs under tensile/compressive bending have been explained by an increase/decrease of the carrier density caused either by the creation of oxygen vacancies[160] or by a change of the electronic structure.[151] These effects (together with the above mentioned values) are only valid if the IGZO TFTs are bent within the mechanically elastic region, whereas bending to smaller radii induces cracks that cause permanent parameter shifts or even device failure.[84,143,152,182] At the same time, it has to be mentioned that other groups have also observed no effect or even an opposing influence of mechanical bending.[149,180,181] These partially contradictory observations (concerning both the direction and the magnitude of strain-induced changes) can be explained by a number of additional factors that need to be considered:

(I) Illumination can have a significant effect on bending measurements. Even if the illumination condition is not reported in the majority of the published bending experiments, it is important to take into account the combined light-strain effect, especially for the fabrication of flexible optical displays. A direct comparison of flexible IGZO TFTs bent while in darkness and under illumination is shown in Fig. 24. Without illumination, the μ_{FE} and V_{TH} change by +3.1% (−1.8%) and −15 mV (+19 mV), respectively, under tensile (compressive) strain ϵ of ≈±0.3%.[151] Under an illumination of 90 lx, the μ_{FE} varies by +14.8% (−3.7%) and the V_{TH} changes by −110 mV (+37 mV) under tensile (compressive) bending.[151] Additionally, also the relaxation behavior is different: a full recovery of the parameters is possible only if the devices are bent in darkness.[151] It is important to underline that illumination only influences the magnitude of the measured parameter shifts, whereas the sign depends on the direction of bending (tensile or compressive). Additionally, Park *et al.* have recently reported a similar study on the combined effect of mechanical bending, illumination, and bias stress in flexible IGZO TFTs.[135]

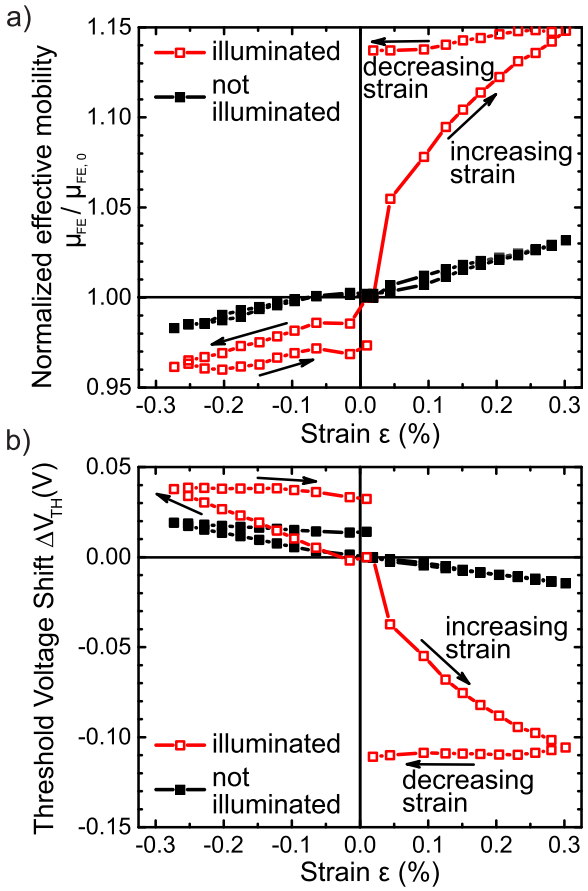

FIG. 24. Saturation field-effect mobility (μ_{FE}) variation (a) and threshold voltage variation (ΔV_{TH}) (b) of flexible IGZO TFTs for tensile and compressive strain (ϵ): $\epsilon > 0$ and $\epsilon < 0$, respectively. The TFTs are either measured in darkness or while illuminated. Reproduced with permission from Münzenrieder *et al.*, IEEE Trans. Electron Devices **58**, 2041 (2011). Copyright 2011 Institute of Electrical and Electronic Engineers.

(II) In short-channel TFTs ($L \lesssim 5\ \mu m$), the channel resistance (R_{CH}) can become comparable to the contact resistance, as well as to the resistance of the interconnection lines. Therefore, also the strain sensitivity of the, generally metallic, contacts (and not only of the metal oxide semiconductor) can influence the response of the TFTs under applied mechanical bending.[113]

(III) Device encapsulation can move the neutral bending axis above the TFT layers, leading to an effective compressive strain induced even if tensile bending is applied.[140] A similar effect can also occur if the strain built-in in the device layers is larger than the strain induced by bending.[90,151] In both cases, strain-induced parameter shifts with an opposite algebraic sign are observed.

(IV) The geometry of the TFTs can also influence their strain sensitivity. While BG and TG IGZO TFTs, in general, exhibit the parameter shifts described above, DG IGZO TFTs show exactly the opposite behavior.[209] A direct comparison of flexible BG and DG IGZO TFTs bent in tensile direction resulted in a μ_{FE} and V_{TH} shift of +2% and −75 mV for BG TFTs, but in shifts of −7% and +25 mV in the DG case, respectively.[90] Similarly, IGZO VTFTs exhibit μ_{FE} and V_{TH} shift between −2% and −5% and +100 mV and +130 mV while strained by +0.5%.[92,145] Here, the Poisson effect leads to the fact that tensile bending results in compressive strain in the device channel.

(V) The influence of repeated bending cycles combined with the specific relaxation behavior causes a time sensitivity of the TFTs during bending experiments. At the same time, different groups also use diverse time scales to apply mechanical bending, with time differences spanning to up to 1 h.[158]

(VI) Furthermore, extensive bending beyond a certain strain value (which delimits the elastic with the inelastic region) can lead to the formation of microcracks in different material layers.[84,143] These cracks can be hardly visible and do not necessarily result in device failure. Nevertheless, TFTs with microcracked layers can present different device parts disconnected from each other and therefore exhibit a reduced W/L ratio, as well as a worst electrostatic control over the channel. In these cases, a decrease of the I_D together with an increase of the I_{OFF} (under both tensile and compressive bending) is observed.

(VII) Finally, the influence of the electrical stress induced by measuring the devices repeatedly during the bending tests needs also to be taken into account. On one hand, it has been reported that the parameter variations caused by mechanical stress (especially cyclic bending) are in the same order of magnitude as the shifts caused be electrical stress (standard gate bias stress measurements).[151] On the other hand, gate bias stress (positive and negative) induces basically the same shifts, regardless if IGZO TFTs are strained, bent to different tensile radii (down to 40 mm),[160] or cycled between flat (radius of 15 mm) and bent state for up to 10.000 repetitions.[155]

Also, the influence of bending on the AC performance of flexible IGZO TFTs has been analyzed.[113,114] The AC performance, in particular, the f_T, is mainly determined by the transconductance g_m and the gate capacitance C_G of the TFTs (see Equation (1.8)). On one side, g_m increases under tensile bending due to the increased μ_{FE} and decreased V_{TH}. On the other side, tensile bending also increases the C_G (typically by 1%–2% for 0.5%–1% tensile strain), due to an increased area, decreased t_{ox}, and increased carrier density under bending. Due to the simultaneous increase of g_m and C_G, the transit frequency remains basically unchanged.

Additionally, it is also important to predict and simulate the strain sensitivity of TFT (as well as circuits) prior to fabrication, in order to optimize the devices and reduce the strain-induced performance variations as much as possible. One step in this direction was done by Ma *et al.*,[217] who included strain-induced μ_{FE} variations into a HSpice-based flexible circuit analyzer. Furthermore, purely mechanical simulations of flexible n-type vacuum-processed metal oxide semiconductor TFTs have also been reported. In particular, COMSOL multiphysics has been used to model strain-stress

curves, as well as von Mises stress induced by tensile, compressive, and torsional forces.[218] Based on these mechanical models, IGZO and graphene active layers show similar performance. Moreover, also device failure due to crack formation has been predicted by a finite element method (FEM). The FEM simulations have been used for flexible IGZO TFTs to identify device areas prone to stress localization under tensile and compressive bending[219] or simulate the strain of a PVP/Al_2O_3 hybrid gate dielectric.[152] Finally, the mechanical stress induced in IGZO TFTs roll-transferred onto a flexible PDMS substrate has also been calculated by Sharma *et al.*[205]

b. Improvement of bendability. As already mentioned, sub-millimeter bending radii are necessary for many novel applications (e.g., smart textiles and implantable and imperceptible medical devices). While TFTs bending radii of several millimeters or even centimeters can be obtained easily,[106,134,135,145,147,152,153,155–158,160,161,178,179,204,208] smaller curvatures are more complicated to be achieved.[23,80,96,140] There are two main approaches to enhance the device bendability: either improving the TFT flexibility or reducing the mechanical strain induced by bending. In particular, the TFT flexibility can be enhanced with the following techniques:

(I) The most obvious way is to increase the ductility of the different device layers. An investigation of flexible IGZO TFTs with different metals used as BG (see Fig. 10) showed that the device bendability scales with the ductility of the gate. Flexible IGZO TFTs using Cr (thin film rupture strain $\epsilon_r \approx 0.5\%$), Ti ($\epsilon_r \approx 2\%$), Pt ($\epsilon_r \approx 4\%$), or Cu ($\epsilon_r \approx 4.5\%$) BG exhibit average bendabilities of 4.2 mm, 2.4 mm, 2.2 mm, and 1.9 mm radii, respectively.[84]

(II) Another promising approach consists of replacing the brittle ceramic gate dielectrics (e.g., Al_2O_3) with more ductile polymers. For example, P(VDF-TrFE) can be used without additional insulating layers and results in TFTs with good electrical and mechanical performance.[149] The use of PVP in combination with 20 nm, 30 nm, or 40 nm thick Al_2O_3 confirmed that 40 nm thick Al_2O_3 yields a reduced mechanical stability.[152] It is also worth mentioning that a comparison of TG TFTs with 25 nm Al_2O_3 or 100 nm P(VDF-TrFE) in combination with 10 nm Al_2O_3 resulted in an increase of the minimum bending radius from 4 mm to 4.7 mm.[146] Therefore, the gain in ductility offered by polymeric dielectrics has to be compared with the increase in thickness and therefore strain (see Equation (2.1)) of the entire device stack.

(III) Although all the n-type vacuum-processed metal oxide semiconductors employed for flexible TFTs have a similar chemical composition, their mechanical properties can vary significantly. If amorphous IGZO TFTs are compared with nano-crystalline ZnO TFTs (Fig. 25), the flexible IGZO devices exhibit considerably higher bendability (≈5 mm instead of ≈15 mm).[183] The worst bendability of ZnO can be explained by its piezoelectric properties, which lead to the creation of an electric field under the applied strain. The so-formed electric field can subsequently significantly influence the TFT performance. Furthermore, the grain boundaries in ZnO can act as nucleation points for micro-cracks.

(IV) Also, the source/drain materials can influence the TFT mechanical properties. A study by Chien *et al.* reported that IGZO TFTs with IZO/Ti source/drain contacts yield better electrical performance and are less sensitive to mechanical bending (down to 3 mm) if compared with devices with only Ti electrodes.[142]

(V) The ductility of flexible IGZO TFTs can also be increased by reducing the device area, and thereby the number of micro-cracks induced by repeated cycles of bending and re-flattening cycles.[161]

(VI) Another way to increase the TFT ductility can be achieved by aligning the devices relative to the strain. Fig. 26 shows that bending parallel to the IGZO TFT channel increases the carrier mobility until the devices are destroyed above $\epsilon \approx 0.7\%$.[143] Perpendicular bending only slightly increases the μ_{FE} for small strain values ($\epsilon \approx 0.3\%$) but leads to a strong μ_{FE} degradation if the strain is further increased. The higher sensitivity of TFTs to perpendicular bending (compared with parallel) is caused by a significantly higher cracking probability in this direction (remember that generally $W > L$).[143] This is also confirmed by Hong, Mativenga, and Jang, who reported flexible IGZO TFTs with $L > W$ showing a reduced cracking formation for cyclic bending in the perpendicular direction.[161] A similar experiment performed with ZnO TFTs showed no significant difference for parallel and perpendicular cyclic bending,[179] which can be probably explained by the low strain values always $\leq 0.07\%$.

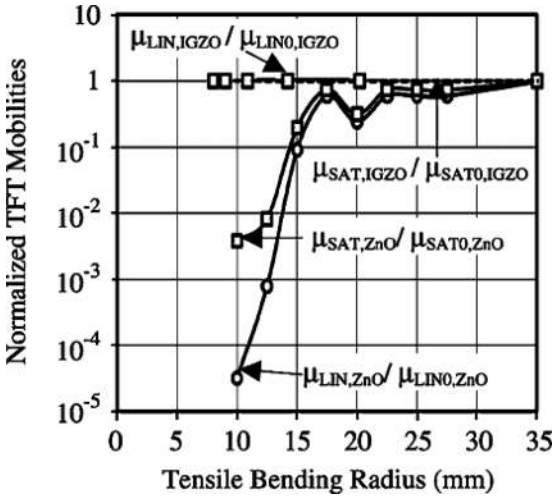

FIG. 25. Evolution of the linear (μ_{LIN}) and saturation (μ_{SAT}) mobilities of flexible IGZO and zinc oxide (ZnO) TFTs under tensile bending. Reproduced with permission from Cherenack *et al.*, IEEE Electron Device Lett. **31**, 1254 (2010). Copyright 2010 Institute of Electrical and Electronic Engineers.

Alternatively, the strain induced by bending can be reduced using the following techniques:

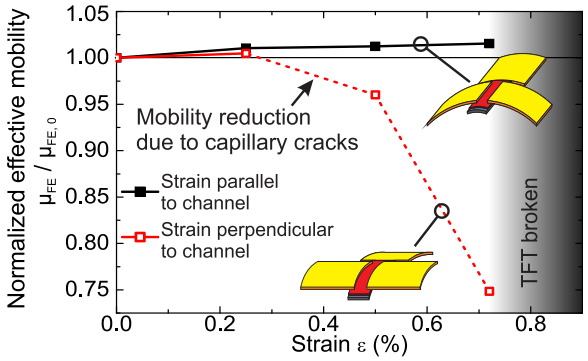

FIG. 26. Influence of bending parallel and perpendicular to the channel (and therefore to the current flow) in flexible IGZO TFTs. Parallel bending increases μ_{FE} until the TFT is permanently destroyed at $\epsilon \approx 0.7\%$. Perpendicular bending increases μ_{FE} for $\epsilon \lesssim 0.3\%$ but results in a strong μ_{FE} degradation if the strain is further increased. Reproduced with permission from Münzenrieder *et al.*, IEEE Trans. Electron Devices **59**, 2153 (2012). Copyright 2012 Institute of Electrical and Electronic Engineers.

(I) The strain induced by bending is inversely proportional to the bending radius and approximately proportional to substrate thickness (see Equation (2.1)). Given the same maximum strain (TFT strain resistance), thinner substrates directly lead to smaller bending radii. Although thin substrates can be difficult to handle and require more complicated fabrication processes, n-type vacuum-processed metal oxide semiconductor TFTs manufactured on a 0.7 μm thick hydrogel/PI hybrid substrate,[23] 1 μm thick parylene,[80,141] 5 μm thick glass,[179] and 15 μm thick PI[161] have been reported. Fig. 27 shows a flexible IGZO TFTs fabricated on a 1 μm thick parylene membrane while wrapped around a human hair (radius of 50 μm). Due to the thin substrate, the devices are fully operational at 50 μm tensile bending radius, which corresponds to a strain of ≈0.4%.[80]

(II) It is also possible to reduce the strain induced in the TFTs by placing the devices in their neutral strain axis thanks to the use of a suitable encapsulation layer. The bending performance of flexible IGZO TFTs fabricated on a 50 μm thick PI substrate and encapsulated with an additional 50 μm thick structured PI foil (+5 μm epoxy glue) is shown in Fig. 28.

By encapsulating the devices, a reduction of the minimum bending radius from ≈4 mm to 0.125 mm was possible.[140] Additionally, Park *et al.* fabricated TFTs on 17 μm thick PI and encapsulated them between layers of PET, which enabled the bending radii down to 1 mm.[137] Here, different distances between the TFTs and the neutral strain axis (caused by different encapsulation layer thicknesses) have been investigated. It was confirmed that the TFTs placed on the neutral strain axis exhibit smaller performance parameter shifts that TFTs placed up to 50 μm away from the neutral strain axis. The drawback of this method is that the additional encapsulation layer (with similar thickness as the substrate) increases also the total stiffness of the final device. At the same time, an encapsulation is anyway necessary in order to increase the robustness of the final device for applications like flexible displays.[39,40]

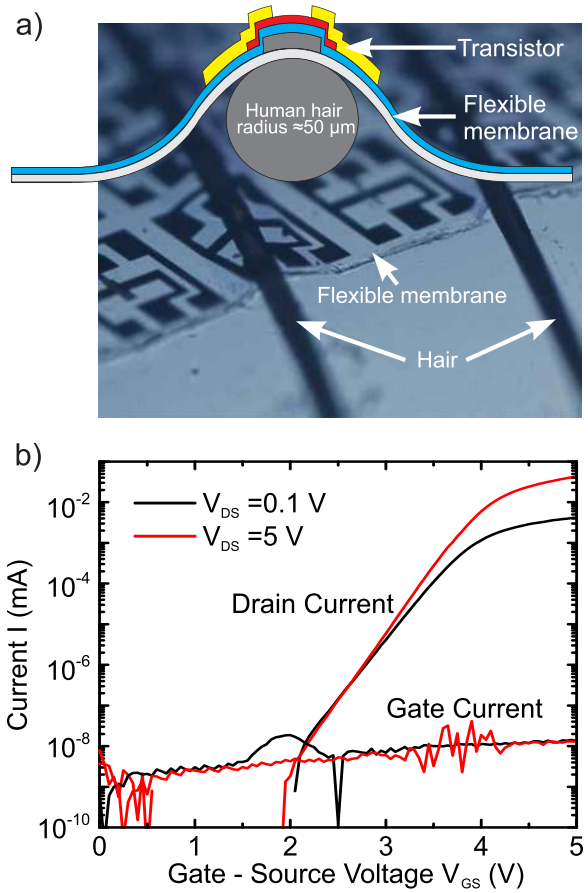

FIG. 27. Flexible IGZO TFTs on a 1 μm thick parylene membrane bent around a human hair with a radius of 50 μm: (a) optical micrograph and device schematic, as well as (b) transfer characteristic. Reproduced with permission from Salvatore *et al.*, Nat. Commun. **5**, 2982 (2014). Copyright 2014 Nature Publishing Group.

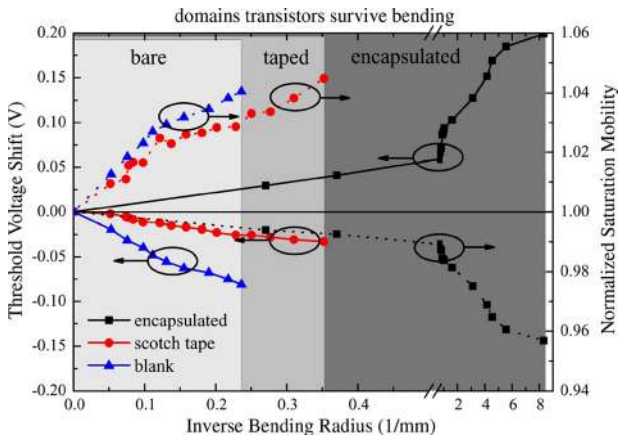

FIG. 28. ΔV_{TH} and normalized μ_{SAT} extracted for different flexible IGZO TFTs (bare, protected with scotch tape and encapsulated) bent to radii as small as 0.125 mm. Reproduced with permission from Kinkeldei *et al.*, IEEE Electron Device Lett. **32**, 1743 (2011). Copyright 2011 Institute of Electrical and Electronic Engineers.

5. Additional features

Electrical and mechanical performance are the two most investigated characteristics of flexible n-type vacuum-processed metal oxide semiconductor TFTs. Nevertheless, the

unique physical properties of metal oxide semiconductors also enable devices which are transparent, stretchable, dissolvable, mechanically active, and even biomimetic and biodegradable.

a. Transparency. Together with flexibility and stretchability, also transparency is an important requirement to seamlessly embed electronic devices into everyday objects, especially to enable applications such as electronic windshields or smart glasses. To realize transparent devices, metal oxide semiconductor TFTs are ideal candidates, due to the intrinsic transparency of the active layer and of nearly all available gate dielectrics (both metal oxides and polymers). To fabricate an entirely transparent device, also the metallic (and therefore opaque) gate and source/drain contacts have to be replaced by transparent conductors. To manufacture transparent conductors, ITO is the most commonly used material,[29,78,80,106,135,137,139,155,158,180,188,189,202,204,205] together with IZO,[133,160,171,184,208] AZO,[93,134] and In_2O_3.[171] Nevertheless, compared with the metallic contacts, conductive metal oxide contacts reduce the TFT bendability. An alternative to brittle metal oxide contacts is the use of graphene which combines flexibility, transparency, and high specific conductivity.[96] For transparent applications, it is essential that not only the device itself but also the substrate is transparent. Unfortunately, the most common material (standard PI) is only partially transparent and exhibits a yellowish to brownish color. Nevertheless, a variety of fully transparent substrates compatible with the fabrication of flexible metal oxide semiconductor TFTs are available, including: PET,[29,69,96,165,171,180,184,188] PEN,[38,40,41,134,136,139,149,153,158,163,166–168,173,181] PC,[154,157] transparent PI and PI-based nano silica composites,[133,142,144,159] parylene,[80,141] PDMS,[78,132,147,205] PVA,[82] and finally glass and glass-fabric reinforced composites.[93,160,169,174] The combination of only transparent materials in one device stack results in fully transparent devices.[78,80,139,188,205] To quantify the transparency of their n-type vacuum-processed metal oxide semiconductor TFTs, some groups have also measured the lucency of the devices in the visible wavelength range, reporting average transmittance values between 70% and 85%[133,134,139,160,180,184] for the complete device stack, as well as 80% (measured on IGZO film only)[29] or 85% of the devices itself in combination with ≈90% transmittance of the substrate.[78] The layout and optical performance of IGZO TFTs fabricated on thin flexible glass substrate are illustrated in Fig. 29, where a transmittance value of 80% was reported.[160] It is worth mentioning that, if designed and fabricated properly, transparent n-type vacuum-processed metal oxide semiconductor TFTs can also exhibit excellent mechanical properties like bendability down to radii of 50 μm,[80] and stretchability by up to 5%.[78]

b. Stretchability. To enable the integration of electronics into soft, elastic, or even 3D deformable objects, n-type vacuum-processed metal oxide semiconductor TFTs need to be also stretchable. Biomedical implants and artificial electronic skins are good examples demonstrating the need for

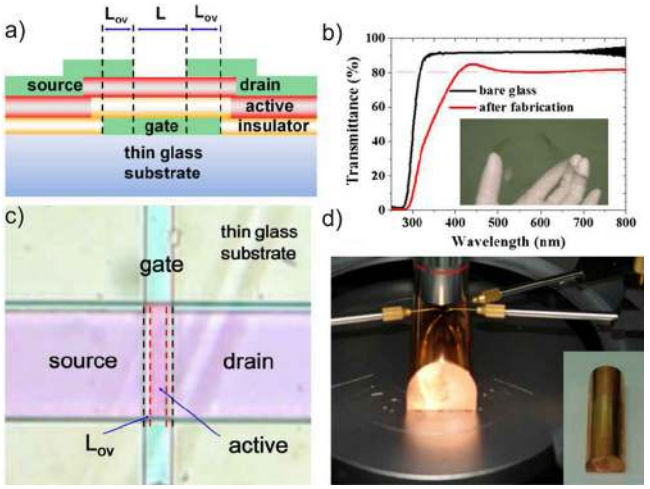

FIG. 29. Fully transparent IGZO TFTs fabricated on flexible glass: (a) device cross-section, (b) optical micrograph, (c) transmittance measurement, and (d) photograph of the devices bent and contacted. Reproduced with permission from Lee *et al.*, Semicond. Sci. Technol. **29**, 035003 (2014). Copyright 2014 Institute of Physics Publishing.

microelectronic devices yielding mechanical properties similar to human skin or other organic tissues. Skin is indeed not only bendable but also stretchable by up to 70%.[81] N-type vacuum-processed metal oxide semiconductor TFTs cannot be directly stretched to such large values, as they can withstand maximum strain values of 1.89%.[202] However, recently several approaches have been proposed to realize stretchable n-type vacuum-processed metal oxide semiconductor TFTs with the use of advanced substrates or geometries:

(I) First of all, stretchability can be achieved by using composite elastomeric substrates. These composite substrates can be engineered in order to present a globally low elastic modulus, which is locally increased in specifically designated device islands. By limiting the strain in these stiff islands, it is possible to protect the devices from the extensive strain they are subject to during stretching. Nevertheless, it is essential to realize a smooth transition between the areas with high and low stiffness, since abrupt stiffness changes are more prone to stress localization (and therefore also to delamination during stretching). At this aim, Erb *et al.* used particle reinforcement to increase the stiffness of polyurethane (PU),[162] as well as to realize a smooth transition between the stiff and stretchable areas. By adding 20 vol. % of magnetically responsive anisotropic alumina microparticles, an increase of 478% of the stiffness of the PU has been achieved.[162] On top of this composite substrate, IGZO TFTs have been manufactured. Due to the shadow mask-based fabrication process (PU has only limited resistance against photolithographic chemicals) and the high surface roughness of around 200 nm, the IGZO TFTs show only limited device resolution and performance. Furthermore, stretching experiments of the resulting devices have not been reported. Another stretchable composite substrate with mechanically graded patches has been fabricated

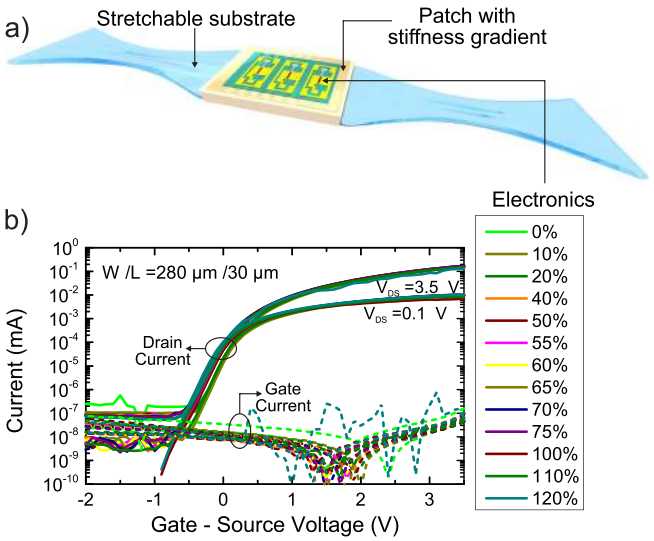

FIG. 30. Elastic IGZO TFTs realized by the use of composite substrates: (a) schematic and photograph and (b) transfer characteristics (measured under different levels of global strain) of devices on a stretchable polyurethane composite substrate. Reproduced with permission from Münzenrieder *et al.*, Adv. Electron. Mater. **1**, 1400038 (2015). Copyright 2015 John Wiley and Sons.

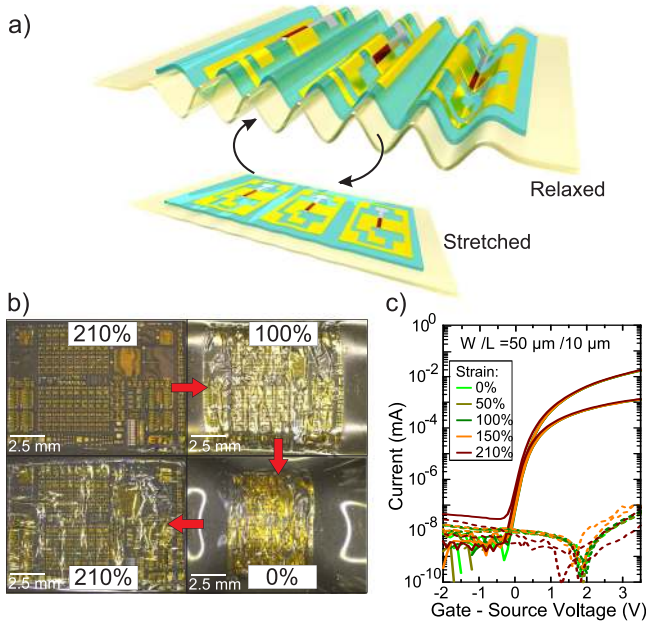

FIG. 31. Elastic IGZO TFTs realized by wavy geometries: (a) visualization, (b) micrographs (taken at different stretching stages), and (c) transfer characteristics (measured for different levels of applied strain) of wavy devices. Reproduced with permission from Münzenrieder *et al.*, Adv. Electron. Mater. 1, 1400038 (2015). Copyright 2015 John Wiley and Sons.

by welding layers of PU-based materials with gradually increasing elastic moduli.[81] In this case, the elastic moduli of the layers have been adjusted at molecular, nano- and microscale by changing the concentration of the PU hard domains, laponite, and alumina platelets, respectively. The resulting elastic moduli span from 40 MPa to 5150 MPa.[81] Given the incompatibility also of this substrate with photolithographic chemicals, IGZO TFTs have been fabricated on a 1 μm thick parylene membrane and afterward transferred to the reinforced islands (Fig. 30(a)). The resulting IGZO TFTs are fully functional while the substrate is strained by 300% and after 4000 cycles of stretching and relaxation. Fig. 30(b) shows the evolution of the TFT transfer characteristic under increasing global strain.

Moreover, full device operation on the 3D surface of a sphere (R = 14 mm) is also possible.[81] In addition to composite PU substrates, recently also engineered elastomeric substrates constituted by PDMS with micro-fabricated and embedded stiff SU-8 device islands have been reported.[207] The smooth stiff-to-soft transition between SU-8/PDMS and PDMS allows stretching the IGZO TFTs manufactured directly on the so-formed device islands to 20%.[207]

(II) Alternatively, stretchable TFTs can be realized using "wavy" geometries. The idea is to realize devices with mechanical properties similar to those of an accordion and at the same time mimic the behavior of human skin. To obtain such wavy devices, the elastomeric substrate needs to be wrinkled while relaxed and subsequently re-flattened during stretching. The fabrication can be done by manufacturing or transferring the TFTs onto a pre-stretched elastomeric substrate. The subsequent release of the pre-induced strain leads to the formation of out-of-plane wrinkles on the substrate surface. The TFTs transferred/manufactured on such "wavy" substrates do not need to be stretchable but have to survive to the harsh bending conditions they are subject to while wrinkled (typical bending radii are $\lesssim$100 μm). Using this approach, IGZO TFTs have been fabricated on a 1 μm thick parylene membrane and then transferred to a pre-stretched elastomer (VHB tape from 3 M) has been demonstrated.[81] The resulting devices are visualized in Figs. 31(a) and 31(b), where TFT operation at substrate strain of up to 210% is demonstrated (Fig. 31(c)). Finally, there is one single report on wrinkled IGZO TFTs directly fabricated on PDMS.[147] In this work, the PDMS has been spin coated on a Si wafer and backed at 150 °C. Due to the different CTE of the Si wafer and the PDMS, tensile strain is induced into the PDMS. The following TFT fabrication and release of the PDMS from the wafer causes a bi-directional relaxation of the PDMS of $\approx$3.5% and the formation of wrinkles in the device layers. Thanks to the so-formed wrinkles, the resulting IGZO TFTs can be stretched by up to 2.3%.

(III) It is also possible to combine wavy geometry and composite substrate.[78,205] In the works of Park *et al.* and Sharma *et al.*, ZnO or IGZO TFTs have been fabricated on a rigid substrate, covered with an epoxy cap and afterward transferred to a bi-axially pre-stretched PDMS substrate. Release of the pre-formed strain results in the formation of wrinkles in the interconnection lines, while the epoxy reinforced TFTs stay flat. These devices show no significant influence

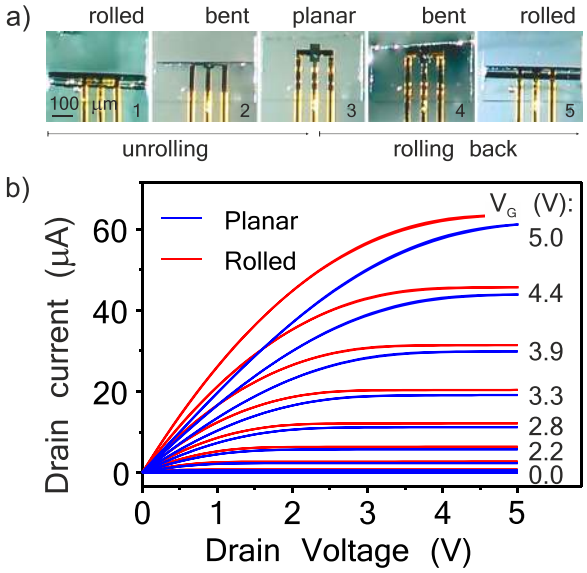

FIG. 32. Mechanically active biomimetic IGZO TFTs: (a) reversible rolling and (b) corresponding TFT output characteristic measure, while the TFTs are flat and bent in compressive direction. Reproduced with permission from Karnaushenko *et al.*, Adv. Mater. **27**, 6797 (2015). Copyright 2015 John Wiley and Sons.

to strain of 5%, and after more than 100 cycles of compression and stretching.

c. Dissolubility. Recently, also completely water-soluble metal oxide semiconductor TFTs have been demonstrated.[82] These devices are based on Mo contacts, SiO_x gate dielectric, and IGZO semiconductor. The fabrication takes place on a Si wafer coated with a Ni sacrificial layer; subsequently, the complete devices are transferred to a water-soluble 20 μm thick PVA substrate. The complete layer stack can be dissolved in 60 °C heated de-ionized (DI) water. The PVA substrate, for example, can be completely dissolved after 1800 s.

d. Mechanical activity. Karnaushenko *et al.* have recently demonstrated a unique combination of mechanical and electrical performance by fabricating IGZO TFTs on a highly cross-linked hydrogel/PI composite substrates. In this work, the hydrogel acts as a swelling layer, whereas the PI serves as a stiff and chemically robust substrate for the TFT fabrication. In response to different chemicals, the resulting devices are able to reversibly self-assemble into micro tubes with radii ranging from the millimeter range down to 25 μm. As shown in Fig. 32, the TFTs are not significantly affected by this self actuated deformation.[23]

C. Flexible n-type solution-processed TFTs

In this subsection, the materials and fabrication techniques involved in the realization of flexible n-type solution-processed metal oxide semiconductor TFTs are discussed. Subsequently, the electrical performance and the mechanical properties of the resulting devices are presented.

1. Materials

As already done for flexible n-type vacuum-processed metal oxide semiconductor TFTs, in the following we describe the substrates, dielectric layers (barrier, gate dielectric, and passivation), and conductive materials (gate and source/drain) employed to manufacture flexible n-type solution-processed metal oxide semiconductor devices.

a. Substrates. Flexible metal oxide semiconductor TFTs fabricated by vacuum- and solution-processed processes share common substrate requirements, such as low surface roughness, flexibility, compatibility with the required process temperatures, as well as resistance against the needed solvents. Compared with vacuum processing of metal oxide semiconductors, solution-deposition techniques typically require higher temperatures ($\geq$250 °C). As a result, substrates with high temperature resistance ($T_G \geq 300$ °C) are necessary. Due to their high $T_G \approx 360$ °C, PI substrates with thickness ranging from $\approx$3 to 50 μm are widely used.[83,145,191,193,197–199,220–223] Polyarylate (PAR) foils have also been employed,[192,200,224,225] given their good temperature stability ($T_G \approx 330$ °C), combined with a colorless transparency in the visible range. If the semiconductor deposition is performed at lower temperatures ($\leq$150 °C), also PES foils (T_G around 200 °C) can be utilized.[226] In an attempt to reduce the substrate cost, especially when cost-effective high throughput fabrication processes are targeted, less expensive (but also less thermally resistance) polymer substrates like PEN[190,195–197,227,228] and PET[76,194,229,230] have been employed. Additionally, the use of paper substrates for flexible solution-processed ZnO TFTs has been investigated.[229,231] Finally, flexible glass substrates have been utilized to allow high annealing temperatures (500 °C) in solution-processed IGZO TFTs.[201]

b. Barrier layers. The use of barrier layers for flexible n-type solution-processed metal oxide semiconductor devices is not very common. A few examples include c-PVP layers applied to planarize and smoothen the surface of PES or PI,[191,226] as well as PVP films utilized to reduce the surface roughness of PI foils from 3.6 nm down to 0.3 nm (root mean square).[232] Also, inorganic barrier layers (e.g., Al_2O_3[196] and SiO_2[83]) have been utilized to planarize, reduce the water permeation, and improve the wettability of PI substrates. Finally, for the purpose of promoting adhesion between PI and either Cr gate contacts or various oxide materials, both SiN_x[145] and zirconium oxysulphate[198] have been employed.

c. Gate dielectrics. As for flexible n-type vacuum-processed metal oxide semiconductor TFTs, also in this case metal oxide gate dielectrics grown from vacuum deposition techniques are widely used, especially SiO_2[76,199,222] and Al_2O_3.[145,197] Nevertheless, for solution-deposited metal oxide semiconductors, it is preferable to solution process also the gate dielectric, in order to further benefit from the low-cost large-area approach offered by solution-deposition processes. Within solution-processed gate dielectrics, polymeric materials are especially suitable due to the moderate annealing temperatures needed, as well as the high bendability that can be achieved.[229] In particular, poly(methyl methacrylate) (PMMA) and PVA gate dielectrics have been evaluated in combination with flexible solution-processed ZnO, In_2O_3, or

IZO TFTs.[194,229,233,234] Nevertheless, compared with metal oxide dielectrics, polymers yield a lower ϵ_R and thus result in devices with higher operational voltages. To combine the advantages of metal oxide dielectrics and solution-processing, recently increasingly efforts have been devoted to grow metal oxide dielectrics with low temperature solution-processing techniques. Main breakthrough in this direction has been achieved by Pal *et al.*, who demonstrated the first solution-processed amorphous Al_2O_3 gate dielectric on PI using an annealing temperature of only 200 °C.[235] Since then, many other groups reported solution-processed Al_2O_3 dielectrics on flexible PI or PAR substrates.[192,220,221,224] Zirconium oxide (ZrO_2)[191,195,198] and tantalum oxide (Ta_2O_5)[201] are other promising metal oxide dielectrics that can be solution-processed on flexible substrates. In this context, it has been shown that the use of high-ϵ_R metal oxide dielectrics (e.g., Al_2O_3, ZrO_2, or Ta_2O_5) not only allows lowering the device voltage operation but also leads to better TFT performance if compared with devices employing dielectrics with lower ϵ_R (e.g., SiO_2, PMMMA, or PVA).[83,192,195,200,224] This improvement is generally ascribed to a reduction of the interfacial trap density and thus to an enhancement of the semiconductor-dielectric interface. Another promising class of dielectric materials comprises ionic liquid/gels and polymer electrolytes. As already reported in Sec. II B, electrolyte dielectrics allow achieving high C_{ox} values and therefore low operation voltage typically below ±2 V. Examples of electrolyte gated n-type solution-processed metal oxide semiconductor TFTs have been successfully demonstrated on PEN, PI, and paper substrates.[190,193,231] Due to the good conformal coating, electrolyte gate dielectrics facilitate also the deposition of structured/rough metal oxide semiconductors, especially nanoparticles (NPs) and nanorods (NRs).

d. Contacts. The contact materials used in n-type solution-processed metal oxide semiconductor TFTs are generally similar to those employed for their vacuum-processed counterparts. Source/drain and gate electrodes are mostly made of Al and Au,[145,193,231] but also of transparent conducting metal oxides, such as ITO,[76,83,190,196,197] IZO,[220,221] or zinc indium tin oxide (ZITO).[192] In addition to the above mentioned materials, gate contacts are also made of Cr[145] or dual layers of Cr/Au,[220,221] which yield a good adhesion. Aiming towards completely solution-processed TFTs, contact materials have also been processed from solution, employing solution-processed poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) gate electrodes[193] or solution-deposited ITO source/drain and gate contacts.[83]

e. Passivation layers. The application of passivation layers in flexible n-type solution-processed metal oxide semiconductor TFTs is not very common. The few available examples include Al_2O_3[196,197] and PMMA layers.[220,221] In particular, 400 nm thick PMMA layers have been utilized to encapsulate flexible solution-processed In_2O_3 and IGZO TFTs fabricated on thin spin coated PI.[220,221] In particular, PMMA encapsulations allow reducing the mechanical stress (and therefore crack formation) during the release of the PI foil from the rigid glass carrier.

2. Fabrication techniques

Like flexible n-type vacuum-processed metal oxide semiconductor TFTs, solution-processed devices employ similar fabrication techniques (especially for the substrate preparation, layer structuring, and device configuration). Main difference between vacuum and solution-processed TFTs is constituted by the deposition methods, which focus on solution-processes (for the active layers and sometimes also for the gate dielectrics and contacts).[87,236,237] After a brief presentation of the substrate preparation methods, the main focus is on solution-processing techniques (i.e., general remarks, deposition methods, and approaches to lower the process temperatures).

a. Substrate preparation. As for vacuum-processed devices, also in this case it is common to employ free-standing polymer foils with thickness of ≥50 μm.[145,191,193,197,199,222] Alternatively, polymers can be spin coated onto a carrier substrate (thickness of ≈3–18 μm) and subsequently peeled off after the device fabrication has been completed.[83,220,221]

b. General remarks on solution-processing. Contrary to most organic semiconducting materials, typical metal oxide semiconductors are not at all or only poorly soluble in common solvents. This is why solution-processing of metal oxide semiconductors cannot occur by simply dissolving the selected materials but requires a chemical reaction (synthesis) between suitable reagents (the so-called precursors). In general, two approaches can be used to solution-deposit metal oxide semiconducting materials:[236] (A) The material is first synthesized and tailored into nanoparticles, nanorods, or nanowires.[76,190,226,227,230,231,238] These nano-scaled shapes are then dispersed in suitable solvents and subsequently deposited and dried. (B) Alternatively, the precursor solution is first deposited and then converted to the final metal oxide semiconducting material, most commonly via thermal annealing at temperatures in the range of 200 to 500 °C, or alternatively via UV irradiation.[87,116,197,200,224,239] The benefit of approach (A) is that the deposition is decoupled from the synthesis, and therefore also from potentially high process temperatures. Using approach (A), crystalline metal oxide semiconductors can thus be easily synthesized and further tailored through their size and shape.[240] There are, however, a number of drawbacks connected to approach (A). First of all, often a stable dispersion of the materials requires the use of additives or ligands (mainly insulating), which then need to be removed from the final film to improve the contact between particles.[241] This removal process usually involves thermal annealing above 300 °C, which is in conflict with the use of temperature-sensitive flexible substrates. Alternative, the high temperature annealing can be substituted by additional low temperature treatments such as UV irradiation, vacuum annealing, or plasma treatments, which anyway complicate the fabrication process.[195,242,243] Additionally, an active channel layer

constituted by nanoparticles inherently features a high number of (grain) boundaries, each one acting as a potential barrier against charge transport. Furthermore, high film porosity and roughness at the interface semiconductor/gate dielectrics have been demonstrated to be detrimental for the TFT performance.[190,238] The impact of residual ligands, grain boundaries, as well as interfacial roughness generally limit the carrier mobility of flexible n-type solution-processed metal oxide semiconductor NP TFTs in approach (A) to below $1\,cm^2\ V^{-1}\ s^{-1}$.[190,226,230,231,241] Compared with NPs, NWs with lengths of several micrometer can lead to unhindered transport all over the active channel (even with only a single wire) and consequently result in drastically increased μ_{FE} of over $120\,cm^2\ V^{-1}\ s^{-1}$.[76,227] Nevertheless, difficulties of alignment and accurate placement of the NWs with respect to the source/drain electrodes are a drawback for more widespread applications. In approach (B), the conversion step takes place after the precursor deposition and therefore in direct contact with the substrate material. Depending on the precursor material, temperatures in excess of 300 °C are typically required to achieve a full material conversion, as well as good layer properties.[244] The commonly high thermal budget required in approach (B) strongly limits the choice of the flexible substrates to materials such as PI[145,193] or PAR.[192] Nevertheless, recent efforts have been devoted to the reduction of the annealing temperatures required to solution-process metal oxide semiconductors (and also gate dielectrics)[87,116,119,237,245] which consequently allows selecting a wider range of substrate materials, including PEN,[196,197,228] and PET.[194,229]

c. Deposition methods. As for vacuum-processed devices, also for flexible n-type solution-processed metal oxide semiconductor TFTs, standard vacuum deposition techniques are widely used, especially to manufacture the conductive and insulating materials. To grow barrier, gate dielectrics, and passivation layers, vacuum-deposition tools like ALD (for Al_2O_3)[83,145,196,197,200] and PECVD (for SiO_2 and SiN_x)[76,83,145,199,222] are commonly utilized. For source/drain and gate contact deposition, thermal and e-beam evaporation[145,193,220,221,231] as well as sputtering[76,83,190,192,196,197,220,221] are mainly employed. With regards to solution-deposition processes on flexible substrates, there are several techniques in use. For most of these techniques, both approaches (A) and (B) can be employed:

(I) Spin coating is the most common coating method used in research environments:[87,237] the film is formed from a liquid precursor ink as a result of the substrate's rotational motion. The layer thickness can be precisely controlled by parameters like spin speed and duration, as well as precursor concentration. Main advantages of spin coating are process simplicity and low investment costs. Additionally, spin coated films yield homogeneous and reproducible film properties. As a drawback, however, spin coating can only be carried out in batch processes and becomes more challenging when the substrate size is increased. Spin coating technique is commonly utilized for flexible metal oxide semiconductor TFTs to grow In_2O_3,[191,197,224] ZnO,[195,229,233] and IGZO[83] active layers. Additionally, many dielectrics layers have also been spin coated on flexible substrates, such as organic PVP barrier layers[191,226,232] or oxide Al_2O_3 and ZrO_2 dielectrics.[83,191,192,195,220,221,224] To realize flexible fully solution-processed devices, also spin coated ITO source/drain and gate electrodes have been reported.[83]

(II) Drop casting is probably the simplest deposition technique in which a defined volume of solution is manually dispensed at the desired location. To control the drying behaviour of the droplet, the substrate can be kept at elevated temperatures. Subsequent annealing steps allow improving the film quality. Especially, TFTs based on nanowires[227] and nanorods[231] following approach (A) have been demonstrated with this technique.

(III) It is also possible to solution deposit metal oxide semiconductors on flexible substrates at low temperatures using hydrothermal growth. Here, the metal oxide formation takes place directly on the substrate surface during the substrate submersion in a heated precursor solution. Growth conditions can be configured to achieve compact films,[194] or NW growth.[246] The deposition time and precursor concentration define the final layer thickness. ZnO TFTs grown at 90 °C on PET substrates have been demonstrated by Lee *et al.* using this method.[194]

(IV) A more sophisticated method is ink-jet printing, which is a digitally controlled drop-on-demand deposition technique. During ink-jet printing, the metal oxide semiconductor is deposited only where needed, preventing waste of material and need for subsequent patterning steps. As ink-jet patterns can easily be controlled digitally (without the need of a physical mask/template), design alterations and prototyping can be carried out easily. However, due to the patterned deposition, the ink drying conditions need to be specially controlled, in order to avoid irregularities and effects such as the coffee ring formation. Examples of ink-jet printed metal oxide semiconductors include ITO nanoparticles [approach (A)],[247] as well as ZnO, In_2O_3, or ZTO from a precursor solution [approach (B)].[198,239,248]

(V) In the process of spray pyrolysis, a fine spray of the precursor solution is created (using an air-blast or an ultrasonic nozzle) and directed onto a heated substrate.[244] Given a sufficiently high substrate temperature, the precursor immediately undergoes the conversion reaction and forms the final film material. In addition to the specific precursor material and concentration, parameters such as substrate temperature, droplet size and distribution, as well as solvent type and feed rate present the toolbox to fine tune the material parameters. Good film properties of metal oxide semiconductors processed via spray pyrolysis are normally only achieved for temperatures in excess of 300–400 °C,[87] thereby ruling out plastic substrates.

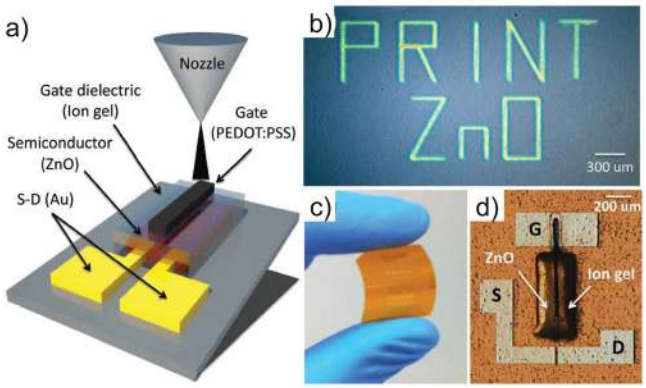

FIG. 33. Flexible aerosol-jet printed ZnO TFTs: (a) device cross-section, (b) example of aerosol-jet printed ZnO pattern, and (c) and (d) complete TFT structure on PI substrate. Reproduced with permission from Hong *et al.*, Adv. Mater. **25**, 3413 (2013). Copyright 2013 John Wiley and Sons.

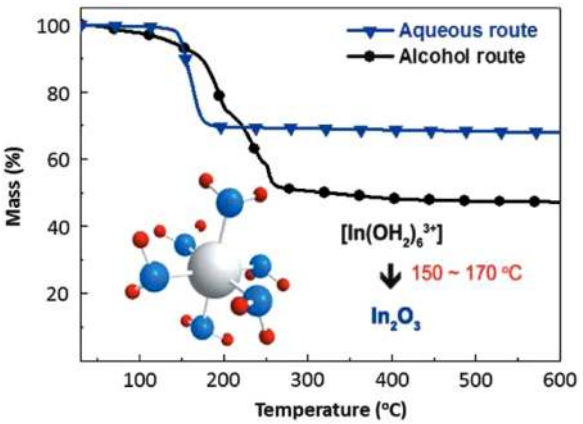

FIG. 34. Thermogravimetric analysis of indium oxide (In_2O_3) precursor solution showing that water requires a lower decomposition temperature if compared with 2-methoxyethanol. Reproduced with permission from Hwang *et al.*, NPG Asia Mater. **5**, e45 (2013). Copyright 2013 Nature Publishing Group.

However, recent advances have enabled the realization of spray coated In_2O_3 TFTs at 250 °C[249] on PI substrates.[145] Main advantage of spray pyrolysis is the possibility to automate the spraying process, thus ensuring repeatability of the film characteristics. In addition, the spray pyrolysis deposition can be further up-scaled, and potentially run in a continuous process.

(VI) Aerosol-jet printing combines attributes from spray pyrolysis and ink-jet printing. In aerosol-jet printing, a fine mist is created and then shaped (by an inert carrier gas and a special nozzle design), in order to allow localized and digitally controlled deposition with feature sizes in the order of a few tens of μm (see Fig. 33(a)). Aerosol-jet printing has recently been utilized to realize the semiconductor (ZnO), the dielectric (ionic gel), and the gate electrode (PEDOT:PSS) in flexible TFTs fabricated on PI at temperatures $\leq$250 °C (see Fig. 33).[193]

(VII) Other solution-processing techniques such as blade/bar coating, slot-die casting, gravure, or flexographic printing are traditionally more in use for organic semiconductor devices and/or solar cells. However, such techniques are currently emerging and their suitability for the fabrication of flexible metal oxide semiconductor TFTs is being investigated. For example, Leppäniemi *et al.* showed the successful flexographic printing of In_2O_3 patterns on PI substrates with a maximum process temperature of 300 °C.[250] Similarly, in a recent study by Lee *et al.*, the bar coating method has been employed to fabricate semiconducting (IGZO) and dielectric films (Al_2O_3, HfO_2) in low voltage TFTs. This technique allows precise thickness control over large areas (4 in. wafer) and, using self-assembled monolayers the creation of selective wetting contrasts, including the possibility of direct patterning during the printing process. Although full devices with good performance ($\mu_{FE} \approx 5\,cm^2\,V^{-1}\,s^{-1}$ at 380 °C) have only been presented on rigid Si substrates, the successful film formation on PI is promising in view of future optimization.[251]

d. Approaches for low temperature solution-processing. Especially for precursor-based methods [approach (B)], there is a wide range of possible techniques to reduce the temperatures needed to solution-process the materials:

(I) First of all, the choice of the precursor material is essential. Thermogravimetric studies of different chloride, acetate, and nitrate precursors generally showed that nitrates react at the lowest temperatures.[237] As a consequence, indium nitrate [$In(NO_3)_3$] has been used in many studies to form either In_2O_3, IZO, or IGZO at temperatures between 200 and 300 °C.[145,191,224] The same applies for Al_2O_3, which can be formed from aluminum nitrate [$Al(NO_3)_3$] using thermal annealing at 200 °C.[224]

(II) In addition to the precursor material itself, the selected solvent can also directly influence the conversion temperature. A study by Hwang *et al.* compared the effect of water and 2-methoxyethanol (2-ME) as solvents for $In(NO_3)_3$ precursors.[197] The decomposition temperature for 2-ME was found to be >230 °C, whereas water only requires ≈170 °C (see Fig. 34). The lower decomposition temperature of water solvent is attributed to the formation of an $[In(OH_2)_6]^{3+}$ complex, whose relatively weak coordination bonds can be broken without excessively high annealing temperatures.

(III) The combination of precursor and solvent is also important. To allow solution-processing of ZnO active layers at temperatures down to 150 °C, Meyers *et al.* proposed to form zinc (Zn) ammine complexes in aqueous solution.[239] The precursor preparation was achieved by dissolution of Zn nitrate in water, followed by precipitation of $Zn(OH)_2$ after the addition of NaOH. Several centrifugation and washing steps

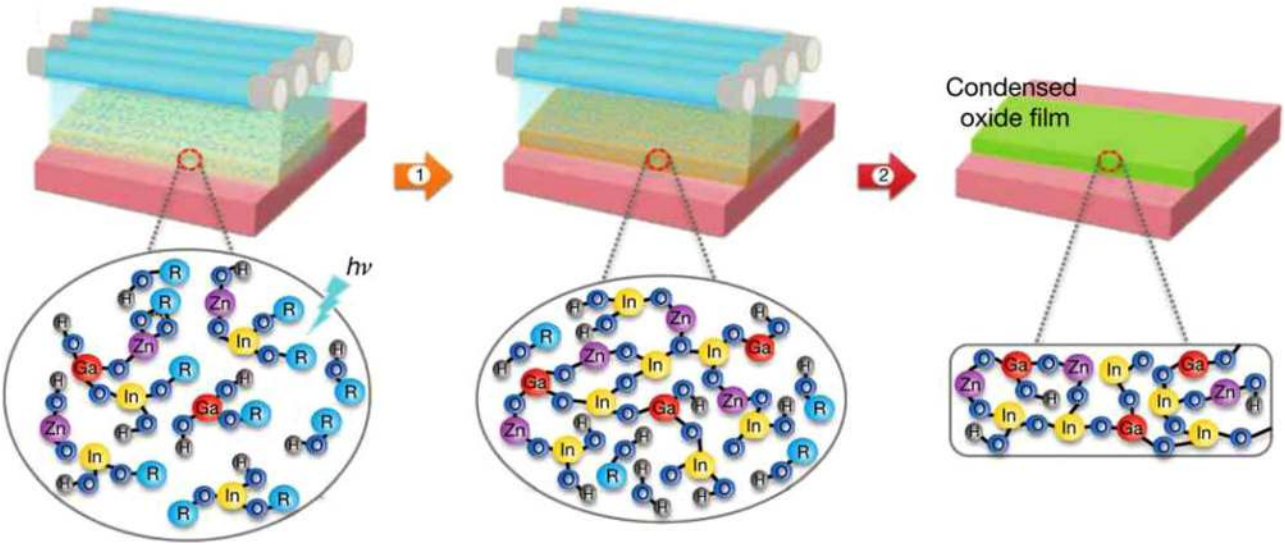

FIG. 35. Scheme of deep UV photoactivation process for low temperature solution-deposition of metal oxide semiconducting films. Reproduced with permission from Kim *et al*., Nature **489**, 128 (2012). Copyright 2012 Nature Publishing Group. Initiated by UV photons, as spun precursor films undergo condensation reactions to form initial metal-oxide-metal framework structures (step 1). Ongoing irradiation continues the process and leads to film densification (step 2) by gradual removal of oxygen and carbon.

were applied to remove Na^+ and NO_3^- ions in the solution before the final complex was created by addition of aqueous ammonia. This laborious process has been simplified by several research groups by directly dissolving ZnO, $Zn(OH)_2$, or $ZnO \cdot H_2O$ powder in ammonia solution.[195,222,233,252] In particular, Fleischhaker, Wloka, and Hennig employed a process temperature of $\leq 150\,^{\circ}C$ to fabricate BG ZnO TFTs on flexible PEN substrates with different polymeric dielectrics.[233] Interestingly, Lin *et al*. combined the Zn ammine approach with a low temperature solution-processable high-ϵ_R ZrO_2 gate dielectric to realize low-voltage ZnO TFTs fabricated on PEN at a maximum process temperature of $160\,^{\circ}C$.[195]

(IV) Another possibility to lower the process temperatures is to locally induce a hydrolysis reaction on the surface of as-deposited films. This approach (so-called sol-gel on chip) has been utilized by Banger *et al*. to obtain low temperature solution-processed amorphous IZO and IGZO.[253] The sol-gel on chip process uses mixed metal alkoxide solutions spin coated in nitrogen (N_2) atmosphere and subsequently annealed at 230–275 °C under controlled water vapor environment. Nevertheless, the application of this approach on flexible substrates (even if possible due to the low processing temperatures) has not been demonstrated yet.

(V) Another effective method to lower the temperatures of solution-processed metal oxide semiconductors is the so-called combustion chemistry approach introduced by Kim *et al*.[224] The idea behind combustion chemistry is to utilize an exothermic reaction that takes place inside the precursor on the as-deposited film. The locally self-generated energy is then able to further carry on the conversion reaction. In this way, only a small amount of external energy supply (i.e., a low annealing temperature) is required to surmount the energy barrier that activates and carries out the following reaction. The precursor composition was chosen by Kim *et al*. to include a fuel component, either acetylacetone or urea, as well as metal nitrates (acting as oxidizing agents). Using this technique and limiting the annealing temperature to $200\,^{\circ}C$, Kim *et al*. were able to demonstrate flexible In_2O_3 devices on PAR substrates.[224]

(VI) Another way to create metal oxide semiconducting materials at low temperatures has been proposed by Kim *et al*.[200] In their work, Kim *et al*. employed a mercury lamp with peak performance at 184.9 nm and 253.7 nm to photo-activate an UV-absorbing precursor containing In, Ga, and Zn salts under nitrogen environment.[200] The authors described the process as a UV-assisted photochemical cleavage of metal alkoxide groups followed by metal-oxide-metal network formation and further densification. An unintentional heating of the substrate to $150\,^{\circ}C$ was demonstrated to be necessary for a successful precursor conversion. The so-formed IGZO films were embedded into TFTs on PAR substrates.[200] Furthermore, similar UV irradiation approaches have been used for low temperature solution-processed gate dielectrics (ZrO_x and HfO_2).[195,220,254] A schematical overview of the UV photoactivation process is shown in Fig. 35.

(VII) Finally, it is possible to combine UV illumination and combustion chemistry.[83] In the work by Rim *et al*., solution-deposited IGZO was formed from a precursor solution containing metal salts (necessary to grow IGZO), as well as additives of acetylacetone and ammonium hydroxide. On one hand, both additives, respectively, act as fuel and oxidizer component for the combustion reaction. On the other hand, the additives enable the formation of metal chelate complexes

TABLE III. Set of performance parameters extracted from recently demonstrated flexible n-type solution-processed metal oxide semiconductor TFTs, together with fabrication details (i.e., maximum process temperature and semiconductor deposition technique).

	Semiconductor deposition	Maximum temperature (°C)	Mobility ($cm^2\ V^{-1}\ s^{-1}$)	Threshold voltage (V)	Current on/off ratio	Substrate thickness (μm)	Bending radius (mm)	Strain (%)	Bending cycles
ZnO NR TFT with ion-gel electrolyte gate dielectric[231]	Drop-casting	150	0.03	0.8	10^2	...	1.1	…	100
In_2O_3 NP TFT with electrolyte gate dielectric[190]	Ink-jet printing	RT	0.8	0.55	2×10^3	125	…	…	…
ZnO TFT with PVP gate dielectric[229]	Spin coating	200	0.09	5.4	10^5	12	4.3	…	10 000
ZnO TFTs with ion-gel electrolyte gate dielectric[193]	Aerosol-jet printing	250	1.6	0.97	10^5	50	25	1	10 000
Quasi-superlattice metal oxide semiconductor TFTs with ZrO_2/Al_2O_3 gate dielectrics[228]	Spin coating	175	11	0.5	10^5	…	…	…	
In_2O_3 TFTs[145]	Spray pyrolysis	250	0.2	5.29	6×10^3	50	4	0.65	…
IGZO TFTs with Al_2O_3:Zr gate dielectric[221]	Spin coating	150	7.7	1.26	10^9	3	1	…	…
IGZO TFTs[83]	Spin coating	350	84	0.6	10^5	18	10	…	320

with enhanced UV absorption. Consequently, UV irradiation can be used to initiate the metal oxide semiconductor formation with the support of an exothermic combustion reaction. The authors employed the same processing scheme to solution-deposit ITO and Al_2O_3 as contact materials and dielectric, respectively.

e. Layer structuring. As for flexible n-type vacuum-processed metal oxide semiconductor TFTs, similar layer structuring methods can be employed for flexible n-type solution-processed metal oxide semiconductor devices. In addition to the standard patterning methods, depending on the specific deposition technique used, additional means to structure the solution-processed layers are possible. Both ink-jet and aerosol jet printing are direct-write methods,[236] meaning that the liquid deposition is carried out only where desired. This reduces material waste and avoids further patterning steps. Due to the digital designs and computer controlled deposition, both ink-jet and aerosol printing allow a flexible and fast patterning. Feature sizes from a few tens up to several hundreds of microns can be easily achieved with these techniques.[190,193,236,239,248] Although not inherently a direct-write method, spray pyrolysis can be combined with shadow masking, as demonstrated for flexible In_2O_3 TFTs on PI.[145] This technique, however, so far is limited to line widths above $\approx 100\ \mu$m.[255] The specific process of combining UV illumination and combustion chemistry shown by Rim *et al.* renders irradiated areas insoluble. In this way, UV treatment through a shadow mask can be used to photopattern the layers with line widths down to 3 μm. This deposition and patterning method (so-called direct light pattern integration) has been employed for IGZO, ITO, and Al_2O_3 layers.[83] Recently, promising results of the first roll-to-roll compatible fabrication of In_2O_3 patterns on PI substrates via flexographic printing have also been demonstrated.[250]

f. Device configuration. The majority of the reported flexible n-type solution-processed metal oxide semiconductor TFTs are fabricated in BG staggered configuration with only few devices in BG coplanar,[145,196] TG staggered,[226] or TG coplanar setup.[231] Only electrolyte gated devices present a configuration where source/drain and gate electrodes are all in the same plane (in-plane configuration).[190]

3. Electrical properties

Flexible solution-processed TFTs based on n-type metal oxide semiconductors show a broad range of electrical performance parameters, depending on the materials, the deposition approaches, and the techniques, as well as the maximum process temperature. An overview of the performance parameters extracted from recently demonstrated flexible n-type solution-processed metal oxide semiconductor TFTs is presented in Table III.

First of all, the performance strongly depends on the solution-deposition approach utilized, based on nano-scaled shapes (A) or on precursors (B). As regards devices based on approach (A), a wide range of performance parameters can be obtained in dependence of the employed shape (NPs, NRs, or NWs). On one hand, flexible NP TFTs typically yield a low $\mu_{FE} \ll 1\ cm^2\ V^{-1}\ s^{-1}$.[190,226,231] The limited performance of flexible NP-based devices can be attributed to the large surface roughness of flexible foils (if compared with rigid Si or glass substrates), which challenges the realization of high-quality nanoparticles. On the other hand, NWs allow realizing longer TFT channels (extending over several microns) based on long range and undisturbed crystalline metal oxide semiconductors. Therefore, flexible NW metal oxide semiconductor devices exhibit higher μ_{FE} up to $120\ cm^2\ V^{-1}\ s^{-1}$ (for In_2O_3 NW TFTs on PET),[76] if compared with NP TFTs. Nevertheless, the random orientation and placement of NWs currently hinder their integration in large-area substrates. Especially for integration purposes, TFTs based on n-type metal oxide semiconductors solution-processed from precursors [Approach (B)] are preferable. Flexible TFT based on metal oxide semiconductor solution-processed from precursors can be roughly sorted into three main categories, according to their performance:

(I) This group includes devices with $\mu_{FE} \leq 1\ cm^2\ V^{-1}\ s^{-1}$.[145,199,222,229,232,233]

(II) The second group contains TFTs with $\mu_{FE} = 1–10\,cm^2\,V^{-1}\,s^{-1}$.[191,193–197,200,220,221,223–225,250]

(III) The third and last group presents a few examples of devices with $\mu_{FE} \geq 10\,cm^2\,V^{-1}\,s^{-1}$.[83,192,201,228]

It is noticeable that with only one exception,[145] all the TFTs in group (I) use either polymeric or SiO_2 gate dielectrics, whereas all the devices in group (II) and (III) predominantly employ metal oxide gate dielectrics (e.g., Al_2O_3 and ZrO_2) with high ϵ_R. Due to the widespread usage of gate dielectrics with high ϵ_R in groups (II) and (III), the device operational voltages are overall small, with threshold voltages $\leq 5\,V$.

a. Device optimization. As for flexible n-type vacuum-processed metal oxide semiconductor TFTs, also in the case of flexible n-type solution-processed metal oxide semiconductor TFTs, the electrical performance can be enhanced by properly selecting the device materials and deposition processes (especially for the semiconductor and the gate dielectric), the maximum process temperature, as well as the device configuration. Additionally, for solution-processed metal oxide semiconductors, there are special approaches to improve the device performance. First of all, in the case of TFTs with nano-scaled shapes [approach (A)], several post-deposition techniques can be applied, for example, to enhance the inter-particle contact. In particular, Bubel and Schmechel used a mechanical layer compaction technique to increase the carrier mobility of ZnO NP-based TFTs from 5×10^{-5} to $\approx 7 \times 10^{-3}\,cm^2\,V^{-1}\,s^{-1}$.[256] Another approach consists in removing the ligand layer of the nanoparticle film via plasma treatment[243] or UV irradiation.[195] Lin *et al.* used room temperature UV treatment to convert formerly unresponsive nanoparticle films into functional active layers, resulting in TFTs with a μ_{FE} of $\approx 10^{-3}\,cm^2\,V^{-1}\,s^{-1}$.[195] In the case of precursor-based metal oxide semiconductor devices [approach (B)], higher process temperature typically results in enhanced device performance.[224] However, a higher process temperature is only beneficial within a given material system and TFT configuration. In some cases, the choice of the semiconductor composition and of the gate dielectric is more important. For example, TFTs based on Ga-doped In_2O_3 annealed at 300 °C and SiO_2 gate dielectric exhibit $\mu_{FE} = 0.4\,cm^2\,V^{-1}\,s^{-1}$,[199] whereas devices based on In_2O_3 annealed at only 150 °C and Al_2O_3 gate dielectric yield $\mu_{FE} = 7.7\,cm^2\,V^{-1}\,s^{-1}$.[220] Combining low temperature solution-processed Al_2O_3 and combustion synthesized In_2O_3 at a maximum temperature of 225 °C, Yu *et al.* demonstrated neat crystalline In_2O_3 TFTs on PAR with a μ_{FE} as high as $22\,cm^2\,V^{-1}\,s^{-1}$.[192] Another interesting approach to realize low temperature high-performance devices has been recently reported by Lin *et al.*[228] In the work by Lin *et al.*, instead of relying on the bulk mobility of a specific semiconductor, multiple ultra-thin ($\leq 10\,nm$) layers of individual metal oxide semiconductors (either In_2O_3, Ga_2O_3 or ZnO) were deposited in different stacking sequences to form quasi-superlattice structures. The best results were obtained using a solution-processed high-ϵ_R ZrO_2 gate dielectric with an active layer sequence of $In_2O_3/Ga_2O_3/ZnO/Ga_2O_3/In_2O_3$.[228] Using this approach and a maximum process temperature of 175 °C, flexible TFTs with a μ_{FE} of $11\,cm^2\,V^{-1}\,s^{-1}$ could be realized on PEN substrates. It was found that the high μ_{FE} obtained is a result of electron confinement at the metal oxide semiconductor hetero-interfaces of the low-dimensional films. The direct light pattern (DLP) integration process proposed by Rim *et al.* has also proved to be a successful technique to realize high-performance flexible devices.[83] Using DLP and a process temperature of 350 °C, fully transparent and solution-processed TFTs with IGZO semiconductor, ITO contacts, and Al_2O_3 gate dielectric yielding a remarkably high μ_{FE} of $84\,cm^2\,V^{-1}\,s^{-1}$ were fabricated (Fig. 36). Finally, another interesting improvement approach has been demonstrated by Dai *et al.*, who proposed to utilize blends of IGZO precursor and graphene nanosheets.[201] In this study, the graphene was shown to act as a conductive filler assisting charge transport in the IGZO active layer, and thereby increasing the drain current. By keeping the graphene concentration below the percolation threshold, only the on current increases, whilst the off current is kept low. Using this technique and high temperatures of 550 °C, bendable IGZO/graphene TFTs with high-ϵ_R Ta_2O_5 gate dielectric and large $\mu_{FE} = 73.6\,cm^2\,V^{-1}\,s^{-1}$ were realized on a thin thermally stable glass substrate.[201]

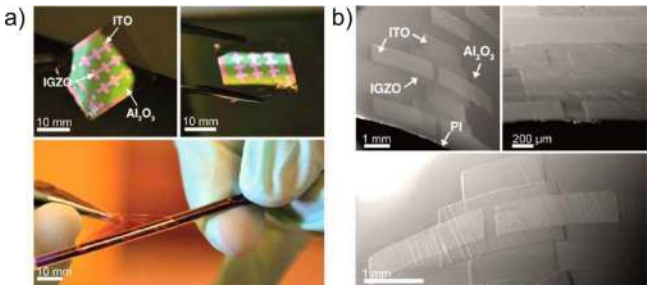

FIG. 36. Fully transparent and solution-processed IGZO TFTs on flexible PI substrate processed using direct light patterning: (a) photograph of IGZO semiconductor, ITO contacts, and Al_2O_3 gate dielectric layers, and (b) scanning electron micrographs of resulting devices. Reproduced with permission from Rim *et al.*, ACS Nano **8**, 9680 (2014). Copyright 2014 American Chemical Society.

4. Mechanical properties

Given the recent advances in low temperature solution-processing of metal oxide semiconductors, an increasing number of works on flexible n-type solution-processed TFTs has been published. However, as the field is still rather premature, often mechanical bending tests are not reported.[76,190,191,194–197,200,224,228,233] Nevertheless, some groups have presented single bending tests (tensile and compressive) at radii between 25 and 1 mm, as well as cyclic bending up to 10 000 cycles.[83,145,192,193,199,201,220–222,225,226,229,231,232] In the case of flexible TFTs with nano-scale shapes, it has been demonstrated that the application of mechanical bending causes a deformation of the particle network. In particular, tensile strain slightly increases the distance between individual particles, resulting in a lower μ_{FE}.[226] For example, tensile bending at a radius of $\leq 8.5\,mm$ leads to crack formation and early device failure in ZnO NR TFTs, whereas the same devices are fully operational down to compressive bending

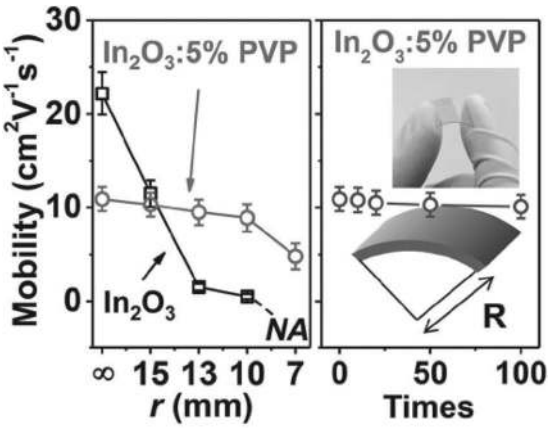

FIG. 37. Comparison of μ_{FE} for TFTs based on neat crystalline In_2O_3 and amorphous In_2O_3-poly(4-vinylphenol) (PVP) under different bending conditions, e.g., different tensile radii and bending cycles. Reproduced with permission from Yu *et al.*, Adv. Mater. **27**, 2390 (2015). Copyright 2015 John Wiley and Sons.

radius of 1.1 mm.[231] In flexible TFTs with precursor-based solution-processed semiconductors, strain-induced device failure is mainly attributed to the formation of cracks or voids in the less ductile device layers. Device failure is often caused by strain-induced breakdown in the gate dielectric layers, e.g., in SiO_2 in combination with amorphous In_2O_3:Ga[199] or thin ZnO (8 nm)[222] metal oxide semiconductor. While solution-processed Al_2O_3 layers can withstand up to 320 bending cycles without failure,[83,192] polymeric (PVP),[229] polymer-oxide hybrids (PVP with 15 nm ZrO_2),[232] or electrolyte[193] gate dielectrics are fully functional up to 10 000 repetitions. The contacts can also originate device failure, especially in the case of brittle ITO electrodes. For example, Song *et al.* attributed the failure of ZnO TFTs (50 μm PI/50 nm ITO/270 nm SiO_2/8 nm ZnO/50 nm Al) during real time bending tests (e.g., manual crumpling of the devices) to the formation of fractures in either the electrodes or the gate dielectric.[222] Device degradation in the active layer is mostly attributed to the use of crystalline metal oxide semiconductors,[192,232] or to a high number of bending cycles paired with a small bending radius.[193] The difference between amorphous and crystalline metal oxide semiconductors is illustrated in a study by Yu *et al.*, where crystalline In_2O_3 and amorphous In_2O_3-PVP were compared (see Fig. 37).[192] Compared with crystalline devices, the PVP-In_2O_3 TFTs result in improved mechanical properties: the μ_{FE} is reduced to ≈18% instead of ≈98% at a tensile bending radius of 10 mm. The difference in behavior is attributed to crack formation within the neat In_2O_3, whereas the doped layers remain crack free. Additionally, in the work by Dai *et al.*, it was shown that blending an IGZO precursor with graphene nanosheets allows improving the strain resistance.[201] While TFTs with neat IGZO result in a μ_{FE} degradation of 70% over 100 bending cycles, the μ_{FE} of IGZO/graphene devices only varies by 8%.

5. Transparency

Due to the wide band gap (E_g) of metal oxide semiconductors, the realization of flexible and transparent n-type solution-processed devices is well established. Aside from polyimide, common plastic substrate materials, metal oxide semiconductors, and also most of the gate dielectrics are transparent in the visible range. To fabricate fully transparent flexible TFTs, ITO or IZO electrodes need to be used.[196,197] Visible light transmittance of entire device stacks yields values between 76% and 81% for In_2O_3-PVP blends on PAR,[192] and In_2O_3 NW on PET substrate,[76] respectively.

III. P-TYPE OXIDE SEMICONDUCTOR TFTs

To complete the analysis of flexible metal oxide semiconductor TFTs started in Section II, in this section we present the ongoing research on flexible p-type devices based on metal oxide semiconductors. First, in Sec. III A, the available p-type metal oxide semiconducting materials are presented. Next, in Secs. III B and III C, the state-of-the-art flexible p-type TFTs based on vacuum- and solution-processed metal oxide semiconductors are reported.

A. P-type metal oxide semiconductors

In general, p-type metal oxide semiconductors are characterized by a band gap E_g ranging from 1.3 eV to 2.7 eV,[71,74] high transmittance in the visible range (>85%),[257,258] and carrier density (N) from 10^8 cm^{-3} (for NWs)[259] to 10^{15} cm^{-3} (for high-quality single crystals).[73] Already since 2005 when the first p-type TFT based on Zn-doped Ga_2O_3 (Ga_2O_3:Zn) NWs was realized by Chang *et al.*,[70] it was clear that the main limitation of p-type metal oxide semiconductors is linked to their electronic structure.[71] As already explained in Sec. II A, the majority of metal oxide semiconductors are characterized by CBM with spatially spread metal orbitals (*s*) and VBM with rather localized oxygen orbitals (2*p*).[71] This electronic structure guarantees a good electron conduction (and therefore a large electron mobility) and at the same time a bad hole transporting path (low hole mobility due to hopping conduction).[71] To date, only a few metal oxide semiconductors (e.g., SnO_x[71,72,79,257,258,260–279] and Cu_xO[73,74,267,280–294]) present a slightly different electronic structure. In particular, SnO_x is an interesting p-type semiconductor, because its VBM is formed by hybridized orbitals of localized oxygen (2*p*) and spatially spread Sn metal (5*s*).[72] SnO-based TFTs were first introduced in 2008–2009 by Ogo *et al.*,[71,72] with a $\mu_{FE} = 1.3$ cm^2 V^{-1} s^{-1} and an $I_{ON}/I_{OFF} \approx 10^2$ (at a process temperature of 575 °C). Following extensive improvements of the deposition techniques combined with deep material analysis,[257,258,260,278,295] SnO_x devices with μ_{FE} ranging from 1 to 10 cm^2 V^{-1} s^{-1} can now be reliably realized at process temperatures of ≤300 °C.[257,271–273,276,278,279] Also, Cu_xO has an interesting electronic structure, with a VBM composed by hybridized orbitals of O_2 (2*p*) and Cu metal (3*d*).[282] First, p-type Cu_2O TFTs were demonstrated by Matsuzaki *et al.* in 2008 with a $\mu_{FE} = 0.26$ cm^2 V^{-1} s^{-1} and an $I_{ON}/I_{OFF} \approx 6$ (at a process temperature above 650 °C).[73] Nowadays, p-type Cu_xO TFTs with a μ_{FE} up to 4.3 cm^2 V^{-1} s^{-1}[284] can be manufactured at process temperatures ranging from room temperature to 500 °C.[282,284,289,291] Interestingly, p-type TFTs based on bi-layers of SnO and

Cu_2O have also been shown.[296] Additionally, devices based on solution-processed SnO[268] and Cu_xO[291,293,297] have been presented. Besides SnO_x and Cu_xO, also NiO has been utilized to realize rigid p-type TFTs with modest carrier mobility.[75,298,299] Moreover, doping of n-type metal oxide semiconductors has enabled the demonstration of p-type TFTs based on P- and N-doped ZnO NW,[259,300] as well Ga_2O_3:Zn.[70] Among all the reported p-type metal oxide semiconductor TFTs,[70–75,79,257–278,280–294,300] only few devices have been fabricated on flexible substrates.[36,79,257,267,272,273,285,289] This is mainly due to the high deposition and annealing temperatures (typically $\geq$200 °C) that are required, which are incompatible with flexible temperature-sensitive substrates. This is why alternative p-type active layers that allow room temperature processing are under investigation. An interesting p-type semiconducting inorganic molecular compound is copper (I) thiocyanate (CuSCN), which is characterized by wide E_g (3.7–3.9 eV) and high optical transparency.[301] The first CuSCN devices presented by Chen and Könenkamp in 2003 were based on a flexible NW VTFT geometry.[302] Subsequently, TFTs with spin coated CuSCN layers have been demonstrated on both glass and Si rigid substrates (μ_{FE} up to 0.5 $cm^2\ V^{-1}\ s^{-1}$).[301,303]

1. Metal oxide semiconductors for flexible TFTs

Not all of the above mentioned metal oxide semiconducting materials have been employed as active layers in flexible p-type TFTs.

a. Vacuum-processed metal oxide semiconductors. For flexible devices, only SnO_x[79,257,267,272,273] and Cu_xO[285,289] active layers have been employed. Flexible SnO_x TFTs exhibit a μ_{FE} up to 5.87 $cm^2\ V^{-1}\ s^{-1}$,[257] whereas Cu_xO devices yield significantly lower performance ($\mu_{FE} \leq 0.0022\ cm^2\ V^{-1}\ s^{-1}$).[285]

b. Solution-processed metal oxide semiconductors. Even if solution-processed p-type SnO_x,[268] Cu_xO,[291,293,297] and NiO[298] TFTs have been fabricated on rigid substrates, there is no report on flexible p-type solution-processed metal oxide semiconductor devices. As already mentioned above, CuSCN offers a valid inorganic alternative and can be easily deposited by spin-coating.[301,303] In Sec. III C, we present unpublished results on flexible p-type TFTs based on spin coated CuSCN films.

B. Flexible p-type vacuum-processed TFTs

In this subsection, the materials and fabrication techniques involved in the realization of flexible p-type vacuum-processed metal oxide semiconductor TFTs are discussed. Subsequently, the electrical performance and the mechanical properties of the resulting devices are presented.

1. Materials

As already done in Section II for flexible n-type metal oxide semiconductor TFTs, here we describe the substrates, dielectric layers (barrier and gate dielectric), and conductive materials (gate and source/drain) employed to fabricate flexible p-type vacuum-processed metal oxide semiconductor TFTs.

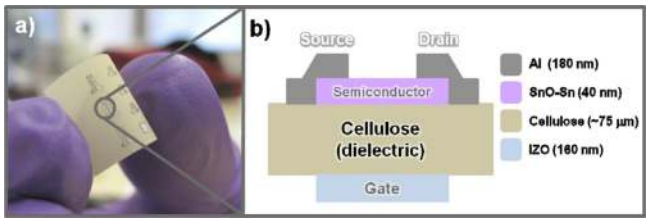

FIG. 38. Flexible p-type tin oxide (SnO_x) TFTs fabricated on and with fiber-based cellulose paper: (a) optical graph and (b) device cross-section. Reproduced with permission from Martins *et al.*, SPIE Proc. **8263**, 826315 (2012). Copyright 2012 International Society for Optics and Photonics.

a. Substrates. Also in this case, the substrates need to fulfill several requirements, such as compatibility with the fabrication process (high T_G and T_m, reduced outgassing, and chemical stability) and good mechanical properties, sometimes even combined with specific features like high transparency. Most common substrate materials are PI,[257,273] PET,[289] and PES.[285] Furthermore, also cellulose fiber-based paper (thickness of $\approx$75 μm) acting as both substrate and gate dielectric has been used (Fig. 38).[79,267,272]

b. Barrier layers. In this case, the use of barrier layers to encapsulate and electrically insulate the substrate is rare. Indeed, only Caraveo-Frescas, Khan, and Alshareef presented a PI substrate covered by 200 nm Si_3N_4.[273]

c. Gate dielectrics. The most common gate dielectrics are HfO_2,[257] Al_2O_3,[285] AlN,[289] ferroelectric P(VDF-TrFE),[273] as well as cellulose fiber-based paper.[79,267,272]

d. Contacts. For the gate contact, Al[273] as well as multi-layer metals (like Ni/Au/Ni[285]) and transparent compounds (ITO[257,289] and IZO[79,267,272]) have been used. At the same time, for source/drain metals, single (Al[267] and Au[289]) and multi-layer contacts (Ti/ITO,[257] Ti/Au,[273] and Ni/Au[79,272,285]) have been chosen.

2. Fabrication techniques

The fabrication techniques employed for p-type vacuum-processed metal oxide semiconductor TFTs are very similar to those used for n-type devices.

a. Substrate preparation. The most common substrate preparation approach is the use of free-standing flexible substrates.[79,257,267,272,273,285,289]

b. Deposition methods. The main deposition technique employed for p-type vacuum-processed metal oxide semiconductors is sputtering. SnO_x and Cu_xO are deposited by both DC[257,273,289] and RF sputtering.[79,267,272,285] One of the main concerns to ensure full compatibility of p-type metal oxide semiconductors with flexible substrates is the post-deposition annealing temperature that needs to be kept

TABLE IV. Performance parameters extracted from recently reported flexible p-type vacuum-processed metal oxide semiconductor TFTs, together with fabrication details (i.e., semiconductor deposition technique and deposition/annealing temperature).

	Semiconductor deposition	Deposition/annealing temperature (°C)	Mobility ($cm^2\ V^{-1}\ s^{-1}$)	Threshold voltage (V)	Current on/off ratio	Substrate thickness (μm)	Bending radius (mm)	Bending cycles
Cu_2O TFT with Al_2O_3 gate dielectric on PES[285]	RF sputtering	Room/150	0.0022	−4.75	…	…	…	…
SnO_x TFT with and on paper (substrate and gate dielectric)[79]	RF sputtering	Room/150	1.3	−1.4	10^2	75	…	…
SnO_x TFT with and on paper (substrate and gate dielectric)[267]	RF sputtering	Room/160	1.2	…	10^2	75	…	…
Nano-crystalline Cu_2O TFT with AlN gate dielectric on PET[289]	DC sputtering	Room/-	0.8	…	4×10^4	…	…	…
SnO_x TFT with and on paper (substrate and gate dielectric)[272]	RF sputtering	Room/160	1.3	1.4	10^2	60	…	…
SnO TFT with HfO_2 gate dielectric on PI[257]	DC sputtering	Room/150	5.87	−1	6×10^3	…	10	200
SnO TFT with ferroelectric P(VDF-TrFE) gate dielectric on PI[273]	DC sputtering	Room/200	2.51	−11.73	10^2	…	…	…

typically below 160 °C. As shown in Table IV, there is only one report where the annealing is performed at room temperature,[289] whereas all other devices require higher temperatures.[36,79,257,267,272,273,285] The deposition of gate dielectrics has been performed using ALD,[257,285] magnetron sputtering,[289] or spin-coating.[273] For the metal contacts, the main deposition techniques are e-beam evaporation,[79,257,272,285] thermal evaporation,[273] and sputtering.[257] The only barrier layer reported (Si_3N_4) has been grown by PECVD.[273]

c. Layer structuring. The pattering of the different device layers is strictly related to the substrate nature. In case of large feature sizes and chemically unstable substrates, shadow masking is used.[79,272,285] For chemically stable substrates (e.g., PI and PET), UV photolithography is chosen.[257,273,289]

d. Device configuration. Two main device configurations have been employed for flexible p-type vacuum-processed metal oxide semiconductor TFTs:

(I) Due to an easier processing, BG structures are very common.[79,257,267,272,285,289] For both coplanar and staggered configurations, the passivation layer is omitted.
(II) TG (typically coplanar) TFTs are used when fragile layers such as P(VDF-TrFE) are implemented in the device structure,[273] with the advantage of having an already passivated active layer.

3. Electrical properties

Table IV compares the electrical performance obtained for recently reported flexible p-type vacuum-processed metal oxide semiconductor TFTs. As shown in Table IV, the best DC performance (μ_{FE} up to 5.87 $cm^2\ V^{-1}\ s^{-1}$) has been achieved in fully transparent SnO TFTs on PI.[257] Such record value (achieved at a low process temperature of 180 °C) has been possible by carefully engineering the SnO phase and controlling the Sn residuals (Fig. 39).[257] The highest current on/off ratio is of 4×10^4,[289] whereas the threshold voltage ranges from −11.73 V (Ref. 273) to 1.4 V.[272] To date, no AC performance of flexible p-type vacuum-processed metal oxide semiconductor TFTs has been reported.

4. Mechanical properties

Due to the small number of publications on flexible p-type vacuum-processed metal oxide semiconductor devices,[36,79,257,267,272,273,285,289] there is only one report by Caraveo-Frescas, Khan, and Alshareef on the TFT mechanical properties.[273] In particular, in their work, Caraveo-Frescas, Khan, and Alshareef showed flexible SnO ferroelectric devices bent at a radius of 10 mm for 200 bending cycles, yielding a μ_{FE} decrease of about 20% (see Fig. 40).[273]

C. Flexible p-type solution-processed TFTs

As already explained in Secs. III A and III B, the field of flexible p-type metal oxide semiconductor TFTs is pretty

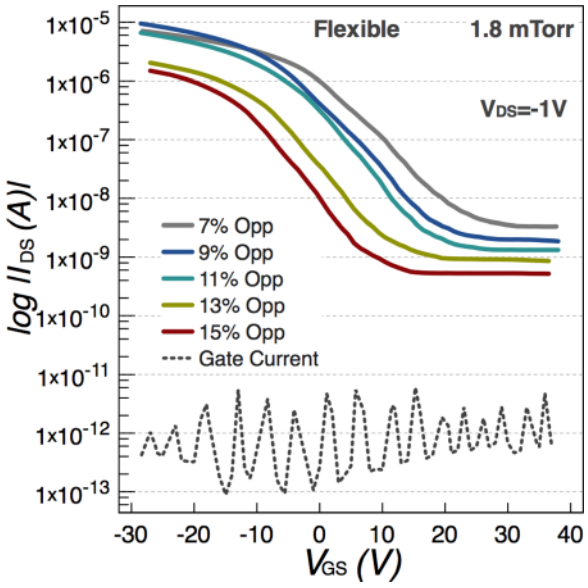

FIG. 39. Flexible fully transparent p-type SnO_x TFTs: transfer characteristics of a device with W/L = 50 μm/50 μm fabricated at different oxygen partial pressures O_{pp}. Reproduced with permission from Caraveo-Frescas *et al.*, ACS Nano **7**, 5160 (2013). Copyright 2013 American Chemical Society.

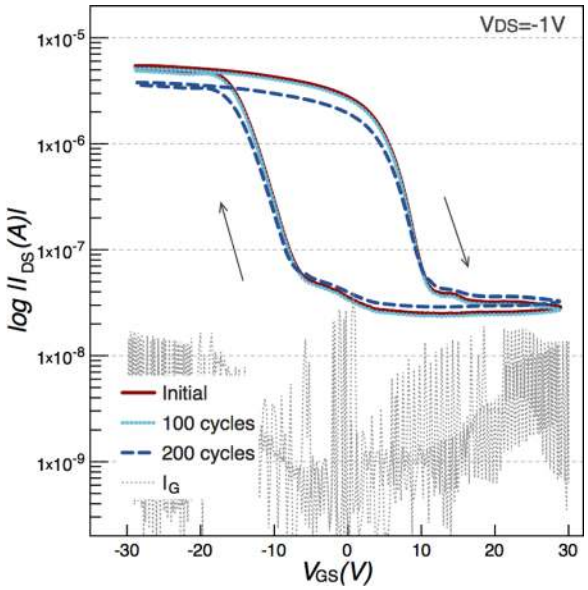

FIG. 40. Flexible p-type SnO_x TFTs with ferroelectric P(VDF-TrFE) gate dielectric: transfer characteristics demonstrating device resistance to 200 cycles of bending at a radius of 10 mm. Reproduced with permission from Caraveo-Frescas *et al.*, Sci. Rep. **4**, 5243 (2014). Copyright 2014 Nature Publishing Group.

unexplored, and there are still many challenges to be solved. No wonder that to date there is no report on flexible p-type solution-processed metal oxide semiconductor TFTs. To this aim, CuSCN represents a valid inorganic alternative to p-type metal oxide semiconductors (especially if solution-deposited). In this subsection, we present the preliminary results we have recently achieved with flexible p-type TFTs based on spin coated CuSCN.

1. Materials and fabrication techniques

Flexible BG coplanar and TG staggered CuSCN TFTs have been fabricated on 50 μm free-standing PI foils. Prior to

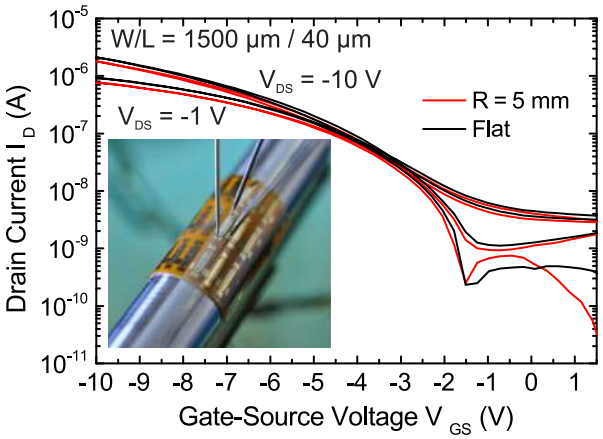

FIG. 41. Transfer characteristics of a flexible solution-processed CuSCN TFT with poly(vinylidene fluoride-trifluoroethylene-chlorofluoroethylene) [P(VDF-TrFE-CFE)] gate dielectric, measured while the device is flat and bent to 5 mm tensile bending radius. The inset shows a photograph of the flexible TFT characterized while being bent.

the TFT fabrication, 50 nm SiN_x adhesion and barrier layers have been deposited by PECVD on both sides of the substrate. Two different gate dielectrics have been employed: for the BG devices Al_2O_3 (25 nm) grown by ALD and for the TG TFTs spin coated 160 nm-thick poly(vinylidene fluoride-trifluoroethylene-chlorofluoroethylene) [P(VDF-TrFE-CFE)]. In particular, P(VDF-TrFE-CFE) is a high-ϵ_R relaxor ferroelectric polymeric dielectric that can be easily solution-processed at low temperatures.[301,304] For the solution-processed gate dielectric preparation, the P(VDF-TrFE-CFE) at 56/36.5/7.5 mol. % has been first synthesized and then dissolved in methyl-ethyl-ketone (MEK). As spin coated P(VDF-TrFE-CFE) films have subsequently been annealed at 60 °C. For both BG and TG TFTs, the active layer solution has been prepared by dissolving the CuSCN precursor in dipropylsulfide. The resulting solution has then been stirred, centrifugated, filtered, spin coated at room temperature, and annealed at 80 °C, resulting in a 15 nm thick CuSCN film. The gate electrodes have been formed by evaporated Cr (for the BG TFT) and Al (for the TG TFT), whereas the source/drain contacts have been made of evaporated Ti/Au (for the BG) and Au (for the TG). BG TFTs have been left unpassivated, while TG devices have been intrinsically passivated by the P(VDF-TrFE-CFE) gate dielectric. For the CuSCN BG TFTs, the structuring of all layers (except for the unpatterned SiN_2 and CuSCN) has been performed by standard UV photolithography. In the case of the TG devices, layer pattering of the gate and source/drain electrodes has been performed by shadow masking, whereas the P(VDF-TrFE-CFE) gate dielectric has been left unstructured.

2. Electrical properties

The flexible CuSCN BG TFTs with Al_2O_3 dielectric yield a $\mu_{FE} = 0.0013\,cm^2\ V^{-1}\ s^{-1}$, a $V_{TH} = -1\,V$, and an $I_{ON}/I_{OFF} = 5 \times 10^2$. The flexible CuSCN TG devices with solution−deposited P(VDF-TrFE-CFE) gate dielectric exhibit a $\mu_{FE} = 0.0012\,cm^2\ V^{-1}\ s^{-1}$, a $V_{TH} = -3\,V$, and an $I_{ON}/I_{OFF} = 2 \times 10^3$, combined with a small gate-induced

hysteresis (as visible from Fig. 41). Due to the high-ϵ_R gate dielectrics, both BG and TG devices can be operated at low voltages of −3.5 V and −10 V, respectively. Even if the achieved μ_{FE} is lower than the values presented for rigid devices,[301] these preliminary results are very promising especially in view of future process and device optimization.

3. Mechanical properties

Both BG and TG CuSCN devices are operational when bent down to 5 mm tensile radius and show only small strain-induced shifts (displayed in Fig. 41 for a flexible TG device). In particular, the V_{TH} changes by only −10 mV and −30 mV for BG and TG, respectively. Additionally, the hole mobility is reduced by 23% (BG TFTs) and 16% (TG TFTs).

IV. METAL OXIDE SEMICONDUCTOR-BASED CIRCUITS

In this section, metal oxide semiconductor-based electronic circuits are introduced. In Sec. IV A, an overview on basic analog and digital circuit configurations and operation is given. Next, in Sec. IV B, the state-of-the-art electronic circuits based on unipolar metal oxide semiconductors are reported. Finally, Sec. in IV C, complementary circuits based on hybrid organic/metal oxide semiconductors, as well as only on metal oxide semiconductors, are presented.

A. Circuit configuration and operation

In this subsection, the most common circuit configurations are presented, followed by an explanation of digital and analog circuit basic operation.

1. Circuit configuration

As already explained, n-type metal oxide semiconductor TFTs, compared with p-type metal oxide semiconductor devices, yield a better performance and can also be easier deposited at low process temperatures. This is why the majority of flexible (and also rigid) metal oxide semiconductor-based circuits are unipolar operating with only n-type TFTs,[94,119,127,133,143,148,159,164,166,212,213,218,305–329] whereas flexible complementary circuits based on both n- and p-type devices are less frequent.[79,103,172,272,285,330–332] Such disparity between n- and p-type devices renews an old challenge encountered in Si technology back in the 1970s and 1980s when the circuits were built using only one semiconductor polarity (n-type or p-type MOSFETs).[333] Fig. 42 displays the two main configurations using n-type TFTs (shown in the case of a logic inverter): (a) the first one is unipolar with only an n-type device and a passive (resistive) pull-up load, whereas (b) the second one is complementary with both n- and p-type devices. The main difference between the two setups occurs when a digital high level ("1") is applied at the inverter input (IN) and the n-type TFT is turned on. In this situation, there is always a current flowing through the supply voltage (V_{DD}) and the ground (GND) of the unipolar circuit (Fig. 42(a)), whereas there is no DC flow in the complementary inverter (Fig. 42(b)) due to the switched off p-type TFT.[333] The absence of a DC for a high digital input

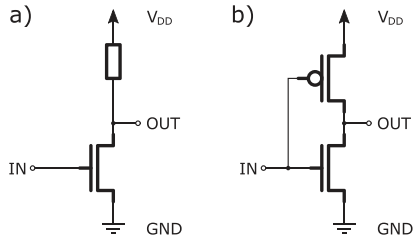

FIG. 42. The two main circuit configurations using n-type TFTs displayed in the case of a logic inverter (NOT gate): (a) unipolar with n-type TFT and passive (resistive) pull-up load and (b) complementary with both n- and p-type TFTs.

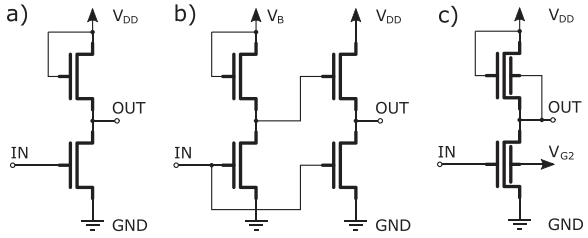

FIG. 43. Unipolar circuit configurations employing n-type TFTs and active pull-up loads displayed in the case of a NOT gate: (a) diode load, (b) pseudo-CMOS, and (c) DG.

in the complementary circuit allows achieving higher gains and lower DC power consumption. For flexible metal oxide semiconductor-based circuits, also other unipolar (NMOS) pull-up implementations are employed, as displayed in Fig. 43 (always in the case of a logic inverter). Aside from the resistive pull-up load, these three main NMOS circuit topologies are common, based on: (a) two n-type TFTs, one of which acting as a diode load (Fig. 43(a)), (b) a pseudo-CMOS circuit with two different supplies (V_{DD} and V_B) and three additional TFTs (Fig. 43(b)), and (c) a more complicated architecture with DG TFTs (Fig. 43(c)) gated at different V_{GS}.[315] Even if shown only in the case of a logic inverter, all the above mentioned configurations (Figs. 42(a) and 42(b) and Figs. 43(a)–43(c)) apply for digital as well as analog circuits. Among the three possibilities with an active pull-up, the diode load configuration (Fig. 43(a)) presents the lowest complexity and area occupation, at a cost of a lower performance if compared with the pseudo-CMOS and DG configurations (Figs. 43(b) and 43(c)).[315] In contrast, the pseudo-CMOS and DG configurations yield better performance (especially gain) at the cost of larger area occupation and more complicated fabrication processes. Despite the improved gain of both pseudo-CMOS and DG configurations, the (DC) power consumption is not reduced with respect to the diode load. The high power budget necessary for unipolar circuits is further increased in the case of flexible unipolar metal oxide semiconductor-based circuits by the use of typical V_{DD} in the range of 5 V to 20 V,[143,159] with some circuits operated at up to 50 V.[314]

2. Circuit operation

In Secs. IV B and IV C, flexible digital and analog metal oxide semiconductor-based circuits employing unipolar or complementary configurations are reviewed. To simplify the understanding of these subsections, we provide first an

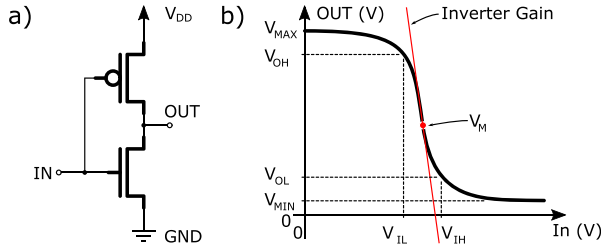

FIG. 44. Complementary NOT gate: (a) device schematic and (b) static (DC) voltage transfer characteristics (VTC).

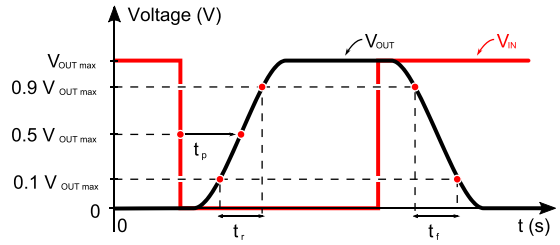

FIG. 45. Transient characteristics of a complementary NOT gate with an ideal input voltage.

overview of the main performance parameters of digital and analog circuits.

a. Digital circuits. Fig. 44 displays the simplest and most straightforward example of a digital circuit, a voltage inverter (also known as NOT gate). The NOT gate is given in its complementary configuration, with both n- and p-type TFTs, but it can be realized in all the other unipolar circuit configurations shown in Figs. 42(a) and 43. The inverter function consists of taking the voltage signal applied at its input, inverting its voltage levels, and providing the inverted signal at its output (OUT), as illustrated by its IN-OUT curve (see Fig. 44(b)), also known as DC voltage transfer characteristics (VTC). From the VTC of a NOT gate, several specific DC parameters can be defined (see Fig. 44(b)):

- Voltage input low (V_{IL}), which is the lowest input voltage where the slope of the VTC equals −1,
- voltage input high (V_{IH}), which is the highest input voltage where the slope of the VTC equals −1,
- voltage output high (V_{OH}), which corresponds to the output voltage at V_{IL},
- voltage output low (V_{OL}), which corresponds to the output voltage at V_{IH},
- maximum output swing (V_L), which is given by V_{OH}–V_{OL}, and
- midpoint voltage (V_M), which is the input voltage at which the NOT gate yields the same input and output level. Ideally, V_M should be equal to $V_{DD}/2$.

Additionally, from the VTC also the maximum and the minimum output voltages, V_{MAX} and V_{MIN}, respectively, can be extracted. Other important parameters are the DC noise margins (NMs): the high (NM_H) and the low (NM_L) noise margin, which are the voltage ranges ensuring that a logic "0" or "1" is interpreted correctly also by a second inverter connected in cascade to the first one. They are defined as follows:

$$NM_L = (V_{IL} - V_{OL}), \tag{4.1}$$

$$NM_H = (V_{OH} - V_{IH}). \tag{4.2}$$

Another important DC parameter is the gain (G), which is the slope of the VTC when $V_{IN} = V_M$. High noise margins and gain, together with a nearly "rail-to-rail" output ($V_L \approx V_{DD}$), are desirable. Together with the DC voltage transfer characteristics, also the transient behaviour is important to determine various time constants, such as the rise and fall times (t_r and t_f, respectively), as well as the propagation delay t_p (Fig. 45). As visible in Fig. 45, in a NOT gate (and in any other digital circuit), there is always a delay between the switching of the input and the output signal. For instance, t_r (t_f) is defined as the time needed for the output signal to switch from a logic "0" ("1") to a logic "1" ("0") (usually measured between the 10% and 90% of the output levels). The t_p is the time required for an output signal to change given a specific input transition (usually measured at the 50% levels of input and output voltage). The maximum switching speed of a larger digital gate is typically measured with ring oscillators (ROs), i.e., digital test circuits comprising an odd number of NOT gates (the so-called delay stages) connected in a closed loop chain. Such configuration results in an output signal oscillating between the two limits (HIGH and LOW) at an oscillation frequency (f_o) that depends on the number of delay stages (m) and the propagation delay t_p of each stage[334]

$$f_o = \frac{1}{2 \cdot m \cdot t_p}. \tag{4.3}$$

Another important parameter is the ring oscillator stage delay, which is simply the double of the t_p. Finally, the dynamic power consumption P is given by[335]

$$P = f_o \cdot C \cdot V_{DD}^2, \tag{4.4}$$

where C is the sum of the capacitances at the output node.

b. Analog circuits. The simplest flexible metal oxide semiconductor-based analog circuit is a single-stage common-source (CS) amplifier (see Fig. 46(c)),[81,106,113] which acts as a voltage or transconductance amplifier. Flexible metal oxide semiconductor-based common-source amplifiers (as well as all other amplifier types) are usually designed in an unipolar configuration with an active n-type TFT (mainly IGZO) and different pull-up loads (see Figs. 42(a) and 43).[81,106,113,212,213,305,313,318–321,323,329] The dynamic performance of a common-source amplifier (and of any other type of amplifier) is evaluated using the so-called Bode plot (amplitude and phase) shown in Figs. 46(a) and 46(b), which is a standard format for plotting the circuit frequency response.[336] On the horizontal axis, the frequency of the input voltage is in logarithmic scale, whereas on the vertical axis the amplitude and phase of the output voltage are, respectively, in decibel (dB) and degrees (deg). The amplitude of the amplifier in dB (A_{dB}) is given by following formula:

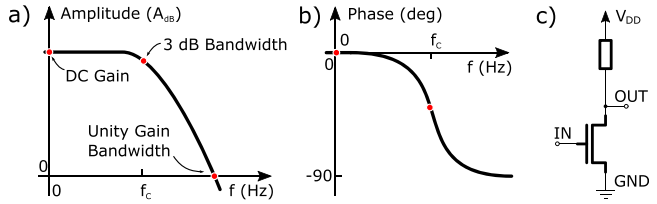

FIG. 46. Analog amplifiers: typical Bode plots of the (a) amplitude and (b) phase, as well as (c) schematic of the simplest analog amplifier (a single-stage common-source amplifier in unipolar NMOS technology).

$$A_{dB} = 20 \cdot \log_{10} \cdot \frac{V_{out}}{V_{in}}, \tag{4.5}$$

where V_{in} and V_{out} are the amplifier input and output voltage, respectively. The Bode plot allows extracting several key circuit parameters:

- The DC gain (G), which is given by the amplifier amplitude at low frequencies,
- the cutoff frequency (f_c), which is the frequency at which A_{dB} drops by 3 dB (−30%), and
- the gain bandwidth product (GBWP), which is also called unity gain bandwidth as it is the frequency at which the amplification falls to unity.

For feedback configurations (e.g., operational amplifiers), instead of the DC gain, the open-loop gain G_{OL} (i.e., the gain obtained in absence of feedback) is employed.

B. Flexible unipolar circuits

In this subsection, the state-of-the-art flexible unipolar metal oxide semiconductor-based circuits (digital and analog) are revised. First of all, the materials and the fabrication techniques employed are reported, followed by the presentation of the electrical and mechanical properties of both digital and analog metal oxide semiconductor-based circuits.

1. Materials and fabrication techniques

Flexible metal oxide semiconductor-based circuits are typically unipolar, mainly based on n-type vacuum-deposited IGZO[150,151,212,312] or ZnO active layers.[328] Solution-processed metal oxide semiconducting materials are only rarely used for circuits, and in any case only for unipolar inverters or ring oscillators.[119,193,200,220,221,231] As gate dielectrics Al_2O_3 or SiO_2 are mostly utilized, whereas source and drain electrodes are typically made of different metals like Au, Ti, Cr, and Cu, which can even be treated with special techniques (e.g., hydrogen plasma treatments) to reduce the contact resistance.[316] Most common substrates are PI, PET, PEN, and parylene.

2. Electrical properties

In the following, we revise the electrical properties of flexible unipolar metal oxide semiconductor-based circuits. In particular, the circuit simulation and the modeling are first presented, followed by the experimental results obtained for both digital and analog circuits.

a. Simulation and modeling. The development of fully flexible TFT-based circuits requires a complete simulation of the AC and DC electrical performance, together with a precise modeling of the device mechanical properties. To this aim, the device DC characteristics needs to be extracted from the transfer and output curves measured for the fabricated TFTs.[213] Additionally, it is also important to obtain the AC characteristics of the TFTs by measuring the device S-parameters and subsequently extracting the f_T, as explained in Section II.[112] In this way, by fitting the coefficients of a TFT model to the measured DC and AC characteristics, the performance of the circuits can be simulated before fabrication. Typical models used for such simulations are HSpice templates,[212,213,305] which can then be used in commercial circuit design tools for circuit analysis. One example of such a HSpice model is shown by Perumal *et al.*, who fitted the model coefficients to the input, output, and frequency measurements of a fabricated IGZO TFT (see Fig. 21).[213] Nevertheless, the model by Perumal *et al.* is only valid for channel lengths down to 3.6 μm, with smaller channels needing an adaption of the coefficients. To prove the validity of this model, Perumal *et al.* also demonstrated that a simulated 2-stage cascode amplifier behaves like the measured one.[213] Similarly, Zysset *et al.* used a HSpice model to predict the performance of an IGZO-based operational amplifier prior to circuit fabrication. In particular, Zysset *et al.* also noticed the importance of modeling the parasitic capacitances caused by the pads and trace crossings at different layers of the circuit.[212] In contrast to the electrical modeling of the circuits (which has been extensively investigated), the influence of mechanical bending has rarely been taken into consideration in the circuit design. Nevertheless, strain-induced effects should definitively be included in the TFT modeling, especially considering that μ_{FE} and V_{TH} change by ≈2.5% and SI20–200 mV for $\epsilon = 0.5\%$, respectively.[84,90,144,148,150,151,156,172] Such changes can impact especially the performance of analog circuits and should be taken into consideration during the design process. To date, only Ma *et al.* have shown a HSpice-based simulator, which is able to include the threshold voltage variations induced by mechanical strain, as well as by process modifications and aging.[217]

b. Digital circuits. The majority of flexible metal oxide semiconductor-based circuits is constituted by NOT gates[143,159,193,231,312] and test structures like ring oscillators.[119,143,159,164,200,220,221,314] Flexible unipolar vacuum-processed IGZO NOT gates on PI employing diode load pull-ups can typically achieve gains up to 2.5 V/V at 20 V supply (voltage output swing $V_L \approx 17.5$ V).[159] Similarly, vacuum-processed ZnO NOT gates on PI foils with gains of 1.5 V/V at supply voltages of only 9 V have also been demonstrated.[328] Additionally, also NOT gates with resistive pull-up loads employing solution-processed metal oxide semiconductors have been reported, like ion-gel gated ZnO NR NOT gates on paper yielding gains of 2 V/V at supply voltages of 1.3 V,[231] and aerosol-jet printed ZnO NOT gates on PI with gains up to 8 V/V ($V_{DD} = 2$ V).[193] Interestingly, Karnaushenko *et al.* demonstrated that IGZO-based NOT (and NAND) gates able

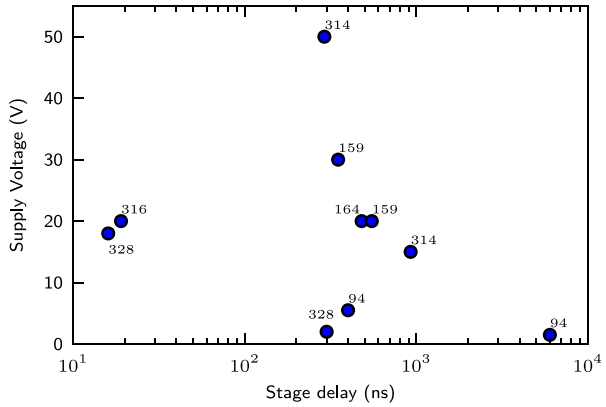

FIG. 47. Flexible ring oscillators (ROs): stage delay with respect to the circuit supply voltage V_{DD} for a number of published ROs employing IGZO or ZnO TFTs.[94,159,164,314,316,328]

to roll up to a radius of 25 μm after fabrication and release.[23] Recently, also 2 TFT/1 Capacitor (2T1C) display drivers based on IGZO devices on PEN or PI foils and capable of driving OLED pixels at a frame rate of >60 Hz have been shown.[127,316] Compared with NOT (and NAND) gates and 2T1C drivers, ring oscillators typically employ a larger number of TFTs. Fig. 47 displays the stage delay (with respect to the supply voltage) obtained for a number of published flexible ring oscillators based on vacuum-deposited metal oxide semiconductors. As shown in Fig. 47, the lowest stage delay has been reported for ZnO ring oscillators, which yield a 16 ns delay at 18 V supply voltage.[328] Already at 2 V supply voltage, the delay of the same ring oscillators increases to ≈300 ns.[328] The smallest ring oscillator is composed by 3 stages of IGZO TFTs on a metal foil and oscillates at $f_o = 360$ kHz (stage delay of 926 ns) with a supply voltage of 15 V.[314] Increasing the supply voltage to 50 V raises the oscillation frequency to 1.14 MHz and results in a stage delay of 291 ns.[314] A larger IGZO ring oscillator (5 stages) oscillating at 182 kHz at 20 V (stage delay of 550 ns) and at $f_o = 572$ kHz at 30 V (stage delay of 350 ns) has been reported by Hsieh and Wu on PI foil.[159] Such a low stage delay is partially a result of the use of a substrate with a high $T_G \approx 350\,^{\circ}C$, allowing a high temperature annealing of the IGZO film (and therefore an improved TFT performance).[159] For display applications, flexible metal oxide semiconductor-based shift registers are also commonly utilized. Mativenga *et al.* reported a 5 IGZO TFT shift register (operated at 19.7 V) yielding a rise time t_r of 0.9 μs and a fall time t_f of 0.8 μs based on 15 μm colorless PI.[133] Interestingly, Nelson and Tutt presented 7-stage ring oscillators based on flexible ZnO VTFTs with 400 ns stage delay at 5.5 V supply voltage (and 6 μs at 1.5 V).[94] Flexible 7-stage ring oscillators based on solution-processed metal oxide semiconductors have also been reported recently,[119,220,221] with the smallest delay of ≈100 ns (at 15 V V_{DD}) obtained for sol-gel In_2O_3 ring oscillators on PI.[220] Even more stages (11) have been shown by Mativenga *et al.*, who demonstrated an IGZO ring oscillator working at 94.8 kHz at 20 V, resulting in a stage delay of 480 ns on PI or PET substrates.[164] The same publication also presented a two clock shift register with 10 TFTs and 1 Capacitor per stage, which is suitable for display

	[This] Diode-load	[This] Dual-gate M2	[This] Dual-gate M3	[This] Pseudo CMOS
# TFTs/inv	2	2	2	4
Footprint inverter [μm²]	19350	40300	19350	65812
Chip area transponder [mm²]	2.70x2.98 (8.046)	3.91x3.87 (15.132)	2.70x3.14 (8.478)	4.69x3.36 (15.759)
# TFTs	218	218	218	436
# supplies	2	3	3	3
# litho	6	6	8	6
NM	Lowest <7.4% VDD/2	Tunable, ~36% VDD/2	Tunable, ~40% VDD/2	Tunable, ~24% VBIAS/2
Max. data rate	71.6kbit/s	11.3kbit/s	25.8kbit/s	43.9kbit/s
Substrate	Foil	Foil	Foil	Foil

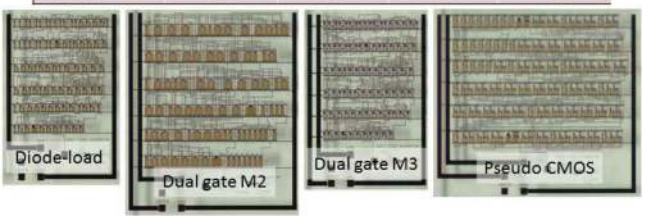

FIG. 48. Flexible near field communication (NFC) code generator: different realizations with three different active pull-up load configurations (diode load, pseudo-CMOS, and DG) based on 218–436 flexible IGZO TFTs. Reproduced with permission from Myny *et al.*, in *IEEE Int. Solid-State Circuits Conf.* (*ISSCC*) (2015), pp. 294–296. Copyright 2015 Institute of Electrical and Electronic Engineers.

applications.[164] Further increasing the number of stages, Zhao, Mourey, and Jackson showed a ZnO 15-stage ring oscillator with 16 ns delay at 18 V and 300 ns delay at 2 V.[328] The realization of a flexible 19-stage IGZO ring oscillator with a stage delay of 19 ns at 20 V has only been possible due to the low TFT contact resistance achieved between source/drain and IGZO.[316] Even more TFTs have been utilized for an AMOLED line driver based on IGZO capable of 45 frames/s at 11 V on PEN foil, which has also been integrated with an optical display (64 × 160 pixels) and a 2T1C pixel driver circuit.[309,310] At a supply voltage of 15 V, the flexible line driver consumes a power of ≈97 μW.[309,310] Similarly, Zhang *et al.* reported a 48 stage scan driver based on IGZO with a output swing of 16 V at 100 kHz.[187] Even larger TFT count has been reported in combination with RFID or near field communication (NFC) applications. For example, Myny *et al.* demonstrated an IGZO-based NFC tag consisting of an high frequency (HF) capacitor, a 19-stage ring oscillators acting as a clock source, a 4-bit modulo-12 counter, a 12-bit decoder, and a several out registers and buffers all integrated on the same foil and laminated on top of an antenna coil.[315] The flexible NFC code generator is capable of transmitting data at 71 kB s^{-1}, given enough supply voltage.[315] Based on this design, three different pull-up load configurations (diode load, pseudo-CMOS, and DG) have been compared, as shown in Fig. 48.[315] The TFT count ranges between 218 and 436 TFTs.[315] Similarly, Tripathi *et al.* demonstrated an IGZO-based RFID code generator (8-bit) operating at 6.4 kB s^{-1} (2 V supply voltage) fabricated on PEN foil. The RFID code generator by Tripathi *et al.* is constituted by 300 flexible IGZO TFTs, resulting in an occupied area of 51.7 mm^2.[325] The most recent work on RFID circuits by Myny and Steudel demonstrated an

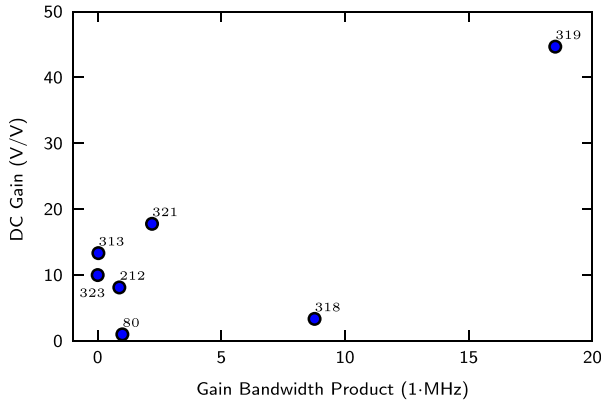

FIG. 49. DC gain versus gain bandwidth product (GBWP) of recently reported flexible metal oxide semiconductor-based analog amplifiers.[80,212,313,318,319,321,323]

NFC transponder with 438 IGZO TFTs on a polyimide foil (occupied area of 10.884 mm^2). With a data rate larger than 14.3 kB s^{-1} and at most 396.5 kB s^{-1}, the circuit by Myny and Steudel complies with the ISO 14443 NFC standard.[138]

c. Analog circuits. Compared with the digital metal oxide semiconductor-based circuits, analog circuits present a completely different TFT count and total area: the largest number of TFTs is of 16 (reported for an IGZO operation amplifier),[212] whereas the largest occupied area is of 9.83 mm^2 (also shown for an operational amplifier constituted by 13 IGZO TFTs).[313] To date, the variety of flexible metal oxide semiconductor-based analog circuits reported ranges from single- to multiple-stage (e.g., common-source,[113] transimpedance,[329] differential,[80,323] cascode,[318,321] operational,[212,313] and Cherry-Hooper[319]) amplifiers, which at the same time often also include biasing circuits like current mirrors.[212] Similarly, new analog functions such as antenna channel select circuits,[337] X-ray readout circuits,[338] and digital to analog converters (DAC)[339] have been implemented recently. However, the majority of the published circuits are amplifiers. Fig. 49 shows a comparison of the GBWPs (with respect to the DC gain) of recently reported flexible metal oxide semiconductor-based analog amplifiers. As shown in Fig. 49, the highest DC gain of 44.67 V/V (33.3 dB) and GBWP of 18.5 MHz have been achieved by Shabanpour *et al.* for a self-aligned IGZO TFT-based Cherry-Hooper amplifier on PI foil.[319] Apart from this example,[319] all other metal oxide semiconductor-based amplifiers show DC gains of $\leq$20 V/V (10 dB) and GBWP of $\leq$2.2 MHz. Flexible IGZO-based common-source amplifiers yield a DC gain of 6.8 dB and a cutoff frequency $f_c = 1.2$ MHz.[113] Similarly, transimpedance amplifiers (with a single active IGZO TFT) yield a DC gain of 86.5 dB Ω at a cut-off frequency of 8.38 kHz (when supplied at 5 V).[329] Tai *et al.* utilized 2 flexible IGZO DG TFTs to realize a flexible differential amplifier with 20 dB DC gain at a cut-off frequency of $\approx$300 Hz ($V_{DD} = 10.5$ V).[323] A similar IGZO amplifier with lower DC gain of 2 dB and higher cutoff frequency of $\approx$1 MHz has also been fabricated on a 1 μm parylene foil.[80] Similarly, Shabanpour *et al.* presented a flexible IGZO-based cascode amplifier with a DC gain of 10.5 dB and a

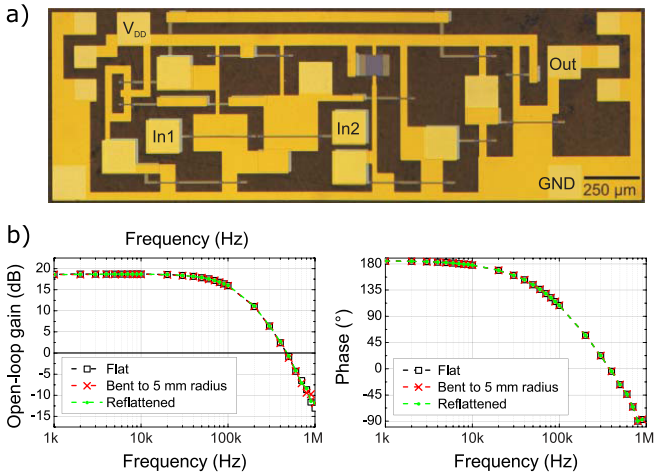

FIG. 50. Flexible operational amplifier with 16 IGZO TFTs: (a) micrograph and (b) corresponding Bode plot. Reproduced with permission from Zysset *et al.*, IEEE Electron Device Lett. **34**, 1394 (2013). Copyright 2013 Institute of Electrical and Electronic Engineers.

cutoff frequency of 2.62 MHz (GBWP $\approx$8.8 MHz) at 6 V supply. The cascode amplifier by Shabanpour *et al.* consumes 762 μW power during standard operation.[318] A second version of this cascode amplifier shows a higher DC gain (25 dB) at the cost of a lower cut-off frequency of 220 kHz, consuming 2.32 mW power at 6 V.[321] Even more TFTs (13 IGZO devices) have been utilized in an operational amplifier with a GBWP of 31 kHz and an open-loop gain G_{OL} of 22.5 dB, resulting in a $f_c = 5.6$ kHz.[313] Furthermore, this operational amplifier consumes 160 μW power during standard operation.[313] Similarly, Shabanpour *et al.* showed a 2-stage Cherry-Hooper amplifier yielding a DC gain of 33 dB at a cutoff frequency of 400 kHz, resulting in a GBWP of 18.5 MHz based on IGZO TFTs.[319] The Cherry-Hooper amplifier (supplied at 6 V) consumes 4.96 mW power.[319] Chung *et al.* realized an alpha particle detecting circuit by AC coupling 4 different stages of amplification with 14 active IGZO TFTs.[308] The circuit by Chung *et al.* yields a linear DC gain of 14.9–20 V/V and a band-pass characteristic.[308] In a similar fashion, simulations of different band-pass topologies have been shown by Bahubalindruni *et al.* with DC gains of up to 75 dB and cut-off frequencies in the order of 25 MHz.[305] The flexible metal oxide semiconductor-based analog circuit with the largest TFT count is an operational amplifier with 16 IGZO TFTs. This amplifier is supplied at 5 V and presents a DC gain of 18.2 dB at a cut-off frequency of 108 kHz (see Fig. 50).[212]

3. Mechanical properties

The realization of reliable flexible (and bendable) metal oxide semiconductor-based circuits is challenged by the dimensional instability of the flexible substrates (e.g., expansion/shrinking occurring during the fabrication process). Due to the substrate deformation, large tolerances are necessary while aligning the different device layers (especially gate with respect to source/drain electrodes). Therefore, the maximum operating frequency of the circuit, as well as the total circuit area, is limited. Another key challenge in the

realization of flexible circuits is constituted by the mechanical strain that is induced in the flexible TFT channels when the substrate is bent. As already explained, the goal is the fabrication of flexible metal oxide semiconductor-based circuits as strain resistant as possible, and at the same time also with the smallest strain-induced performance parameter variations. Regarding strain resistance, as shown in Equation (2.1), the minimum bending radii depend directly on the thickness of the substrate, as well as on the other device layers (materials and thicknesses). Depending on the device layer stack and thickness, the typical bending radii range from 30 mm (Ref. 159) down to 50 μm (demonstrated for a differential amplifier on 1 μm parylene substrate).[80] While strain resistance limits the application range of the circuits, strain-induced TFT performance parameters can severely compromise the circuit functionality, especially when the occupied area is large (as for digital circuits). Prior to the circuit fabrication, it is indeed important to account for the bending-induced variations each single TFT is subjected to by simulating the mechanical TFT behaviour and by modeling/designing the circuit topologies. In particular, there are several approaches that allow mitigating strain-induced performance variations. First, all the TFTs can be aligned parallel to each other in order to present the same strain-induced variations, as well as resistance for bending all over the circuit structure.[143] This approach has been first proposed by Münzenrieder *et al.*, who demonstrated that 5-stage ring oscillators constituted by IGZO devices all aligned parallel to each other show only small performance decrease when mechanically bent to $\epsilon = 0.72\%$.[143] By aligning parallel to each other all the 40 TFTs of a 8-stage 5 TFT shift register, Mativenga *et al.* demonstrated an almost negligible parameter shift of the circuit down to radii of 4 mm.[133] Moreover, by employing a 25 μm-thick PEN foil and an encapsulation layer shifting the neutral strain axis close to the TFT stack, Tripathi *et al.* realized an 8 bit code generator yielding negligible parameter shift for tensile bending at a radius of 2 mm.[326] Additionally, also the circuit design can be selected in a way to achieve a performance based on the ratio of the same TFT performance parameters. Such approach applies especially for analog circuits, which can be designed to yield a gain depending only on the ratio of the transconductance of the different TFTs and not on a single transconductance. Using this technique for an operational amplifier based on 16 IGZO all aligned parallel to each other, Zysset *et al.* realized a flexible circuit yielding a strain-independent DC gain and bandwidth (at a radius R = 5 mm).[212]

C. Flexible complementary circuits

All the results presented in Sec. IV B have been obtained with unipolar circuits, employing mainly flexible n-type vacuum-processed metal oxide semiconductor TFTs. Even if excellent performance can be achieved with unipolar circuitry, key issues such as low-power consumption, as well as easy and compact circuit design can only be accomplished by complementing n- with p-type TFTs. Nevertheless, to realize flexible metal oxide semiconductor-based complementary circuits, flexible n- and p-type devices with similar performance (especially mobility) are required. This is particularly challenging in the case of metal oxide semiconductors, due to the typically low carrier mobility values obtained for flexible p-type devices (see Section III). For this reason, only few groups have reported flexible complementary circuits (mainly digital gates) based on both n- and p-type metal oxide semiconductor TFTs.[79,177,272,285] To overcome this bottleneck, other technologies have been considered to realize the p-type channel. For instance, organic semiconductors have well-known hole transporting properties, with sufficient carrier mobility. Thus, different combinations of p-type organic TFTs with n-type metal oxide semiconductor devices have so far been demonstrated on flexible substrates.[103,172,330–332,340–342] In the following, the materials and fabrication techniques, the electrical and the mechanical properties of flexible complementary circuits based on both fully metal oxide semiconducting materials, as well as hybrid organic-metal oxide semiconductors are reviewed.

1. Materials and fabrication techniques

The materials and fabrication processes employed for flexible complementary metal oxide semiconductor-based circuits are similar to the materials and techniques mentioned previously, except that the channel is made by two different semiconducting materials. Common substrates used for flexible complementary circuits include: paper,[79,272] PES,[285,330,331,340] PI,[103,172,177,332,343,344] PET,[341,342] and PDMS.[332] In addition to the substrate, sometimes a barrier, buffer, or encapsulation layer is deposited in order to improve electrical isolation, decrease surface roughness, and increase stability, like inorganic SiN_x adhesion layers[103] and organic Cytop[103] or AZ1518 (Ref. 103) encapsulation films. Most widely used gate dielectrics for flexible complementary circuits are AlO_x,[330] Al_2O_3,[103,285,332,340,343,344] paper,[79,272] SiO_x,[332,343,344] PVP,[172] Si_3N_4,[331] and HfO_2.[177] As metal oxide semiconductors provide good n-type transport, the n-channel is always made of a metal oxide semiconductor deposited via RF-magnetron sputtering[79,103,172,177,272,285,330–332,340–344] or spray pyrolysis[103,145] on flexible substrates at compatibly low temperatures. Best performing n-type metal oxide semiconductors include IGZO,[79,103,172,272,285,331,332,340–344] ZnO,[177,330] and In_2O_3.[103,145] On the other hand, the p-channel is either formed by a metal oxide[79,272,285] or an organic semiconducting material.[103,172,330–332,340–344] As p-channel metal oxide semiconducting materials, till now only SnO_x[79,177,272] and Cu_xO[285] deposited by RF-magnetron sputtering have been employed. In the case of organic p-type semiconductors, several materials have been used, employing solution-processable, low temperature, scalable, and cost-effective techniques such as ink-jet printing,[341,342] spin-coating,[103] and dip-coating,[332,343,344] in addition to the widely used thermal evaporation with shadow masking.[172,330,331,340] Different groups have so far demonstrated the potential of integrating p-type pentacene,[172,330,331,340] poly-(9,9-dioctyl-fluorene-co-bithiophene) (F8T2),[341,342] and semiconducting single walled carbon nanotubes (SWCNTs)[103,332,343–345] with n-type ZnO,[330] In_2O_3,[145] and IGZO.[103,172,331,332,340–344]

2. Electrical properties

Compared with unipolar circuits, the range of the reported flexible complementary metal oxide semiconductor-based circuits is smaller. The majority of the published complementary circuits are digital, especially NOT, NAND, and NOR gates, and ring oscillators based both on p- and n-type metal oxide semiconductors and on hybrid p-type organic and n-type metal oxide semiconducting materials. Additionally, also two common-source amplifiers and one differential amplifier have been reported.[272,343]

a. Digital circuits. The first example of flexible complementary metal oxide semiconductor-based circuit is dated 2008, when Oh *et al.* demonstrated the integration of pentacene and ZnO TFTs to realize a complementary NOT gate on PES with a gain of 100 V/V and a low voltage operation.[330] The dynamic behavior of the hybrid pentacene/ZnO complementary NOT gate shows an f_o of 5 Hz.[330] In 2010, Kim *et al.* demonstrated a pentacene/IGZO NOT gate on PES with a gain up to 165 V/V centered at $V_M = 14$ V ($V_{DD} = 30$ V).[331] In 2011, Kim *et al.* reported vertically stacked pentacene/IGZO NOT gates.[340] Furthermore, the same group also showed bendable pentacene/IGZO NOT gates.[172] Alternatively to pentacene devices, Nomura *et al.* exploited p-type F8T2 TFTs in a vertically stacked geometry on top of ZnO devices, employing a common gate electrode on PET.[342] The F8T2/IGZO NOT gate shows a gain G = 100 V/V at a maximum supply of 30 V.[342] The same group realized also vertically stacked F8T2/IGZO NAND gates on PET.[341] In 2011, the first fully metal oxide semiconductor-based NOT gates have been presented, employing n-type IGZO and either p-type CuO_x[285] or SnO_x.[79] In particular, Dindar *et al.* presented vertically stacked CuO_x/IGZO NOT gates on PES, yielding a high gain of 120 V/V with a nearly "rail-to-rail" output swing.[285] Employing n-type IGZO and p-type SnO_x TFTs on a flexible paper substrate (acting also as gate dielectric), Martins *et al.* showed NOT gates with a maximum G = 4.5 V/V at V_M of 3.6 V ($V_{DD} = 17$ V).[79] This structure has been later improved with an optimized geometric aspect ratio $(W/L)_p/(W/L)_n$, which enabled also the realization of NAND and NOR logic gates.[272] Li *et al.* recently demonstrated a flexible 5-stage ring oscillator based on n-type ZnO TFTs and p-type SnO_x TFTs, with a maximum oscillation frequency of 18.4 kHz.[177] Recently, solution-processed semiconducting SWCNTs have also been exploited as p-type TFTs[345] and integrated into flexible complementary circuits with n-type sputtered IGZO[103,332,343,344] or spray coated In_2O_3 TFTs.[145] Bendable hybrid SWCNT/IGZO NOT gates on PI show a maximum gain of 87 V/V, a nearly perfectly centered V_M, and a "rail-to-rail" V_L (Fig. 51).[103] In addition, Petti *et al.* exploited also the use of spray coated In_2O_3 as n-type semiconductor and presented SWCNT/In_2O_3 NOT gates with a lower gain of 22 V/V.[145] The reduced performance of the SWCNT/In_2O_3 NOT gates is attributed to the poorer performance of the solution-deposited In_2O_3 active layers. Using SWCNT and IGZO TFTs, Chen *et al.* successfully realized large-scale complementary circuits (NOT, NAND, and NOR gates, as well as ROs) on PDMS comprising a large TFT count.[332] Figs. 52(a) and 52(b) show the optical micrograph and output characteristic of the 501-stage hybrid SWCNT/IGZO complementary RO with up to 1004 TFTs, yielding an f_o of 294 Hz.[332] Finally, Honda *et al.* presented bendable NOT, NAND, and NOR gates based on SWCNT and IGZO TFTs on PI.[344] The SWCNT/IGZO NOT gate shows a gain of 45 V/V and a low $t_r = 0.75$ ms.[344] The same group also realized 3D vertically integrated SWCNT/IGZO NOT gates with similar performance.[343]

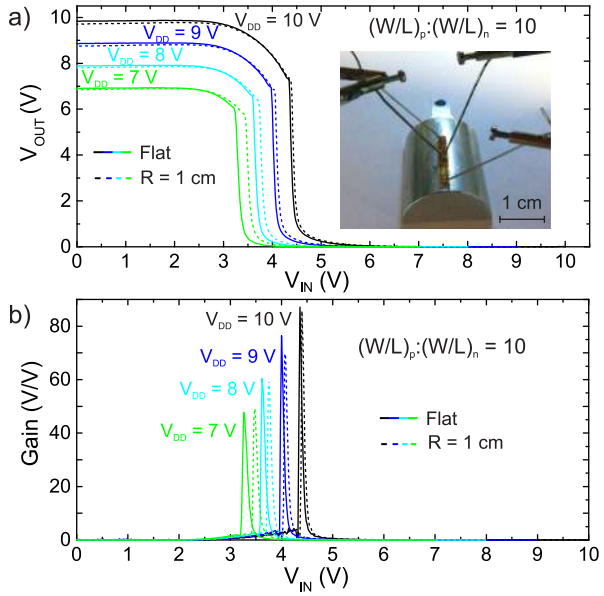

FIG. 51. Flexible complementary single walled carbon nanotubes (SWCNTs)/IGZO NOT gate: (a) VTC and (b) gain (G), showing a maximum G = 87 V/V for a supply voltage $V_{DD} = 10$ V at a bending radius of 10 mm. The inset displays a photograph of the contacted and bent NOT gate. Reproduced with permission from Petti *et al.*, in *IEEE Int. Electron Devices Meet.* (*IEDM*) (IEEE, 2014), pp. 26.4.1–26.4.4. Copyright 2014 Institute of Electrical and Electronic Engineers.

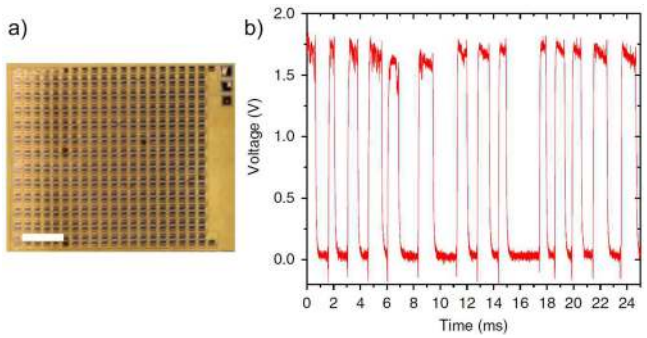

FIG. 52. Flexible complementary SWCNT/IGZO 501-stage RO: (a) optical micrograph and (b) output characteristic at an oscillation frequency of 294 Hz. Reproduced with permission from Chen *et al.*, Nat. Commun. **5**, 4097 (2014). Copyright 2014 Nature Publishing Group.

b. Analog circuits. As regards flexible metal oxide semiconductor-based analog circuits, Martins *et al.* reported common-source and differential amplifiers (see Fig. 53), respectively, with gains of 16.3 V/V and 4.1 V/V, based on the same optimized device structure employed to realize the SnO_x/IGZO NOT, NAND, and NOR gates on (and with) paper.[272]

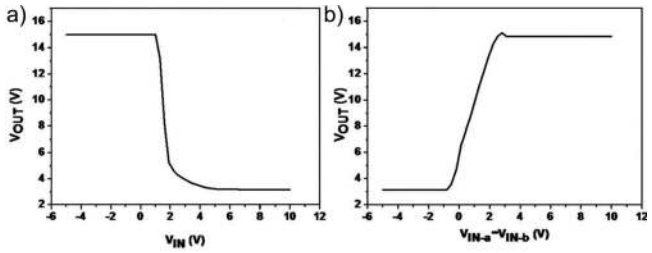

FIG. 53. Input-output characteristics of flexible complementary SnO_x/IGZO analog circuits: (a) common-source and (b) differential amplifier. Reproduced with permission from Martins *et al.*, Adv. Funct. Mater. **23**, 2153 (2013). Copyright 2013 John Wiley and Sons.

Based on the previously mentioned 3D vertically integrated SWCNT/IGZO TFT structure shown by Honda *et al.*, common-source amplifiers with a gain $G > 5$ dB have also been fabricated.[343]

3. Mechanical properties

In addition to the electrical DC and AC characterization, also bendability influences the device performance. Several groups[103,172,177,330,343,344] have characterized hybrid complementary NOT gates under tensile bending, down to radii of 2.6 mm ($\epsilon = 1.25\%$),[343] showing only minor variations. Oh *et al.* reported mechanical bending tests of pentacene/ZnO NOT gates at bending radii of 56 mm with high gains of 100 V/V.[330] The hybrid pentacene/IGZO complementary NOT gate demonstrated by Kim *et al.* yields a maximum gain of 60 V/V at a bending radius of 6 mm.[172] Furthermore, hybrid SWCNT/IGZO complementary NOT gates have proven to be functional, with a maximum gain of 87 V/V even when bent to a tensile radius of 10 mm ($\epsilon = 0.29\%$), as shown in Fig. 51.[103] Additionally, Honda *et al.* proved also the functionality of both the planar and the 3D vertically integrated SWCNT/IGZO NOT gates down to tensile bending radii of 2.6 mm, with a maximum gain of 50 V/V and a low voltage operation.[343,344] Finally, Li *et al.* successfully characterized ZnO/SnO_x CMOS inverters under tensile and compressive strains.[177] In particular, a small gain reduction has been observed under tensile strain, while the influence of compressive strain has been demonstrated to be negligible.[177]

V. METAL OXIDE SEMICONDUCTOR-BASED SYSTEMS

The improvements recently achieved in the electrical (DC and AC) and mechanical performance of flexible metal oxide semiconductor TFTs, combined with special features like transparency, stretchability, conformability, dissolubility, and mechanical activity, envision a wide range of possible applications that go beyond optical displays. Even if the research in this area has only shown significant advances in the last years, already quite a few systems have been developed and brought at least to a prototype stage. This section exemplary lists the progresses achieved in the field of flexible metal oxide semiconductor-based electronics, covering systems for optical displays, sensorics, power transmission, as well as data storage and transmission.

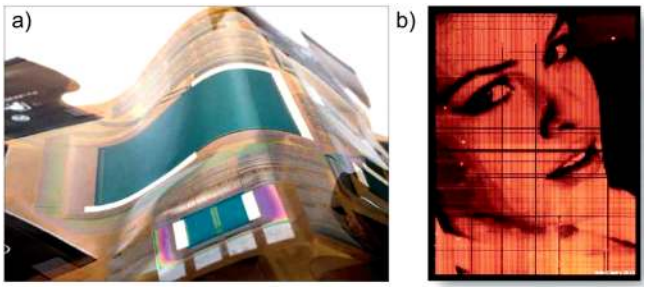

FIG. 54. Flexible active matrix organic light emitting diode (AMOLED) display with self-aligned IGZO TFT backplane: (a) photograph of entire system on PI and (b) quarter-quarter-video-graphics-array (QQVGA) AMOLED display with image applied. Reproduced with permission from Nag *et al.*, J. Soc. Inf. Disp. **22**, 509 (2014). Copyright 2014 John Wiley and Sons.

A. Optical display systems

Optical displays are still the main driving application for metal oxide semiconductor TFTs. Recently, many prototypes of flexible optical displays, especially AMOLED, based on metal oxide semiconductor TFT-based backplanes have been published. The majority of the reported display systems employ vacuum-processed IGZO TFTs[39,40,127,158,175,176,203,310,316,346–352] on PEN,[40,127,158,310,348–352] PI,[316,346–348] or PEEK foils.[203,348] Besides IGZO, also other multicomponent vacuum-processed metal oxide semiconductors like ITZO have been utilized to realize flexible displays.[127] Among the various demonstrated systems, in 2013 Chida *et al.* reported a mechanically flexible 3.4-in. top-emitting AMOLED display yielding 326 pixels per inch (ppi) resolution and consuming 570 mW power.[39] Additionally, the display by Chida *et al.* is operational after 1000 bending cycles at 5 mm bending radius. One year later, Genoe *et al.* proposed the use of a digital pulse width modulation (PWM) to drive a flexible top-emitting AMOLED display (0.54-in., 320 ppi).[310] The PWM concept presented by Genoe *et al.* allows reducing the DC power consumption down to 102.4 mW.[310] Recently, Motomura, Nakajima, and Takei proposed the use of air-reactive electrode-free inverted OLEDs (iOLEDs) in flexible IGZO TFT-driven AMOLEDs (8-in., 100 ppi) to suppress typical undesired effects like dark spot growth and achieve longer lifetimes.[127] Although the iOLED characteristics are inferior to those of conventional OLEDs, the flexible display by Motomura, Nakajima, and Takei yields stable and clear moving images even while bent.[127] Recently, Nag *et al.* successfully demonstrated the integration of a flexible quarter-quarter-video-graphics-array (QQVGA) AMOLED display (85 ppi) driven by self-aligned TG IGZO TFTs.[316] The resulting flexible display requires only five lithographic mask steps and results in a total thickness of $\approx 150\,\mu$m.[316] Fig. 54(a) displays a photograph of the entire system on PI, whereas Fig. 54(b) shows the display with an image applied.[316] Komatsu *et al.* demonstrated a flexible AMOLED displays (3.4-in., 249 ppi) with a CAAC IGZO TFT backplane. The flexible display by Komatsu *et al.* is functional after $\leq$70.000 folding cycles at 1 mm radii.[176] Employing this structure, Komatsu *et al.* fabricated a 5.9-in. foldable book-type AMOLED display, as well as a 5.9-in.

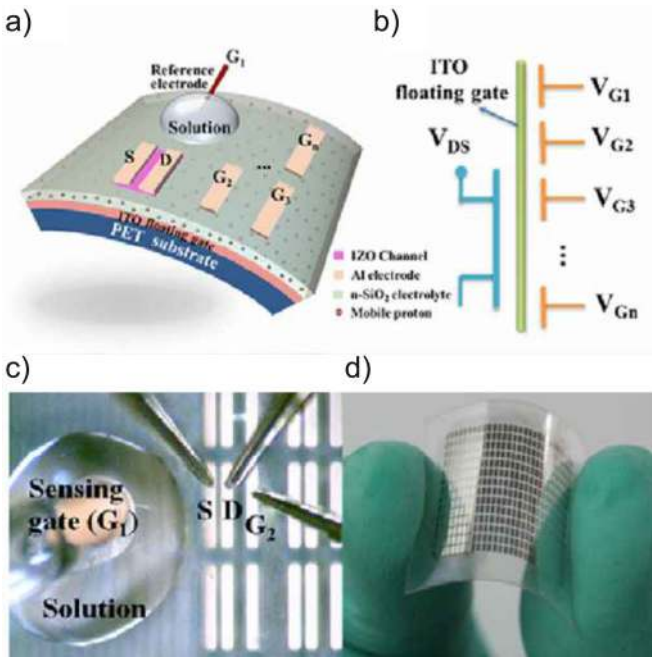

FIG. 55. Flexible pH sensor based on IZO neuron TFT on polyethylene terephthalate (PET) substrate: (a) device cross-section, (b) schematic, as well as (c) micrograph and (d) macrograph of the system. Reproduced with permission from Liu *et al.*, Sci. Rep. **5**, 1 (2015). Copyright 2015 Nature Publishing Group.

tri-foldable AMOLED display for smartphone applications.[176] Beyond AMOLED displays, also a (smaller) woven textile display employing LEDs (3 × 3-matrix) actuated by flexible IGZO TFTs has been realized, showing the feasibility of this technology also for smart textile applications.[214]

B. Sensoric systems

Several sensoric systems, based on metal oxide semiconductor TFTs, have been demonstrated, e.g., for biochemical, temperature, and image sensing applications.

1. Biochemical sensors

Flexible and stretchable metal oxide semiconductor devices are attracting an increasing interest especially in the field of epidermal electronics,[13,15] smart implants,[353] artificial electronic skins for robots,[19] as well as food safety and water monitoring.[166] In order to enable these applications, biochemical sensors are necessary. Recently, Liu *et al.* reported a metal oxide semiconductor TFT-based pH sensor on PET (Fig. 55).[185] The pH sensor is based on an electrolyte gated IZO neuron device, i.e., a TFT with multiple input gates that are capacitively coupled to a floating gate, as proposed by Shibata and Ohmi.[354] In the work by Liu *et al.*, the V_{TH} shift of the flexible IZO neuron TFT is employed to detect pH changes with a sensitivity of around 105 mV/pH.[185] Fig. 55 shows the sensor structure, together with a micrograph and a photograph of the bent device. Also, Shah *et al.* presented a low-cost flexible pH sensoric system (sensitivity: 50 mV/pH) based on an ITO sensing layer fully integrated on top of a flexible IGZO TFT.[166]

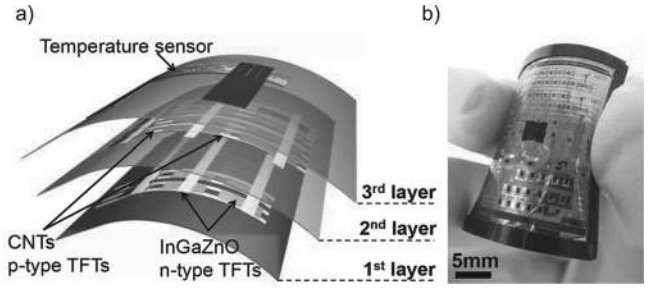

FIG. 56. Flexible three-dimensional vertically integrated temperature sensor and complementary SWCNT/IGZO NOT gate on PI substrate: (a) device cross-section and (b) photograph of the entire system. Reproduced with permission from Honda *et al.*, Adv. Mater. **27**, 4674 (2015). Copyright 2015 John Wiley and Sons.

2. Temperature sensors

To continuously monitor the temperature of temperature-sensitive AMOLEDs or AMFPDs (Active-Matrix Flatpanel Displays), flexible metal oxide semiconductor TFT-based temperature sensors are required. To this regard, an interesting approach has been proposed by Honda *et al.*, who vertically integrated a printed temperature sensor constituted by a SWCNT and poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) conductive sensor ink on top of a SWCNT/IGZO CMOS NOT gate, as shown in Fig. 56.[343] The flexible temperature sensing system yields a sensitivity of 0.68% $°C^{-1}$ and a resolution of $\leq$0.3 °C and is functional while bent to 2.6 mm tensile radius.[343] The high density integration (only 4 μm passivation layer) paves the way to highly integrated and high-performance flexible devices, e.g., for wearable health monitoring.

3. X-ray detectors

Another interesting and novel field of application for metal oxide semiconductor TFTs is represented by flexible x-ray detectors.[355] In 2012, Lujan and Street reported a flexible flat panel (FP) x-ray detector array based on flexible IGZO TFTs on PET.[355] The device operates in indirect detection mode and is based on the integration of a phosphor layer, an a-Si continuous photodiode, and an IGZO TFT backplane. In the device, the x-rays incident on the phosphor layer excited fluorescence, which is subsequently detected and imaged by the a-Si photodiode and TFT backplane. In this way, images with a resolution of 160 × 180 pixel and pixel size of 200 μm can be recorded. Fig. 57 shows an image recorded with the flexible FP x-ray detector array. Few years later, also Smith *et al.* reported large-area flexible x-ray detectors based on a-Si continuous photodiodes and IGZO TFT backplanes on 125 μm PEN foils. In this work, Smith *et al.* proposed a novel assembly technique that allows connecting single flexible x-ray detectors to create a larger composite x-ray detector (Fig. 58).[322] As visible from Fig. 58, 9 x-ray detectors (each with 16 × 16 pixel resolution) are overlapped to create a larger detector array. The assembly technique can be scaled up to even larger x-ray imaging arrays enabling applications in the medical imaging, e.g., single-exposure and low-dose digital radiography. In 2015, Gelinck *et al.* presented a flexible x-ray detector based

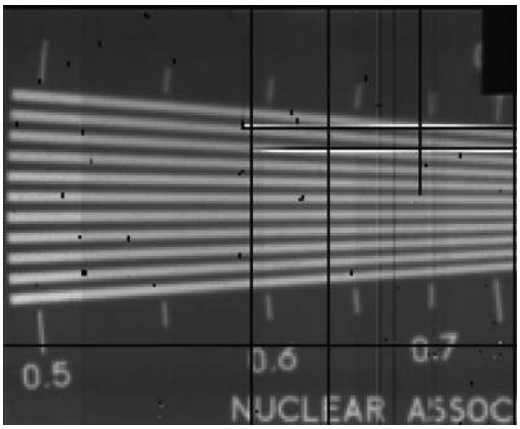

FIG. 57. X-ray image obtained from an 80 kV exposure with a flexible flat panel x-ray detector array fabricated with an IGZO TFT backplane on PET. The black dots and lines are defects. Reproduced with permission from R. A. Lujan and R. A. Street, IEEE Electron Device Lett. **33**, 688 (2012). Copyright 2012 Institute of Electrical and Electronic Engineers.

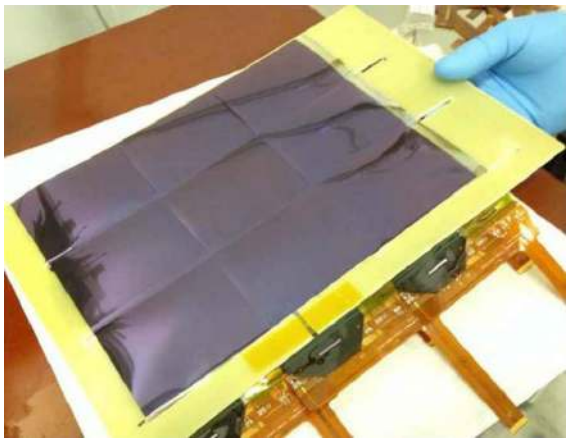

FIG. 58. Large-area flexible composite x-ray detector constituted by a 3 × 3 active matrix array of 9 individual flexible x-ray detectors based on a continuous photodiodes and IGZO TFT backplanes. Reproduced with permission from Smith *et al*., IEEE Trans. Compon., Packag., Manuf. Technol. **4**, 1109 (2014). Copyright 2014 Institute of Electrical and Electronic Engineers.

on an organic photodetector (OPD) layer and an IGZO TFT backplane all integrated on a 25 μm PEN foil.[356] The use of a solution-processed OPD instead of an a-Si photodiode allows reducing the number of photolithographic steps, opening the way to lower production costs. Using this flexible OPD/IGZO TFT x-ray detector, images with a resolution of 120 × 160 pixel and pixel size of 126 μm can be recorded at a high-resolution (10 frames/s).[356] The flexibility of all these x-ray imaging systems allows realizing curved detectors for applications such as computed tomography, where a round detector is more beneficial.

C. Power transmission systems

Flexible wireless power transmission systems can be realized by utilizing two coils (source and receiver) and a rectifier circuit, which can be either implemented with p-n diodes[81] or with TFTs in diode load configuration (i.e., shorted gate-drain nodes).[315] In the following, we introduce the basic structure and operating principle of p-n diodes, followed by an overview of the state-of-the-art flexible p-n diodes based on metal oxide semiconductors. Finally, we introduce two wireless power transmission systems developed, based on elastic NiO/IGZO diodes[81] and flexible diode load IGZO TFTs.[315]

1. Diodes

Diodes are electronic components with two terminals that conduct primarily in one direction. A p-n diode is realized by a p- and an n-type semiconductor brought in contact with each other to form a p-n junction.[97] The p-n junction facilitates the current conduction exclusively in one direction and suppresses the current flow in the other direction, acting thus as a rectifying element.[97] Instead of a semiconductor-semiconductor junction, a Schottky diode possesses a metal-semiconductor junction. Here, a Schottky barrier is formed, allowing the device to have a very high switching speed and a low forward voltage drop.[97] At the same time, also a diode-connected TFT with shorted drain and gate electrodes acts as a diode.[357]

2. Metal oxide semiconductor diodes

Flexible metal oxide semiconductor-based p-n diodes have been realized by employing n-type IGZO and either Cu_2O or NiO p-type semiconductors.[81,358,359] In particular, Chen *et al*. reported a mechanically flexible Cu_2O/IGZO p-n diode on PEN.[358] The authors demonstrated also the rectification characteristics of the Cu_2O/IGZO diode by converting an AC voltage of 4 V into a DC voltage of around 2.5 V.[358] The −3 dB frequency of around 27 MHz (even while bent to 20 mm radii) allows employing the rectifier even for HF applications.[358] Utilizing IGZO and NiO semiconductors, Münzenrieder *et al*. presented a mechanically bendable p-n diode fabricated at room temperature on PI.[359] The rectification properties of the NiO/IGZO diode have been shown even down to a radius of 10 mm. The 4.7% increased rectified voltage for the bent NiO/IGZO rectifier is attributed to the enhanced conductivity of the bent diode compared with the flat one.[359] Flexible Schottky diodes based on metal oxide semiconductors have been demonstrated with both ZnO and IGZO.[360–363] Specifically, Zhang *et al*. presented an Ag/ZnO Schottky diode fabricated on ITO-coated PET substrates bendable down to a radius of 30 mm.[360] Notably, in a follow-up work, Zhang *et al*. further successfully increased the cutoff frequency to 6.3 GHz, which is well beyond the critical speed of 2.45 GHz needed for principal frequency bands for smartphones.[362] Another work by Chasin *et al*. showed IGZO-based Schottky diodes converting 3 V AC voltage into a 1.7 V DC voltage at a cutoff frequency of 1.1 GHz.[361] Only recently, Semple *et al*. showed solution-processed Schottky diodes based on ZnO, which have a cutoff frequency well beyond 20 MHz.[363]

3. Diode-based power transmission systems

Utilizing a rectifier circuit constituted by 4 NiO/IGZO p-n diodes in a bridge configuration, Münzenrieder *et al*. realized an elastic and conformable wireless power transmission system (Figs. 59(a) and 59(b)). In the system by

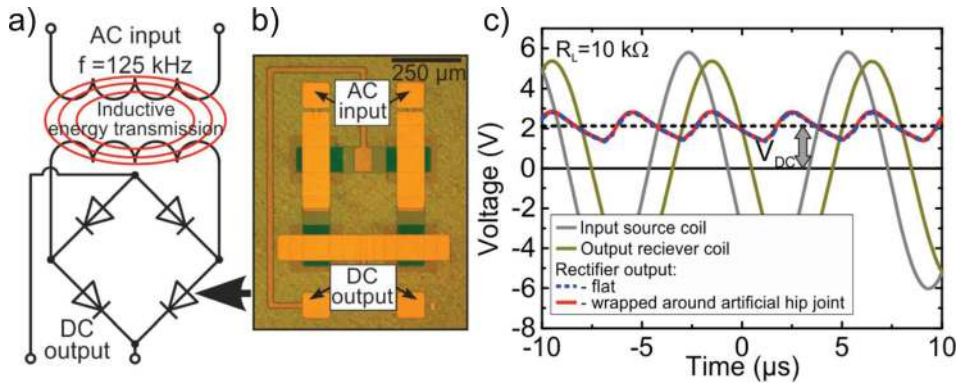

FIG. 59. Elastic wireless power transmission system: (a) circuit schematic, (b) optical micrograph, and (c) time evolution of the input and output signals. The system is capable of transmitting a DC voltage of around 2.1 V (the transmitted power is of 450 μW), even when conformed around an artificial hip joint with a radius of 14 mm. Reproduced with permission from Münzenrieder *et al*., Adv. Electron. Mater. **1**, 1400038 (2015). Copyright 2015 John Wiley and Sons.

Münzenrieder *et al*., an AC voltage is first transferred wirelessly via inductive coupling of two coils (source and receiver) and subsequently rectified by the diode bridge (Fig. 59).[81] The transmitted DC power of 450 μW is sufficient to supply standard metal oxide semiconductor-based circuits. Furthermore, the wireless power transmission system is functional while conformably wrapped around an artificial hip joint (at a radius of 14 mm), as shown in Fig. 59(c).

4. TFT-based power transmission systems

It is also possible to rectify a wireless transmitted AC voltage utilizing flexible IGZO TFTs in diode load configuration, as demonstrated by Myny *et al*.[315] In this particular example, Myny *et al*. employed the rectified voltage to power an NFC tag on PET (typical transmitted power of $\approx$10 μW).

D. Data transmission systems

Aside optical displays, one of the main application areas of flexible metal oxide semiconductor TFT is that of large-scale, cheap, and disposable data transmission systems, such as RFID/NFC tags and smart labels.[87] In this field, special features like transparency would even enable new application frontiers, such as flexible and transparent RFID/NFC tags seamlessly embedded in food and water packages, mirrors, windows, or even books.

1. NFC tags

Myny *et al*. demonstrated a flexible NFC tag based on at least 218 IGZO TFTs on PET.[315] Details of the circuit block diagram can be found in Sec. IV B. The flexible NFC tag is powered by inductively coupling it to a commercial USB-connected NFC reader (operating at 13.56 MHz and at a maximum distance of 5.2 cm).[315] As a main result, Myny *et al*. demonstrated that the flexible IGZO-based NFC tag can meet the key requirements for RFID/NFC applications (e.g., power consumption, data rates, and signal encoding).[315]

E. Data storage systems

Storing data is also essential for flexible electronic systems. As already seen in Sections II and III, ferroelectric P(VDF-TrFE)[132,136,146,149,167,273] or chicken albumen[204] gate dielectrics allow realizing non-volatile 1-bit memory elements. To this regard, Van Breemen *et al*. demonstrated a non-volatile memory array [16 × 16 IGZO TFTs with P(VDF-TrFE) gate dielectrics on PEN] with retention times of up to 12 days.[167] The same group reported also the integration of a similar flexible non-volatile memory array (4 × 4) with a TFT addressing circuit (based on standard BG IGZO devices) that can read and write each single memory element of the array.[136] It was shown that the IGZO TFT-based addressing circuit is able to successfully program/erase the non-volatile memory array using 10 ms per memory element. Furthermore, a suitable margin of 4 V between the "0" and "1" states allows a fast and reliable read-out of the stored data.

VI. CONCLUSIONS

Flexible metal oxide semiconductor-based TFTs have not only made their entry in the market of optical displays[30] but also shown to be suitable for other novel electronic systems, e.g., for sensorics, power supplies, as well as data storage and transmission. This wide range of applicability of flexible metal oxide semiconductor technology is owed to its excellent electrical and mechanical properties, combined with unique features like transparency, light-weight, 3D conformability, stretchability, and/or solution-processability. In this paper, we have reviewed the state-of-the-art of flexible TFTs, circuits, and systems based on metal oxide semiconductors. Significant attention has been devoted to aspects especially important for flexible devices: from the materials (i.e., substrates that are flexible, temperature- and chemical-resistant, etc.), the fabrication techniques (i.e., substrate preparation, low temperature deposition methods, layer structuring on dimensionally unstable substrate, etc.), the electrical performance, the mechanical properties (i.e., bendability and improvement of bendability) to special features (i.e., transparency, stretchability, dissolubility, etc.). The main part of the review has described the currently available approaches to realize flexible TFTs based on vacuum-deposited n-type metal oxide semiconductors. However, also novel topics like solution-processing and hole conduction in flexible metal oxide semiconductor TFTs have been

thorougly reported. Given the recent progresses achieved in the large-area integration of flexible devices, a relevant part of the review has focused on circuits, as well as on systems based on metal oxide semiconductor TFTs. Examples of novel large-area flexible electronic systems include flexible, textile-integrated, rollable and/or foldable optical displays,[39,40,127,158,175,176,203,214,310,316,346–352] flexible and/or stretchable systems for temperature,[343] pH,[166,185] and x-ray sensing,[322,355,356] wireless power transmission,[81,315] as well as non-volatile storage and NFC transmission of data.[136,167,204,315] Despite the advances that flexible metal oxide semiconductor TFTs have witnessed in the last decade, there are still some bottlenecks that prevent the commercialization of this technology in new areas of application beyond optical displays. To broaden the field of application of flexible metal oxide semiconductor TFTs, future work should focus first of all on the optimization and establishment of the developed technology. In particular, specifically complete TFT models simulating both electrical and mechanical TFT properties are necessary to predict the performance under every circumstance, e.g., substrate fabrication, peeling and/or transferring, as well as bending and/or stretching. In addition to the development of suitable models, further advances in the material technology are also necessary. This means combining advanced flexible substrates (i.e., ultra-thin, lightweight, transparent, conformable, stretchable, biocompatible, biodegradable, and/or cheap) with suitable device layers (i.e., thin, ductile, transparent, biocompatible, and/or biodegradable) to realize a broad range of flexible devices: from TFTs, circuits, sensors, display elements, actuators to power supplies. Furthermore, with the help of suitable models, many efforts need to be devoted also in the heterogeneous integration of all these devices over large-area flexible substrates in order to achieve electrically and mechanically robust and reliable systems. Finally, future commercialization of flexible metal oxide semiconductor electronics calls for a reduction of the manufacturing cost. To this regard, scalable and high-throughput solution-processing fabrication techniques on large-area flexible substrates need to be optimized and established, aiming especially at fully printed or roll-to-roll manufacturing processes.[87,119] Once these issues will be solved, flexible metal oxide semiconductor-based devices promise to be integrated into everyday objects, such as disposable and inexpensive consumer products like smart labels for food, water, and plant monitoring,[1,80,166] autonomous textile-integrated systems for healthcare, sport, and automotive,[5,6] conformable and stretchable devices for robotic artificial skins,[19] as well as imperceptible and implantable prostheses or diagnostic tools.[13,15,353] Even if at present there is still work to be done, the speed of development that this field has undergone in the last years lets us foresee that flexible metal oxide semiconductor-based technology will play a key role in tomorrow's electronic scenario.

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