Metastability of CMOS Latch/Flip-Flop

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Abstract

This paper presents several design issues of CMOS latch/flip-flops for meta-stable hardness in terms of optimal device size, aspect ratio, and configurations by using the AC small signal analysis in the frequency domain rather than the time domain. This new design approach is verified experimentally. The power supply disturbance and temperature variation effects on the metastability are measured and the measurement data confirm that a reduced power supply voltage and a higher temperature cause a lower meta-stable resolving capability.

Introduction

Arbiters and synchronizer are essential parts of VLSI circuits such as microprocessors and memories. However, these circuits can cause system failures and malfunctions in digital systems due to metastability. These failures come from the delay of logic decision time due to the meta-stable state which lasts between the stable logic states (0 or 1) for an unlimited time. To date, analysis has mainly focused on the understanding of this phenomena and its measurement. Considering that the process sequence and device parameters cannot be chosen purely for the hardness against metastability. the best way for the circuit designer to attack this problem is to choose the optimal device size, aspect ratio and circuit configuration as long as these changes do not affect the original purpose and overall performance of the latches and flip-flops. Simulations and ensuing analyses such as finding out the resolving time have been mostly in the time domain. In this paper, the AC frequency domain analysis is used for the simulations, and it is verified that this approach is viable by comparing with the results previously investigated analytically and by time domain simulation. Moreover, this new approach suggests the optimal aspect ratio of feedback transmission gate of the CMOS D-latch, D flip-flop with preset and clear, and RS flip-flop. These are verified experimentally by the late transition detection method. Using the same method, the power supply disturbance and chip temperature effects on the meta-stability are measured as well.

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Simulation

As published in many reports, flip-flops or latches used in arbiters or synchronizers have a positive feedback loop which consists of back to back inverters. When a flip-flop hangs in the meta-stable state, then it can be viewed as the differential amplifier biased with operating voltage, V_m, where the input and output of an inverter are the same, which is exactly the meta-stable state. After a few iterations, V_m is obtained in SPICE. As can be seen in the DC transfer curve of the CMOS inverter, the PMOS and NMOS transistors are both in the saturation region, therefore this inverter has a high AC gain. By SPICE simulations, the AC gain of the output node with respect to the input node of the back to back inverters with V_m the operating voltage is looked at in frequency domain to find the gain-bandwidth product. All simulation results which will be presented later are obtained basically by the same simulation approach.

Design of CMOS D-latch

The failure rate of the latch/flip-flop is exponentially proportional with the resolving time, τ, which is the measure of how quickly latch/flip-flop comes out of the meta-stable state and settles to a stable state. This resolving time is inversely proportional to the gain-bandwidth of the positive feedback system. Therefore, maximizing the gain-bandwidth is the target task for designing the meta-stable hardened latch/flip-flop. The device parameters used in SPICE simulations are listed in Table 1.

Ratio of inverters

The schematic diagram of a commonly used CMOS D-latch is shown in Fig. 1. When the set-up time is violated, a runt signal latches in node A, which is meta-stable condition. At the next clock phase $\bar{\phi}$, Q and $\bar{Q}$, the output voltages at node B and C, are equal to V_m. This is the initialization phase of meta-stable operation. The back to back inverter can be viewed as a differential amplifier with V_m an operating voltage. AC small signal analysis is used to find out the gain-bandwidth product for different inverter ratios k ($=W_p/W_n$) while having minimum channel length 4 μm. As shown in Fig. 2, the maximum gain-bandwidth product is achieved when k=1, which agrees with the previous analytical results

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[ref.2,3,4]. Therefore, this AC small signal approach with SPICE simulations is viable in finding the maximum gain-bandwidth.

Aspect ratio of feedback transmission gate

In normal design, the size of the feedback transmission gate is not critical since it only provides a path from output to input. However in the case of the meta-stable hardened design, the feedback gate can contribute to maximizing the gain-bandwidth product of the closed feedback loop system. Again, using SPICE, the gain-bandwidth product is obtained assuming that this system is a linear differential amplifier with DC operating voltage set at V_m. As shown in Fig. 3, the gain-bandwidth product is maximum when W/L of the NMOS transistor is 0.375 - 0.75 (W/L of PMOS is 0.75 - 1.5). The DC gains are the same, regardless of size for the feedback transmission gate. The bandwidth increases with 1/W owing to the reduction of source/drain junction capacitance. But due to channel resistance, it decreases If W is too small. All simulations are made by changing only device widths with fixed channel length. Considering the narrow channel effect, 0.75(1.5) is the optimal W/L of NMOS(PMOS) transistors for the feedback transmission gate.

Design of CMOS RS flip-flop

The same criterion of maximizing the gain-bandwidth product of a flip-flop for the hardness against meta-stable operation is applied to a CMOS RS flip-flop design. In Fig. 4, two commonly used configurations for a two input NAND gate RS flip-flop are shown. From a functional viewpoint, the two configurations are equivalent. However once the flip-flop reaches the meta-stable state, the resolving times can be different. In Fig. 5, the equivalent circuit configurations of these flip-flops when they are in the meta-stable state are shown. DC operating voltages are set at V_m with both reset/set high (this is a condition for triggering into the meta-stable state), and both circuits can be seen as differential amplifiers consisting of two inverters connected back to back. Configuration A turns out to be a "cascode" amplifier which reduces the miller effect, and accordingly gives a higher gain-bandwidth product. DC gains and bandwidths for configuration A and B are listed in Table 2. As expected, configuration A has a higher gain-bandwidth product than B. Therefore configuration A is more desirable than B in terms of the hardness against the meta-stable operation. The same analysis can be applied equally to two input NOR RS flip-flops as well.

Design of CMOS D flip-flop with preset and clear

In Fig. 6, two different configurations of the NMOS section of the first stage of a 3 input NAND gate CMOS D flip-flop with preset and clear are shown. The same analysis which was used in the RS flip-flop design can be applied, and configuration A is better than B in terms of having the higher gain-bandwidth, with accordingly shorter resolving time of meta-stable operation since it reduces the miller effect more effectively. Compared with the simple D-latch, either configuration is better than the D-latch in terms of the gain-bandwidth product because it has a cascode configuration with data and clock high, while the D-latch has just a configuration of simple inverters. This will be discussed further in the next section.

Measurement and Results

In the case of chips where all output signals are amplified at output buffers, the late transition detection method [ref.1] can be used to measure the metastability. The schematic of the measurement set-up is shown in Fig. 7. A CMOS D-latch with the configuration of Fig.1 and a CMOS D flip-flop with preset and clear are compared in terms of the failure rates due to metastability, and their results are shown in Fig 8. These two are fabricated by the same technology and on the same wafer. The slopes inversely represent the resolving capability. By using the least square error method, it turns out that the flip-flop with preset and clear has a higher slope (shorter resolving time) than the D latch as shown in Table 3. This verifies that the cascode configuration of D flip-flop resulting from either configuration of Fig. 6 gives a higher gain-bandwidth product (shorter resolving time) than a simple D-latch. In addition, the power supply (DC) voltages were reduced and by the same detection method, its effects on the MTBF were measured as shown in Fig. 9. The slopes (resolving capability) were obtained by the least square error method and listed in Table 4. It is observed that the power supply disturbance not only causes a shorter MTBF, but also a longer resolving time. In Fig. 10 and Table. 5, the chip temperature effects on the metastability are also shown. It is again observed that a latch/flip-flop has a worse meta-stable resolving capability under higher chip temperature.

Conclusion

The design of a meta-stable hardened CMOS latch/flip-flop is discussed using the criterion that the higher gain-bandwidth product of the closed feedback loop system gives the shorter resolving time for the meta-stable state. AC small signal analysis using SPICE predicts an optimum inverter ratio of 1, which agrees with previous results. Using this approach, the optimal aspect ratio of feedback transmission gate of a CMOS D-latch is obtained. For the CMOS RS flip-flop and CMOS D-latch with preset and clear, an improved configuration is found by showing that it has a higher gain-bandwidth product. Finally this design approach using AC small signal simulations is confirmed experimentally, and the power supply disturbance and chip temperature effects on the meta-stability are also measured and its results analyzed.

Acknowledgement

The authors wish to thank Signetics for fabricating the test circuits.

References

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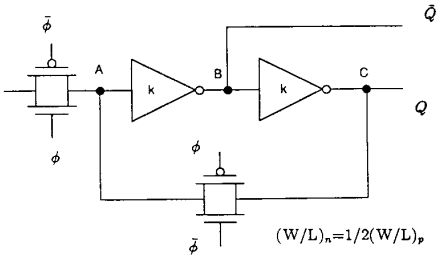

Fig. 1. CMOS D-latch.

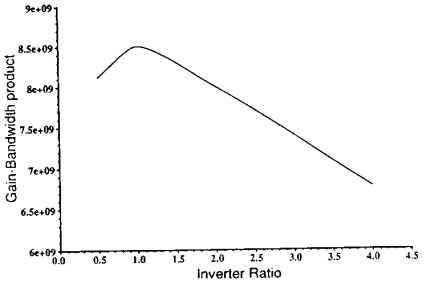

Fig. 2. Gain-Bandwidth product with respect to the ratio of inverters of CMOS D-latch.

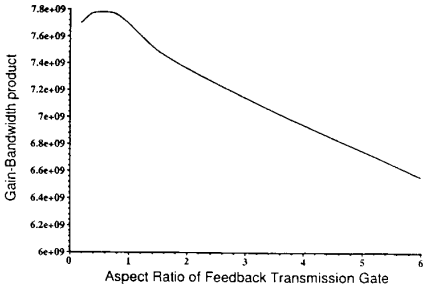

Fig. 3. Gain-Bandwidth product with respect to the aspect ratio of feedback transmission gate of CMOS D-latch.

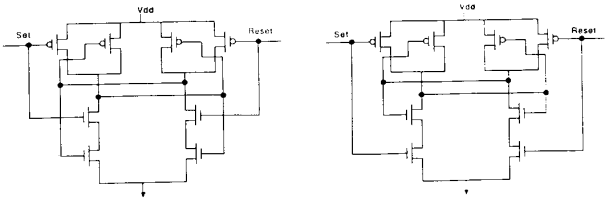

Fig. 4. Configuration A (left) and B (right) of CMOS RS flip-flop.

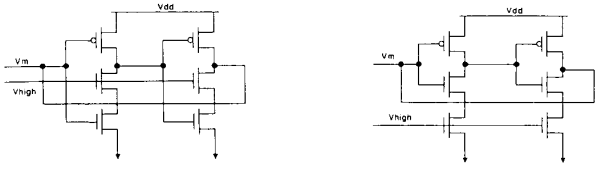

Fig. 5. The config. A (left) and B (right) in the meta stable operation of CMOS RS flip-flop.

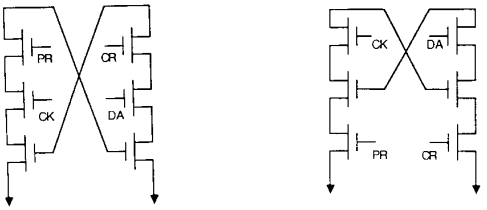

Fig. 6. Configuration A (left) and B (right) of CMOS D flip-flop with preset and clear.

Parameter	NMOS	PMOS	Unit
V_{to}	0.7	-0.7	Volt
K_p	6.04	3.02	10^{-5}
Gamma	0.21	0.667	
CGSO	3.5	3.5	10^{-10}
CGDO	3.5	3.5	10^{-10}
Phi	0.576	0.695	
T_{ox}	4.0	4.0	10^{-8}
N_{sub}	1.0	1.0	10^{15}
L_d	0.3	0.3	10^{-6}
C_j	8.0	2.0	10^{-5}
λ	0.0138	0.0138	

Table 1. SPICE parameters for NMOS and PMOS.

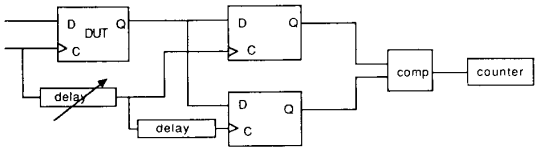

Fig. 7. Late transition detection measurement set-up.

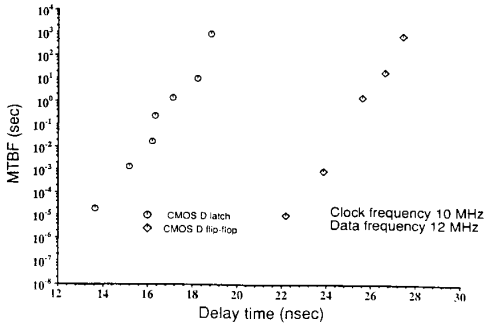

Fig. 8. Measurement data for CMOS D-latch and CMOS D flip-flop with Preset and Clear.

	CMOS D-latch	CMOS D flip-flop with pr/cr
slope	1.44 dec/ns	1.52 dec/ns

Table 3. Slopes of Data in Fig. 8.

	Config. A	Config. B
(1) Gain	1128	8552
(2) Bandwidth	6.50E06	7.20E05
(1)×(2)	7.33E09	6.15E09

Table 2. Gain and Bandwidth of config. A and B of CMOS RS flip-flop.

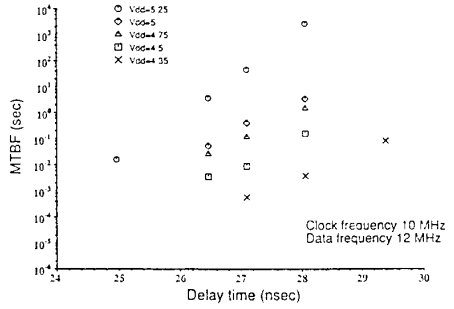

Fig. 9. Measurement data with power supply disturbance.

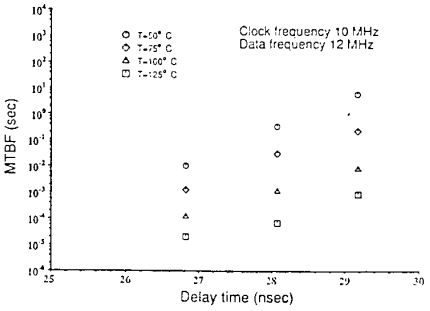

Fig. 10. Measurement data with chip temperature variations.

Vdd	slope
5.25	1.68 dec/ns
5	1.12 dec/ns
4.75	1.10 dec/ns
4.5	1.05 dec/ns
4.35	0.90 dec/ns

Table 4. Slopes of Data in Fig. 9.

Temperature	slope
$50°C$	1.160 dec/ns
$75°C$	0.951 dec/ns
$100°C$	0.773 dec/ns
$125°C$	0.674 dec/ns

Table 5. Slopes of Data in Fig. 10.