Metric-Driven Design Verification

An Engineer's and Executive's Guide to First Pass Success

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Hamilton Carter has been awarded 14 patents in the field of functional verification. The patents address efficient sequencers for verification simulators, MESI cache coherency verification and component-based reusable verification systems. Carter worked on verification of the K5, K6, and K7 processors and their chipsets at AMD. He staffed and managed the first functional verification team at Cirrus Logic and has served as a manager, engineer, or consultant on over 20 commercial chips and EDA projects.

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Shankar Hemmady is a senior manager at Cadence responsible for verification planning, methodology, and management solutions. Mr. Hemmady has verified and tested, or managed the functional closure of over 25 commercial chips over the past 18 years during his tenure in the industry as an engineer, manager, and consultant at 12 companies, including AMD, Cirrus Logic, Fujitsu, Hewlett Packard, Intel, S3, Sun, and Xerox.

Dedications

To my Parents who removed the word "cannot" from my vocabulary!

Hamilton Carter

To Seema, Shona, & Anand who make each and every moment a special one!

Shankar Hemmady

Preface

With the alarming number of first pass silicon functional failures, it has become necessary for all levels of engineering companies to understand the verification process. This book is organized to address all verification stakeholders at all levels of the engineering organization. The book is targeted at three somewhat distinct audiences:

- *Executives*. The people with their jobs on the line for increasing shareholder value.
- *Project, design, and verification managers*. The people responsible for making sure each design goes out on time and perfect!
- *Verification and design engineers*. The innovators responsible for making sure that the project actually succeeds.

The book is divided into three parts corresponding to its three audiences. The level of technical depth increases as the book proceeds.

Part I gives an overview of the functional verification process. It also includes descriptions of the tools that are used in this flow and the people that enable it all. After outlining functional verification, Part I describes how the proper application of metric-driven techniques can enable more productive, more predictable and higher quality verification projects. Part I is targeted at the executive. It is designed to enable executives to ask appropriate educated questions to accurately measure and control the flow of a project.

Part I also holds value for project managers and verification engineers. It provides an overall view of the entire chip design process from a verification perspective. The chapters on a typical verification project and the overview of verification technologies will be of use to entry level verification engineers as well. This part of the book also provides a unique viewpoint on why management is asking for process data and how that data might be used.

Part II describes the various process flows used in verification. It delves into how these flows can be automated, and what metrics can be measured to accurately gauge the progress of each process. Part II is targeted at design and verification project managers. The emphasis is on how to use metrics within the context of standardized processes to react effectively to bumps in the project's execution.

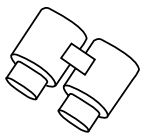
Part III's audience is the design and verification engineering team. It focuses on the actual verification processes to be implemented and executed. This section of the book is divided with respect to the various verification technologies. Each chapter on a given technology is further subdivided into sections on how to plan effectively, and how to track metrics to closure.

Entire books have been written on implementing verification using the technologies discussed in Part III. We will not reiterate what those excellent volumes have already stated, nor do we intend to reinvent the wheel (yet, we are engineers after all). Implementation details will be discussed when they will make the metric-driven techniques discussed more effective.

Part IV contains various case studies and commentaries from experts in the metric-driven verification field.

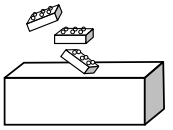
The various parts of the book can also be described as a progression of process abstractions. The layers of abstractions are "Observational Processes," "Container Processes," and "Implementation Processes."

Observational Processes



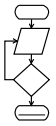
Part I looks at the verification process from an observational point of view. The various aspects of a project that should be observed are described to the reader along with informal suggestions about how to strategically manage a verification project based on these observations.

Container Processes



Part II looks at processes that are necessary regardless of the verification technology you are using; processes such as regression management, revision control, and debug. Part II describes how to implement these processes using metric-driven methodologies. It also also discusses the inter-relations of these processes.

Implementation Processes

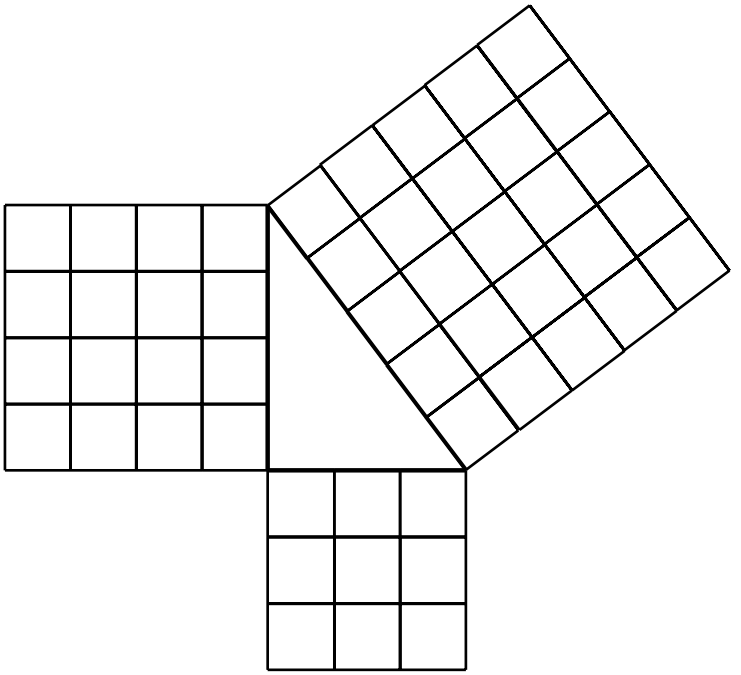


Part III describes each of the verification technologies and explores how a metric-driven methodology can be used to enhance the productivity, predictability, and quality offered by each of these technologies.

Finally, *Part IV* leaves the world of abstraction altogether and presents several concrete case studies that illustrate metric-driven processes in action. In addition to these case studies are several commentaries offered by industry experts in metric-driven methodologies.

Introduction

Legend has it that 2300 years ago, Euclid walked the beaches of Egypt with his students. They were exploring the fundamentals of a new field: geometry. Each day, Euclid would draw a new problem in the sandy shores of the Mediterranean Sea. He'd ask his students to reflect on each problem and discover what they could. One day he sketched a diagram that would come to be known as Euclid's 42nd Problem.



One of his particularly bright students worked on the diagram and came back with a simple formula:

$$a^2 + b^2 = c^2$$

This formula became so famous that it is now known simply by its discoverer's name: the Pythagorean Formula.

Pythagoras thirsted for knowledge and spent most of his life traveling the various countries of the ancient Hellenic world searching for it. In his travels, he encountered many cultures and gleaned valuable knowledge from each of them applying it to the burgeoning new field of geometry.

Today we're witnessing the birth of another new field, Metric-Driven Verification. Like Euclid, we hope to layout templates that not only illustrate the basics of this promising new field, but also inspire the reader to make even greater discoveries. Like Pythagoras, we have traveled the world searching for the best applications of this knowledge.

This book contains more than our basic understanding of the principles of metric-driven verification. The book also contains examples and experiences gleaned from many industry experts in verification and design. All of these are presented in their entirety in Part IV.

The last three chapters of Part III are about emerging technologies in the field of metric-driven verification:

- System verification
- Mixed-signal verification
- Verification of DFT hardware

These chapters use a different format. Each chapter contains a complete case study from one of the industry leaders in each of these three emerging areas.

Contributing Authors in Order of Appearance

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Jason Andrews is a project leader at Cadence Design Systems, where he is responsible for hardware/software coverification and methodology for system-on-chip (SoC) verification. He is the author of the book "Co-Verification of Hardware and Software for ARM SoC Design" and holds a bachelor's degree in electrical engineering from The Citadel (Charleston, SC) and a master's degree in electrical engineering from the University of Minnesota (Minneapolis).

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Ms. Chiavacci cofounded Yogitech in 2000. She is responsible for the mixed signal division. She worked as an analog designer from 1998 to 2000 after receiving her degree cum laude in electronic engineering at the Pisa University. Her work experiences include high-reliability systems in critical environments such as biomedical, space, and high-voltage automotive applications.

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Mr. Zarri is a verification engineer at Yogitech. He is responsible for the development of verification IPs, verification environments for many international customers, and trainings on verification methodologies. His experience includes automotive protocols such as LIN, CAN, and Flexray. He is expert in OCP protocol, a universal complete socket standard for SoC design, and has recently acquired experience in the verification of mixed signal circuits. Gabriele specialized in Microelectronics and Telecommunications with an MS from Nice Sophia-Antipolis University.

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Jean-Paul Lambrechts has over 20 years experience in leading hardware design in the networking and computer areas. His experience covers board-level hardware design, FPGA, and verification. Jean-Paul has now been with Cisco for 9 years where he has been responsible for line cards, packet forwarding engines, and layer 4–7 processor card. Jean-Paul holds a MSEE degree from the Louvain University in Belgium.

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Dr. Andreas Dieckmann

In 1995, after obtaining his MA at the University of Erlangen and his Ph.D. in electronic engineering at Technical University of Munich, Dr. Dieckmann began working at Siemens AG. He was initially responsible for board and fault simulation. From 1997, Dr. Dieckmann gained expertise in system simulation and verification of ASICs. Since 2001, he has been in charge of coordinating and leading several verification projects employing simulation with VHDL and Specman "e," formal property and equivalence checking, emulation, and prototyping.

Susan Peterson

Susan Peterson has been trying to escape from the EDA industry for the past 20 years, where she has spent her time listening to customers and trying to help them to solve their critical problems in various sales and marketing roles. Prior to that, she was a practicing engineer, and earned her MBA from the University of Denver.

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Paul Carzola is a senior consulting engineer for verification at Cadence. He received a Bachelor of Science Degree in computer engineering at Florida Atlantic University in 1995. Since then, Paul has spent the last 10 years in functional verification and the pursuit to finding effective and powerful methods to verification while making it easier and enjoyable to apply. For the past 5 years, he has served in a consulting role in the area of functional verification methodology and has seen first hand the power of a Coverage-Driven approach.

YJ Patil

YJ Patil is a senior verification engineer at Genesis Microchip, where he is responsible for managing the verification of digital television (DTV) controller ASICs. Prior to Genesis, Mr. Patil was a verification engineer at several technology leaders including ATI, Silicon Access Networks, and Philips Semiconductors. He was a board designer at Tektronix. Mr. Patil holds an MS in software systems from BITS Pilani, India and BE in electronics and communication from Gulbarga University, India.

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