Micropower CMOS Temperature Sensor with Digital Output

Anton Bakker and Johan H. Huijsing, *Senior Member, IEEE*

***Abstract*—A CMOS smart temperature sensor with digital output is presented. It consumes only 7 μW. To achieve this extremely low-power consumption, the system is equipped with a facility that switches off the supply power after each sample. The circuit uses substrate bipolars as a temperature sensor. Conversion to the digital domain is done by a sigma-delta converter which makes the circuit highly insensitive to digital interference. The complete system is realized in a standard CMOS process and measures only 1.5 mm^2. In the temperature range from -40 to $+120$°C, the inaccuracy is ± 1°C after calibration at two temperatures. The circuit operates at supply voltages down to 2.2 V.**

I. Introduction

LOW-COST high-performance temperature sensors are increasingly required for the following applications: 1) on VLSI chips to control the dissipation; 2) in microsystems to compensate for temperature cross sensitivity of other sensors; 3) in strongly automated production plants; and 4) in automated consumer products like cars and domestic appliances.

Next to the demands on costs and performance, it is also needed to reduce the power consumption of the temperature system to a minimum. The reasons for this are to be able to use the sensor in battery operated products, to reduce the errors caused by self-heating, and to be able to add the sensor to a VLSI chip without causing a significant increase in power consumption of the complete system.

The micropower CMOS smart temperature sensor described here perfectly fits in this low-cost, high-performance, and low-power market. It has its application in the automotive industry, where it is meant to measure the temperature in car tires. This is first for safety reasons and second to compensate for the temperature sensitivity of a pressure sensor which is also located in the tire.

Krummenacher and Oguey [1] presented a smart CMOS temperature sensor with a power consumption of 120 μW. For our application, however, the power consumption should not exceed 10 μW. This is required to guarantee a lifetime of the battery of at least seven years, which is equal to the maximum lifetime of the tire.

Another important disadvantage of the circuit of Krummenacher and Oguey is that they use a lateral bipolar transistor as a temperature sensor. This device can only be used in special processes.

We decided to use the substrate transistor, which is much more compatible with standard CMOS technology. This implies, however, the design of a complete new circuit topology, including offset-reduction techniques. Without degrading the accuracy too much, we obtained a power consumption of 60 μW at continuous operation. Including a power-down facility, this could be reduced to 7 μW at a nominal sample rate of 2 samples/s.

The complete temperature measurement system consists of a temperature sensor, a bandgap voltage reference, and an analog to digital converter on one single chip. The interface to an external microcontroller is 8 b parallel. The target specifications are shown in Table I.

TABLE I
TARGET SPECIFICATIONS

	Min.	Nom.	Max.	Unit
Supply voltage	2.4	3.0	4.0	V
Average supply current (3V, 2 samples/sec)			3	µA
Range	-40		130	°C
Error			±1	°C
Bandwidth	2			samples/sec

II. Integrated Temperature Sensors

In CMOS technology, there are three possible devices which can be used as a temperature sensor:

1) CMOS transistors operating in weak inversion;
2) lateral bipolar transistors;
3) vertical bipolar transistors.

Vittoz [2] showed that it is possible to make voltage references using CMOS transistors operating in weak inversion. However, for temperature sensing, these devices suffer from limited reproducibility on absolute value and temperature coefficient, which are both depending on the threshold voltage.

A lateral bipolar transistor can be used to make an accurate temperature sensor [1], [3]. The quality of the lateral bipolar transistor depends heavily, however, on the IC process. In many processes, especially when no attention has been paid to optimize this device, the current gain of this transistor is very low (< 5) and the leakage current toward substrate (via

Manuscript received December 4, 1995; revised February 5, 1996. This work was supported by the European Committee (ESPRIT Project 9011, acronym Slopsys).

The authors are with the Delft Institute of Microelectronics and Submicron Technology (DIMES), Delft University of Technology, 2628 CD Delft, The Netherlands.

Publisher Item Identifier S 0018-9200(96)04470-8.

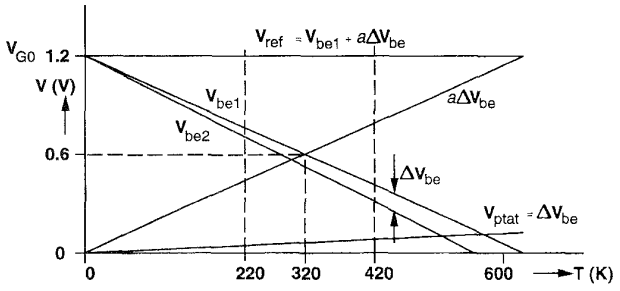


Fig. 1. Derivation of $V_{\rm ptat}$ and $V_{\rm ref}$.

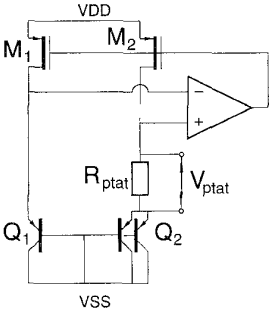


Fig. 2. Basic PTAT circuit.

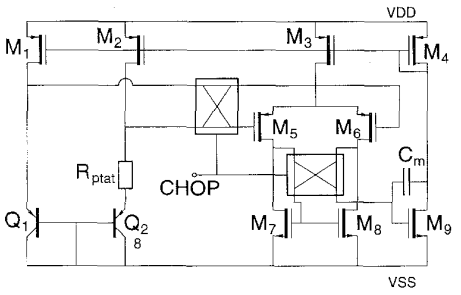


Fig. 3. PTAT circuit with chopper.

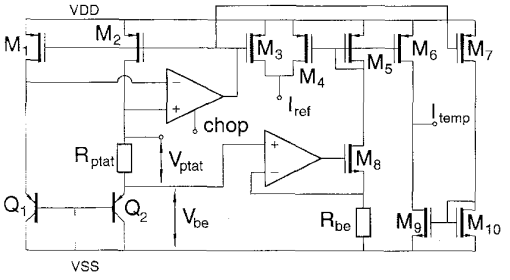


Fig. 4. Simplified schematic of complete analog interface.

the parasitic vertical bipolar) is difficult to control and can be up to 50%. Considering also that data on these parameters is hard to obtain, good circuit design with these devices is hardly feasible.

The vertical bipolar substrate transistor seems to be the best candidate for integrated temperature sensors [4]. The quality of this transistor is comparable to transistors in standard bipolar processes. The characterization of these devices may not be very elaborate in most processes, but is usually sufficient for our purpose. The main problem is the lack of a free collector terminal, which is inherently connected to substrate. This problem can, however, be solved on circuit level.

III. System Design

A. Derivation of Temperature and Reference Signals

The method to derive temperature and reference signals from bipolar transistors has been published extensively [5]–[7]. The design methodology is shown in Fig. 1.

The base-emitter voltage $V_{\rm be}$ of a bipolar transistor decreases almost linearly with temperature. The temperature coefficient is approximately -2 mV/°C. This temperature coefficient is dependent on the emitter current density. The difference between two base-emitter voltages $\Delta V_{\rm be}$ is in a first-order approximation linearly proportional to absolute temperature and can be written as

$$V_{\rm ptat}(T) = \frac{kT}{q}\ln(p) \tag{1}$$

where p is the emitter current density ratio, k is Boltzmann's constant, and q is the electron charge.

At an emitter current density ratio of eight, the temperature coefficient of this PTAT voltage is 0.2 mV/°C. Amplifying this voltage ($a\Delta V_{\rm be}$) and adding it to a base-emitter voltage ($V_{\rm be1}$) results in a so-called bandgap reference voltage independent of temperature ($V_{\rm ref}$).

B. A-D Conversion

$\Sigma\Delta$ converters have proven to be very suitable in low-frequency, high-performance applications. In our case, having a very low-frequency signal (< 2 Hz) and moderate accuracy (8 b) a first-order $\Sigma\Delta$ converter has been chosen because of the lower complexity and die area compared to higher order $\Sigma\Delta$ converters.

C. Calibration

Because a microprocessor is already needed to control the transmitter for the tire control application, it will be cheaper to implement the calibration facility in this microprocessor than to do a laser trimming or digital calibration on the chip. At this moment, a choice still needs to be made whether to implement the calibration figures in EEPROM, PROM, or even in RAM. This is mainly dependent on the quality of EEPROM at high temperatures (130°C) and long lifetime (over seven years).

IV. Circuit Implementation

A. PTAT Circuit

The basic schematic for a CMOS PTAT circuit is shown in Fig. 2. Because the collectors of the substrate bipolars are connected to the substrate, an operational amplifier is required to regulate the emitter currents. The offset drift of this CMOS amplifier is, however, in the order of the

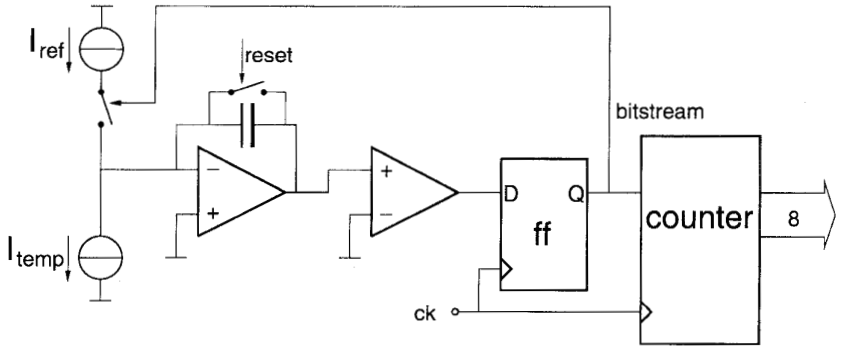


Fig. 5. Schematic of first-order current-mode $\Sigma\Delta$ converter.

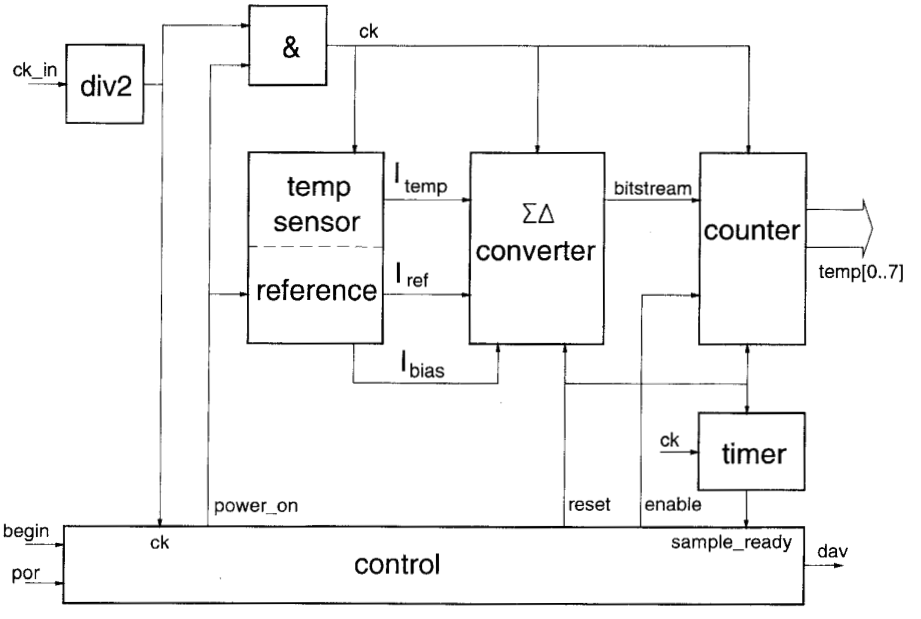


Fig. 6. Block schematic of complete temperature system.

required accuracy (1°C $\approx$ 200 μV) which makes an offset compensation technique necessary.

There are two topologies for offset compensation: Autozeroing and chopping [8]. The autozeroing technique is more complicated to combine with a current-mode $\Sigma\Delta$ converter, because of the not continuously available output signal. A choice has therefore been made to implement the chopping technique.

B. Chopper Circuit

The PTAT circuit with chopper is shown in Fig. 3. The opamp, as schematically shown in Fig. 2, consists of two amplifying stages. The first stage of the opamp is formed by $M_5 \cdots M_8$, while the second one is formed by M_9. The Miller capacitor C_m is needed for stabilization of the circuit.

The chopper circuit is usually placed across the entire opamp. In our case, however, the chopper is placed only across the first stage of the opamp including the mirror. The offset of the mirror is therefore also removed. The advantage of not placing the chopper across the complete opamp is that the second (Miller compensated) stage acts as a low-pass

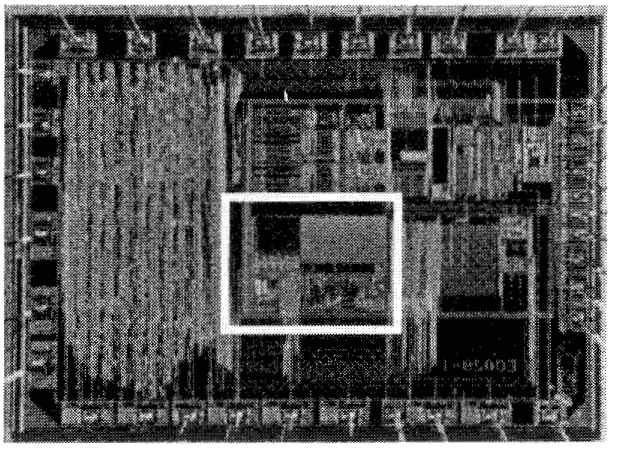


Fig. 7. Micrograph of the realized chip.

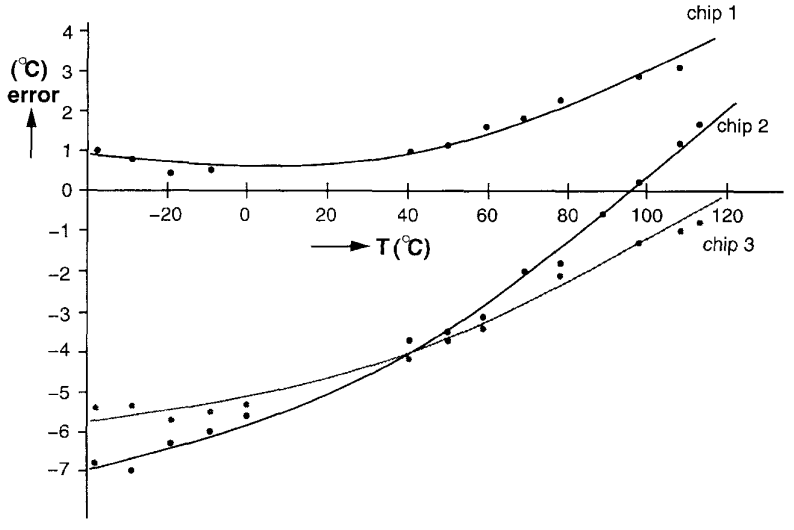


Fig. 8. Error before calibration.

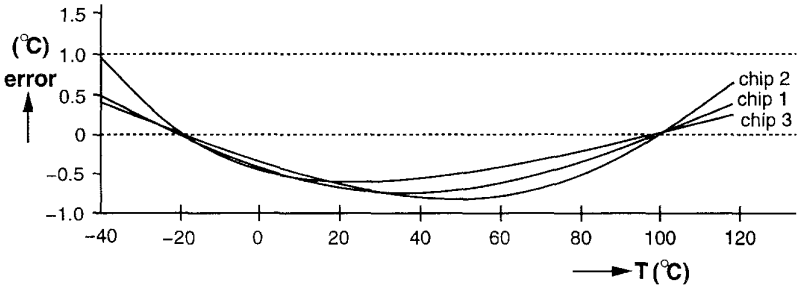


Fig. 9. Error after calibration at $-20°C$ and $100°C$.

filter, which makes an additional low-pass filter unnecessary. Another advantage is that the lack of an additional low-pass filter also increases the bandwidth of the complete system.

This circuit is patent pending [9].

C. Analog Interface Electronics

A simplified schematic of the analog interface is shown in Fig. 4. The left part is the PTAT circuit. The base-emitter voltage of Q_2 is transformed into a current by $R_{\rm be}$. The reference current $I_{\rm ref}$ is the addition of the current through M_3, which is PTAT and the current through M_4, which is proportional to $V_{\rm be}$, thus making a current independent of temperature. The temperature dependent current $I_{\rm temp}$ is formed by the PTAT current through M_9 minus a small current proportional to $V_{\rm be}$ to shift the point at which $I_{\rm temp}$ is zero from $-273°C$ (0 K) to $-61°C$. This is done to enlarge the useful range of the $\Sigma\Delta$ converter. The choice for $-61°C$ as a lowest temperature point is mainly dictated by the need to have a ratio, which makes an accurate scaling of the current mirrors possible. The values of $R_{\rm ptat}$ and $R_{\rm be}$ are 110 kΩ and 560 kΩ, respectively, which are relatively large, but needed to reduce power consumption. The opamp which is used to generate the current proportional to $V_{\rm be}$, does not need to be chopped because the offset drift is fairly small compared to the signal ($1°C \approx 2$ mV).

D. A-D Converter

The principle of the first-order $\Sigma\Delta$ converter is shown in Fig. 5. The bitstream at the output is proportional to $I_{\rm temp}/I_{\rm ref}$. This signal is led to a counter, which acts as a first-order digital decimation filter. The integrator is reset at the start of each sample. The value of the capacitor is 60 pF.

E. Complete Temperature System

A block schematic of the entire temperature system is shown in Fig. 6. The control block is needed to control the power-down mode and the counter. The clock signal has to be divided by two to guarantee a precise 50% duty-cycle, which is needed for the chopper. Both the digital and the analog part can be switched off by the power_on signal.

F. Layout Design and Fabrication

The circuit has been realized in a double-poly 2 μm CMOS process. Special attention has been paid to the matching of transistors and resistors. The complete circuit measures 1.5 mm^2 (excluding bond pads), of which 20% is occupied by poly resistors and 10% by poly-poly capacitors. A micrograph is shown in Fig. 7. This chip, which measures 12 mm^2, also incorporates the pressure sensor interface, which is needed for the tire control application. The analog part of the temperature system is marked by a white rectangle. A second version is

TABLE II
SPECIFICATIONS OF MEASURED TEMPERATURE SYSTEM

	Min.	Nom.	Max.	Unit
Supply voltage	2.2		5.0	V
Supply current Average (3V, 2 samples/sec) During sample		3 25		μA
Clock frequency	25		40	kHz
Range	-40		120	°C
Error			±1	°C
Resolution		8		bits
PSR			0.1	°C/V
Noise		0.1		°C
Bandwidth			50	samples/sec

currently being processed in a state-of-the-art 0.7 μm process, and measures only 0.7 mm^2. This reduction could be reached mainly by resizing the digital part and by replacing the poly resistors of 25 $\Omega/\square$ by high-resistive (undoped) poly of 2 k$\Omega/\square$.

V. MEASUREMENT RESULTS

The chip has been encapsulated in a standard IC package and has been exposed to temperatures in the range from -40 to $+120$°C. The circuit is working at supply voltages varying form 2.2 to 5.0 V. The current consumption is 25 μA at continuous operation (50 samples/s) and 3 μA at a sample rate of 2 samples/s, thus having a nominal power consumption of 3 μA $*$ 2.2 V $=$ 7 μW. Due to the cascoding of all current mirrors and bias circuits, the power supply rejection is limited to 0.1°C/V, which is very good for circuits operating at voltages as low as 2.2 V. The noise is only 0.1°C over the entire temperature range. The specifications of the measured circuit are shown in Table II.

The error over temperature before calibration is shown in Fig. 8. The error is below ±7°C for the entire temperature range for three samples, which is in accordance with the calculated error of ± 8°C. Fig. 9 shows the error after calibration at -20°C and 100°C. This shows that the residual error after calibration is ±1°C.

VI. CONCLUSION

A smart temperature sensor has been presented which offers extremely low power consumption and small chip area. The circuit has been made in standard CMOS technology. Calibration is done in an external microcontroller. The specification of very low power consumption and wide temperature range makes this smart temperature system very suitable to be used as a subsystem in various existing and future electronic systems.

A next generation of this system will use more elaborate offset reduction techniques which will further reduce the errors. The total residual error will then be due to the offset in the base-emitter voltage of the bipolar temperature sensor, which will be ±3°C. The required accuracy of ±1°C can then be met with a single calibration of V_{be} at room temperature.

ACKNOWLEDGMENT

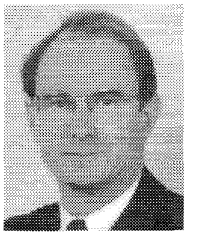
The authors wish to thank F. R. Riedijk for fruitful discussions.

REFERENCES

[1] P. Krummenacher and H. Oguey, "Smart temperature sensor in CMOS technology," *Sensors and Actuators*, vols. A21–A23, pp. 636–638, 1990.
[2] E. A. Vittoz, "A low-voltage CMOS bandgap reference," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 573–577, 1979.
[3] ——, "MOS transistors operated in the lateral bipolar mode and their application in CMOS technology," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 273–279, 1983.
[4] M. Ferro, F. Salerno, and R. Castello, "A floating CMOS bandgap voltage reference for differential applications," *IEEE J. Solid-State Circuits*, vol. 24, pp. 690–697, 1989.
[5] G. C. M. Meijer, "Thermal sensors based on transistors," *Sensors and Actuators*, vol. 10, pp. 103–125, 1986.
[6] G. C. M. Meijer, A. J. M. Boomkamp, and R. J. Duguesnoy, "An accurate biomedical temperature transducer with on-chip microcomputer interfacing," *IEEE J. Solid-State Circuits*, vol. 23, pp. 1405–1410, 1988.
[7] F. R. Riedijk and J. H. Huijsing, "An integrated absolute temperature sensor with sigma-delta A-to-D conversion," *Sensors and Actuators*, vol. A34, pp. 249–256, 1992.
[8] C. C. Enz, E. A. Vittoz, and F. Krummenacher, "A CMOS chopper amplifier," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 335–342, 1987.
[9] A. Bakker and J. H. Huijsing, "Chopper amplifier with internal filter," Dutch patent application no. 10.01231, Sept. 18, 1995.

Anton Bakker was born in Amsterdam, The Netherlands, on July 11, 1968. He received the M.Sc. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1991.

Since then, he has been involved in the development of mixed-mode analog-digital circuits on digital gate-arrays. In 1993, he joined the Electronic Instrumentation Laboratory at the Delft University of Technology where he is now working toward the Ph.D. degree on the subject of CMOS temperature microsystems.



Johan H. Huijsing (SM'81) was born in Bandung, Indonesia, on May 21, 1938. He received the M.Sc. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1969, and the Ph.D. degree from the same university in 1981 for work on operational amplifiers. His thesis was "Integrated Circuits for Accurate Linear Analogue Electric Signal Processing," supervised by Prof. Dr. Ir. J. Davidse.

Since 1969 he has been a member of the Research and Teaching Staff of the Electronic Instrumentation Laboratory, Department of Electrical Engineering, Delft University of Technology, where he is now Professor of Electronic Instrumentation. He teaches courses on electrical measurement techniques, electronic instrumentation, operational amplifiers and analog-to-digital converters. His field of research is analog circuit design (operational amplifiers, analog multipliers, etc.) and integrated smart sensors (signal conditioning on the sensor chip, frequency and digital converters which incorporate sensors, bus interfaces, etc.). He is the author or coauthor of some 110 scientific papers and 15 patents.