Micropower High-Performance SC Building Block for Integrated Low-Level Signal Processing

PETER M. VAN PETEGHEM, MEMBER, IEEE, INGRID VERBAUWHEDE, AND WILLY M. C. SANSEN, MEMBER, IEEE

Abstract—**A switched-capacitor (SC) instrumentation amplifier (IA) is presented, which uses correlated-double sampling (CDS) to reduce the amplifier offset. Additional offset caused by clock-related charge injection is canceled by a symmetrical differential circuit topology, and a three-phase clocking scheme. An experimental low-power test cell has been integrated, showing 100-μV equivalent offset voltage, and input noise equal to 270 μV. For a fixed gain equal to 10- and 8-kHz sampling frequency, the power dissipation is 36 uW (power supply: 5 V), and the circuit only measures 0.2 mm^2.**

NOMENCLATURE

a	Closed-loop gain of the IA.
$A1$	Open-loop gain of differential OTA from main input to output.
$A2$	Gain of the buffers (level shifters) in the CM and offset correction feedback paths (nominally one).
$A3$	Open-loop gain of differential OTA from auxiliary input to output.
CDS	Correlated double sampling.
CMRR	Common-mode rejection ratio.
IA	Instrumentation amplifier.
V_{off1}	Equivalent offset voltage of the OTA main input.
V_{off3}	Equivalent offset voltage of OTA auxiliary input.
$\Delta V1$	Equivalent clock-feedthrough voltage at OTA main input.
$\Delta V3$	Equivalent clock-feedthrough voltage at OTA auxiliary input.
ΔVR	Equivalent differential control voltage at OTA auxiliary input, at the end of the compensation phase.
Fs	Sampling frequency.
OTA	Operational transconductance amplifier.

I. INTRODUCTION

IN THE DESIGN of medical equipment, an evolution is observed towards miniaturization and reduction of power consumption. In this, integration of complex electronic functions on one single chip is becoming a vital point [8].

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The authors are with Katholieke Universiteit Leuven, Department Electrotechnick, B-3030 Heverlee, Belgium.

One of the most critical building blocks is, of course, the instrumentation amplifier (IA): physiological signals usually are very low-level (microvolts), mostly carry information around dc, and exhibit a large and varying common-mode (CM) voltage. Amplifier stages are required at the transducer output, to amplify these signals to a nominal level, adequate for further processing. The offset and integrated noise voltages, which can be attributed to the IA, should be small compared to the input signals; also spurious responses, from common-mode voltages, and disturbances on the supply lines, should be negligible. Gain accuracy, signal bandwidth, and input impedance also are important design specs.

In typical discrete configurations, these requirements are met by using high-quality passive components, by a careful circuit layout, and trimming [20]. In an integrated signal-processing concept, 8 or 10 parallel channels with their own IA are put on the same chip: the design now can only rely on the matching and reliability figures of the MOS technology in which the circuits are implemented, and on the (automatic) compensation and correction schemes, inbedded in the circuitry.

There is a growing consensus to jump over from the established time-continuous approach, to the time-discrete switched-capacitor (SC) approach. This decision is based mostly upon technological design considerations such as sensitivity and matching [12].

Recently, SC techniques have been applied to implement totally integrated IA circuits [2]–[4]. The published building blocks are fully differential stages, which rely on two signal-processing mechanisms:

1) The offset is measured in one clock phase, stored on capacitors, and then subtracted in the subsequent signal amplification clock phase. This technique is known in literature as correlated double sampling (CDS) [9],[10]; CDS not only effectively reduces the offset voltage of the active parts, but also introduces a zero at dc in the transfer functions of the $1/f$-noise and the power-supply noise sources.

2) By the symmetrical differential topology, most spurious signals (like power-supply noise, common-mode signals, and clock feedthrough) appear as common-mode signals, and so are reduced by the CM rejection of the IA.

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Resulting equivalent input offset is ultimately determined by the mismatching in the charge injection of the switches, being a differential-mode signal; reported values [2] are on the order of 1 mV.

In this paper a SC instrumentation amplifier is presented, which uses both CDS and symmetrical differential topology, but which also compensates for charge injection at the most critical nodes [21]. In Section II, the working principles and design equations are clarified. In Section III, measurements are shown, carried out on an experimental test cell, having a fixed gain of 10 (i.e., 20 dB) [1]. As the influence of clock feedthrough (charge injection from the switch transistors) is crucial, Section III is partially devoted to discussion of clock feedthrough and the circuit specs related to it, such as equivalent offset and CM rejection.

II. Design of the SC Instrumentation Amplifier with Offset Cancellation

The SC instrumentation amplifier, presented here, has some correspondence to the circuit of Yen [2],[3]: This means that the input-output switching topology is mainly the same. However, the offset compensation approaches differ widely.

Yen has implemented a two-phase system with two operational amplifiers, and with the coupling capacitors between them serving as offset memorizing devices. One of these amplifiers has a severe upper limit on dc open-loop gain, because in the compensation phase, this amplifier has to amplify its own offset voltage without output saturation. Clock feedthrough is only canceled to the first order by the strictly symmetrical configuration. Equivalent input offset voltages of approximately 1 mV have been reported [2].

The newly invented IA, as shown in Fig. 1, is based on a three-phase clocking scheme. The scheme is completely insensitive to parasitic capacitances. Phase 1 and 2 are the "regular" SC clocks, and due to their switching action, the circuit exhibits a fixed gain. Clock phase 3 does not interfere with the input–output characteristics; its longer duty-cycle (with respect to phase 1) is aimed at the sensing and sampling of amplifier offset and phase 1 clock-feedthrough voltages.

As a compromise between specifications, area and power consumption, an integrated IA can be split into identical sections, with a moderate gain (e.g., 10 or 20). In Fig. 1(a) the total circuit schematic of such an IA is drawn; identical stages can be cascaded to obtain a higher gain. The input capacitors $a \cdot C$ and the feedback capacitors C determine the stage gain a. The capacitors C_H are the offset "hold" capacitances. By the CDS mechanism [9], the output terminals only carry valid signal information, during clock phase 2. Capacitors C_L and the switches $SW12$ and $SW13$ function as a sample/hold stage, and also stabilize the internal amplifier during this clock phase. Buffers $BUF1$ to $BUF4$ are added in order to be able to monitor the measured circuit without altering in a drastic way the

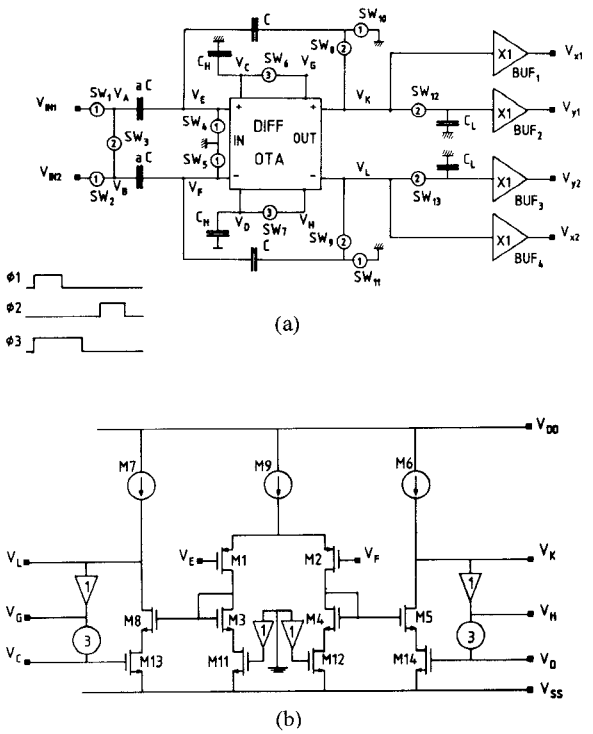


Fig. 1. Circuit schematic of the switched capacitor instrumentation amplifier. (a) Total cell, with inclusion of the unity-gain output buffers (for measurement purposes only). (b) Equivalent circuit schematic of the differential-in, differential-out OTA with common-mode feedback and auxiliary (clocked) input pair for offset and clock-feedthrough reduction. $A1$: gain from (V_E, V_F) to (V_K, V_L). $A3$: gain from (V_C, V_D) to (V_K, V_L).

capacitive and resistive loading of the output (and also accuracy and resolution). Their offset, of course, is not compensated for, but their individual contributions can be measured, as will be commented on further.

Node V_E to V_L refer to the input nodes (V_E, V_F), the output nodes (V_G, V_H, V_L, V_K) and the control input nodes (V_C, V_D) of the amplifier in the IA; the equivalent circuit schematic of it can be found in Fig. 1(b). Globally, it has the topology of a differential-in, differential-out operational transconductance amplifier (OTA) [6] with CM feedback loop [11]. In the presented configuration, transistors $M11$ to $M14$ are biased in the linear region; these voltage dependent resistors act as active-source degeneration of the current mirrors. The CM feedback loop has been opened, and the gate terminals of transistors $M13$ and $M14$ serve as a clocked auxiliary input pair, aimed at the cancellation of amplifier offset. In the following discussion, the OTA gain from the main input (V_E, V_F) is named $A1$, the OTA gain from auxiliary input (V_C, V_D) to output is named $A3$. For buffering and level-shifting purposes source-followers with gain $A2$ (nominally 1) are incorporated.

In clock phase 1, the input signal is sampled on the input capacitors $a \cdot C$, the feedback capacitors C are disconnected from the circuit, and discharged. By switches $SW6$ and $SW7$, the OTA has partial feedback from the output to the auxiliary input. The output voltage (and so also the voltage on the hold capacitors C_H) carries information on the offset voltages, which can be associated with the differ-

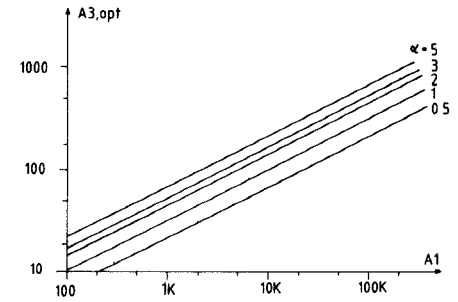


Fig. 2. The optimal gain $A3$ as a function of gain $A1$, for different values of the ratio of equivalent offset at the main input terminal pair, versus the equivalent offset at the auxiliary input terminal pair α.

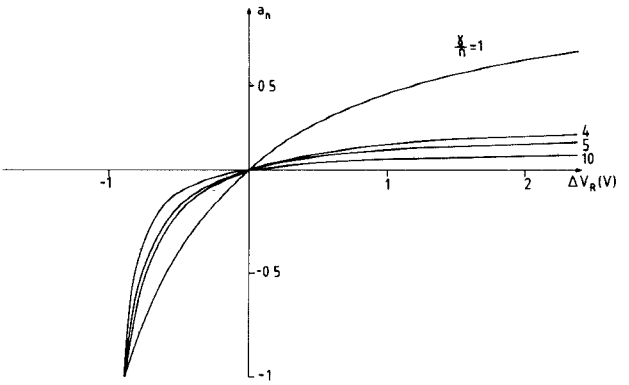


Fig. 3. Input differential-pair current correction factor a_n as a function of the output range, for different values of the design parameter γ/n.

ent gain stages in the OTA (see Nomenclature)

$$V_{\text{out}} = \frac{A1}{1+A2\cdot A3}\cdot V_{\text{off1}} + \frac{A2\cdot A3}{1+A2\cdot A3}\cdot V_{\text{off2}} + \frac{A3}{1+A2\cdot A3}\cdot V_{\text{off3}}. \quad (1)$$

As $A2$ is nominally 1, and $A1$ and $A3$ are both much higher than 1, formula (1) simplifies to

$$V_{\text{out}} = \frac{A1}{A3}\cdot V_{\text{off1}} + V_{\text{off2}} + V_{\text{off3}} \cong \frac{A1}{A3}\cdot V_{\text{off1}} \quad (2)$$

as long as V_{off2} and V_{off3} are on the same order of magnitude as V_{off1}. In the time slot between the falling edges of clocks 1 and 3, this feedback mechanism also stores the additional offset, due to charge injection (clock feedthrough). $\Delta V1$ is the resulting difference signal between terminals V_E and V_F, and can be attributed to mismatches in the circuit. In the same way, at the end of phase 3, the differential charge injection $\Delta V3$ on the hold capacitors C_H must be taken into account. At the beginning of clock phase 2, the charge on capacitors $a\cdot C$ is dumped onto the feedback capacitances. The effective gain of the stage is equal to the capacitance ratio a. The total effective input offset is then

$$V_{os,\text{eq}} = \left[1+\frac{1}{a}\right]\cdot\left[\frac{V_{\text{off1}}+V1}{A3} + \frac{V_{\text{off2}}}{A1} + \frac{V_{\text{off3}}}{A1} + \frac{A3}{A1}\cdot\Delta V3\right]. \quad (3)$$

Equations (2) and (3) dictate that gain $A1$ should be sufficiently high (also for reasons of charge transfer accuracy during phase 2); for every choice of $A1$, there exists an optimal choice of $A3$ which guarantees minimal offset; this choice is a function of the design parameter α (Fig. 2)

$$\alpha = \frac{V_{\text{off1}}+\Delta V1}{\Delta V3} \quad (4)$$

which has to be evaluated based upon previous experience. The values to be applied here should be maximal values, corresponding to the statistical $+3\sigma$ boundaries; under these conditions an upper bound on equivalent input offset can be derived

$$V_{os,\text{eq}} = 2\cdot\sqrt{\frac{(V_{\text{off1}}+\Delta V1)\cdot\Delta V3}{A1}}. \quad (5)$$

If in a particular circuit the offset voltages are smaller than the rated ones, the equivalent offset voltage will also decrease (but only to the square root of the individual offset voltages!). If they are larger, the amplifier ultimately will saturate in phase 1 or 3, and equivalent offset rapidly becomes worse. Any *a priori* estimation of the factor α will thus be a tradeoff between specifications and yield.

As has already been indicated, the gain $A3$ is the result of modulating MOS transistors, biased in the linear region. It is clear that this way of operation is nonlinear, so it is very important to check the large-signal correction ability. For the topology of Fig 1(b), this swing can be characterized by an equivalent current correction factor a_n; a_n is the relative current deviation in the associated current mirror, caused by a deviation of the control terminal ΔV_R from its reference value. The important design parameter is γ/n. γ is the ratio of the transconductances of $M13$ and $M8$, respectively, $M3$ and $M11$, etc. The symbol n stands for slope in weak inversion, and is approximately 1.4; it enters the equations as the input differential pair $M1/M2$ is biased in weak inversion. This option guarantees that for a given gain-bandwidth product (GBW), the power consumption is minimal [14]. It can be seen in Fig. 3 that negative correction factors (i.e., turning $M13$ off) are much easier to achieve than positive correction factors. To get a reasonable correction capability in this circuit configuration (10 percent in both directions), moderate values of γ, leading to reasonable transistor dimensions, are sufficient.

As calculations show, this IA topology has ideally an infinite reduction of CM signals; even the mismatching between switched capacitors, or alternatively, between parasitic capacitances, does not influence the CM gain. Actual CM behavior will be governed by two mechanisms:

a) There will be nonzero CM gain according to the nonzero CM gain of the differential OTA itself; as this last gain is divided by the open-loop gain $A1$, this effect can be neglected.
b) The dynamic redistribution of switch channel charge over source and drain electrodes depends on impedance levels at those electrodes during switching. Therefore mismatches in impedance levels can create a differential signal.

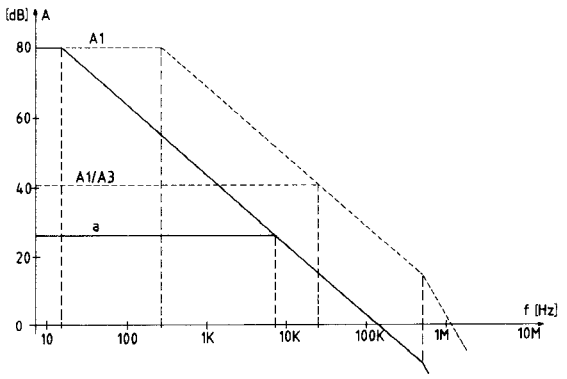


Fig. 4. Bode plot of the gain between differential output, and main input terminal pair, taking into account the two most dominant poles. Solid lines: valid in the amplification phase (phase 2). Dotted lines: valid in the compensation phase (phases 1 and 3).

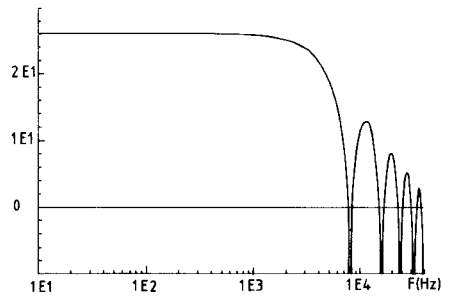


Fig. 5. Calculated transfer function of the SC instrumentation amplifier, for a clock frequency of 8 kHz, and taking into account the $\mathrm{sinc}(x)$ effect.

According to the above discussed circuit principles, some design rules can be given, in order to characterize the total amplifier. Open-loop gains $A1$ and $A3$ are functions of the transconductances g_m and the much less predictable output conductances g_o. As soon as minimal specs are fullfilled with respect to charge transfer inaccuracy, their exact values are not critical. However, their ratio $A1/A3$, which is a very important factor in the offset compensation scheme, can be calculated to depend solely on transconductances

$$\frac{A1}{A3} = \frac{g_{m1}}{n \cdot g_{m13}} \cdot (\gamma + 1). \tag{6}$$

So, current correction capability (a large-signal spec), and minimal achievable offset (a small-signal spec), are interrelated.

Of equally large importance are the dynamical aspects of this circuit. Due to the switched nature, the OTA has in any clock phase a different transfer function, as is graphically shown in Fig. 4; in it the open-loop characteristics referring to gain $A1$, as well as the closed-loop transfer function are shown. As can clearly be seen on this picture, even for relatively low-clock frequencies, very high GBW products have to be achieved, as effective system bandwidth (BW) is the GBW product in that phase, divided by the loop gain in that same phase

$$\mathrm{GBW}_{,\min(ph.1)} = \frac{1+(A1/A3)}{2.\pi} \cdot \frac{1}{T_1} \cdot \ln\left(\frac{1}{\epsilon}\right) \tag{7a}$$

$$\mathrm{GBW}_{,\min(ph.2)} = \frac{1+a}{2 \cdot \pi} \cdot \frac{1}{T_2} \cdot \ln\left(\frac{1}{\epsilon}\right). \tag{7b}$$

In this T_1 (T_2) is the total on-time of clock phase 1 (2), and ϵ is the desired change transfer inaccuracy. As the GBW's in this OTA topology are inversely proportional to the load capacitance

$$\mathrm{GBW} = \frac{g_m}{2 \cdot \pi \cdot C_{\mathrm{load}}} \tag{8}$$

it is clear that for typical parameters ($A1/A3 = 100$, $a = 10$), the load capacitance in phase 1 at the OTA output should be much smaller than in phase 2, to make the amplifier bandwidths equal and minimal, to reduce the aliasing of noise bands into the baseband between dc and the sampling frequency F_s. To decouple the large offset hold capacitor C_H from the output, source followers/buffers were introduced between terminals V_K and V_G, respectively, V_L and V_H (Fig. 1(b)). Two additional source followers were introduced also at the gates of $M11$ and $M12$, where they have no other function than to make the global CM and offset cancellation system insensitive to variations in technological parameters. These source followers add an additional parasitic pole to the loop gain; calculations and simulations show that this amplifier isn't any more stable in unity-gain configuration; however, for the realized loop gains in any clock phase, a sufficiently large phase margin is obtained (larger than 85° typically, according to simulations).

The slew-rate (SR) needed to implement a CDS circuit, is also a very critical design spec, as in each clock phase, the output is reset to the weighted sum of offset voltages (2)

$$\mathrm{SR\,min} = \left[1 - \cos\left(\frac{2 \cdot \pi \cdot f}{F_s}\right)\right] \cdot \frac{V_{\mathrm{ampl}}}{2} \cdot 2 \cdot \pi \cdot (\mathrm{BW}) \tag{9}$$

with

V_{ampl} maximal output signal amplitude,
f signal bandwidth.

As there is a fixed relationship between GBW and SR, if the input transistors work in weak inversion

$$\mathrm{SR} = 4 \cdot \pi \cdot n \cdot k \cdot T \cdot (\mathrm{GBW})/q \tag{10}$$

the signal bandwidth f and the signal amplitude V_{ampl} therefore determine whether the power-efficient [14] weak-inversion operation mode can be used.

An experimental test cell has been integrated, with a gain of 10 (Fig. 5), in a standard 4-μm double-poly CMOS process. The data provided in Tables I and II refer to this design (Fig. 6): this circuit conforms to the topology of Fig. 1(a), including the four-buffer amplifiers (extreme left and right). This microcircuit has a perfect symmetry line around the horizontal axis, except for two noncritical contact holes in the feedback loop (interconnection across that symmetry line). Also, the output buffers are mirrored around that line of symmetry. The gain-determining capacitors $a \cdot C$ and C are composed of unit capacitors; the much less critical capacitors C_L and C_H are contiguous areas. Total chip area is about 2.1 mm^2, while the IA active area (without buffers) only measures about 0.7 mm^2.

TABLE I
GLOBAL DESIGN PARAMETERS OF THE IA AND THE INCORPORATED DIFFERENTIAL OTA

$V_{off1} + \Delta V1$	15	mV
$\Delta V3$	5	mV
α	3	
I.A. gain a	10	
γ	2	
main input gain A1	36000	
aux. input gain A3	330	
ratio A1/A3	110	
Input capacitance a.C	0.40	pF
Feedback capacitance C	4.00	pF
Offset store capacitance C_H	8.30	pF
Total capacitance	25.4	pF
Charge Transf. Inaccuracy ε	0.13	%
O.T.A. unity-gain frequency	420	kHz
O.T.A. phase margin	60	degrees
O.T.A. slew rate	65	mV/usec
Signal bandwidth (-0.2 dB)	650	Hz
Total power consumption	36	uW
Active area	0.7	mm2

TABLE II
DIMENSIONS OF MOS TRANSISTORS, WITH REFERENCE TO FIG. 1(b).

Supply voltage	5	Volt
Reference voltage	2,5	Volt
Clock frequency	8	kHz
Clock rise time	10	nsec
Phase 2 duty cycle	36	%
Output buffers load capacitance	15	pF

III. MEASUREMENTS ON EXPERIMENTAL CIRCUIT

As has been indicated above, the four buffer amplifiers, present in Fig. 1(a), also have been incorporated in the experimental test circuit, in order to be able to monitor voltages without influencing the system behavior (output loading of the IA cell!). However, the specifications of this BUF cell with respect to offset and common-mode rejection ratio (CMRR), are worse than the IA itself (offset standard deviation: 3 mV, CMRR > 75 dB), and are not compensated for. Although, the exact characteristics of any BUF cell can be measured, and so subtracted from the final IA measurements by:

cutting off the biasing current of the OTA, which transforms it in an open circuit, with only pico-Ampere leakage; and closing every switch in the circuit (phases 1, 2, and 3).

This allows the measurement of the transfer characteristics of every BUF cell from analog ground terminal to buffer output terminal, in a nondestructive way. All measurements have been carried out on a set of four samples; relevant specs are averaged over this set.

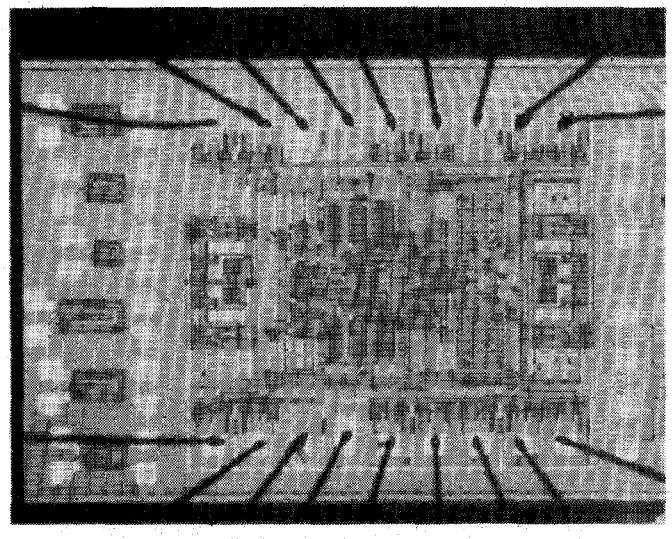
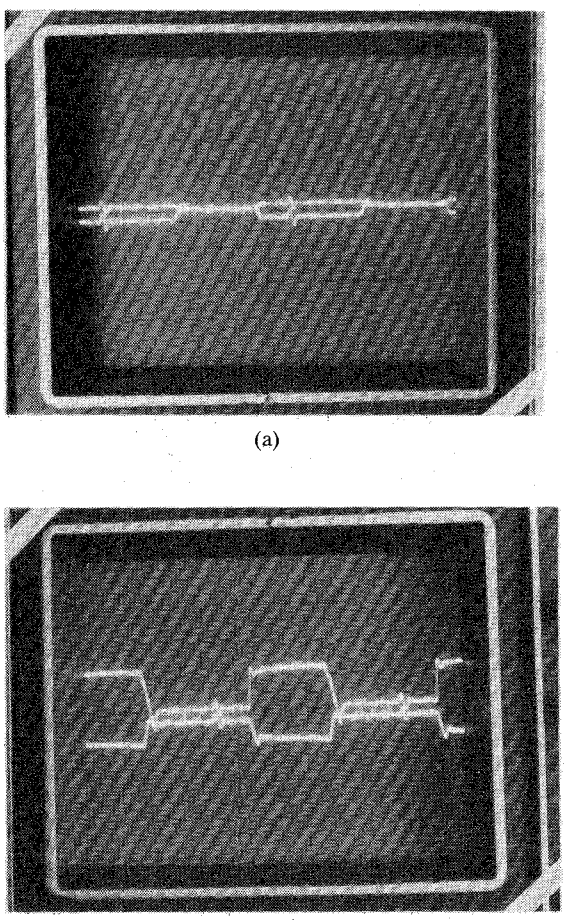


Fig. 6. Microphotography of the integrated instrumentation amplifier, using a standard 4-μm p-well double-poly CMOS process; the circuit has perfect symmetry around the horizontal axis, except for two non-critical contact holes; also the output buffers are mirrored around the same line of symmetry.

In Fig. 7 the differential outputs of the OTA are shown in operation, according to the set of parameters in Table III. In Fig. 7(a) no differential voltage is applied. During the offset compensation phase a differential output voltage is seen, conformal to the amplified sum of offset voltages, as derived in (2). During phase 2, this offset voltage is effectively cancelled. In Fig. 7(b) the same picture is shown for a differential input voltage of 100 mV, causing a differential output voltage 1 V. Differential gain a has been measured and is very close to the *a priori* 20 dB ($\times$10) value (see Table IV), the systematic error of 0.27 dB being due to capacitor mismatch and charge transfer inaccuracy.

The linearity of the IA has been measured by fitting the low-frequency input–output characteristic in the least-mean-squares sense to a linear relationship, and monitoring the residual voltage, which is shown in Fig. 8. Total harmonic distortion is lower than 0.5 percent for the whole range of differential signals: 140-mV_{rms} input level, or 1.4 V_{rms}, 4-V peak–peak output level.

Measurements also have been done with respect to noise. Total integrated input-referred rms noise level is shown in Fig. 9, as a function of clock frequency. At the nominal-



(a) (b)

Fig. 7. Photography of the output voltages, for a typical sample. Output corresponds to the output nodes of the differential OTA in the instrumentation amplifier. (a) Differential input voltage: 0 V. (b) Differential input voltage: 50 mV.

sampling frequency F_s of 8 kHz, noise is approximately 270 μV_{rms}, and increases rapidly when F_s is decreased, as more and more noise bands are aliased. Due to the CDS technique, at F_s equal to 8 kHz this noise mostly originates from white noise sources; when the sampling frequency is reduced, the cancellation of $1/f$-noise gradually deteriorates, leading partially to the observed increase in noise power.

In many applications where IA circuits are applied, there exists a significant mismatch between the resistive impedances of the differential input leads to common. It has been noticed that this influences both unsampled [20], as well as sampled [21] implementations of IA circuits; more precisely, equivalent offset and CMRR specifications have been reported to be degraded. It is therefore very important to investigate how resistive unbalance affects the performance of the here-presented IA.

In our measurement setup, switchable 100-kΩ resistors were introduced between the signal source, and the differential input pair. When the resistors were both switched in the circuit, (or both short-circuited), the rejection of CM signals was very good: more than 100-dB CMRR, see Table IV). However, resistive unbalance significantly decreased this figure; for the extreme case of 100-kΩ unbalance, the CMRR drops to 65 dB at dc, and 60 dB at 50 Hz. As this CMRR decreases is due to clock feedthrough

TABLE III
MEASUREMENT SETUP DATA

TRANSISTOR NUMBER	TYPE	WIDTH (micron)	LENGTH (micron)
M1 M2	P	630	5
M3 M4	N	6	6
M5 M8	N	3 x 6	6
M6 M7	P	3 x 10	6
M9	P	10	6
M11 M12	N	5	30
M13 M14	N	3 x 5	30
Switches	N,P	4	4

TABLE IV
COMPARISON OF DESIGN SPECS AND MEASURED SPECS; THE MEASUREMENTS REFER TO THE CONDITIONS TABULATED IN TABLE III, AND ARE AVERAGED OVER FOUR SAMPLES

	DESIGN SPEC	MEASURED SPEC
Gain	20.00 dB	20.27 dB
		σ = 0.07 dB
Linearity	-	0.5 %
		(at Vin = 140 mV_{RMS})
Offset voltage ($\Delta R = 0$)	< 100 uV	100 uV
		σ = 200 uV
C.M.R.R. ($\Delta R = 0$)	> 120 dB	> 100 dB
(ΔR = 100K)	-	> 65 dB
C.M.R.R. (at 50 Hz) ($\Delta R = 0$)	> 120 dB	> 100 dB
(ΔR = 100K)	-	> 60 dB
Input noise	100 uV_{RMS}	270 UV_{RMS}
PSRR to Vss (at 50 Hz)	-	> 50 dB
PSRR to Vdd (at 50 Hz)	-	> 65 dB

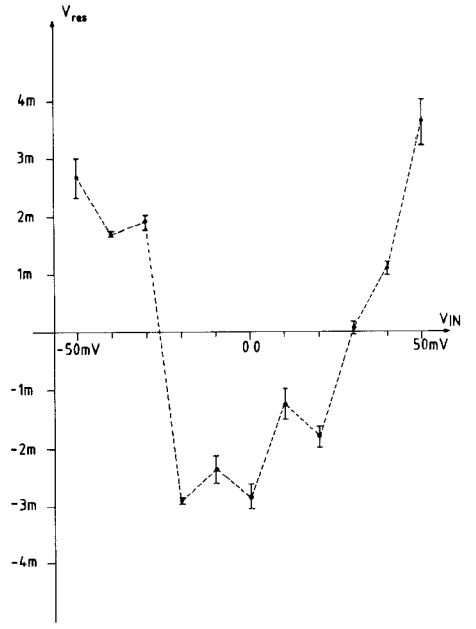


Fig. 8. Nonlinear residual voltage V_{res}, obtained after least-squares fitting of the low-frequency transfer functions, averaged over four typical samples.

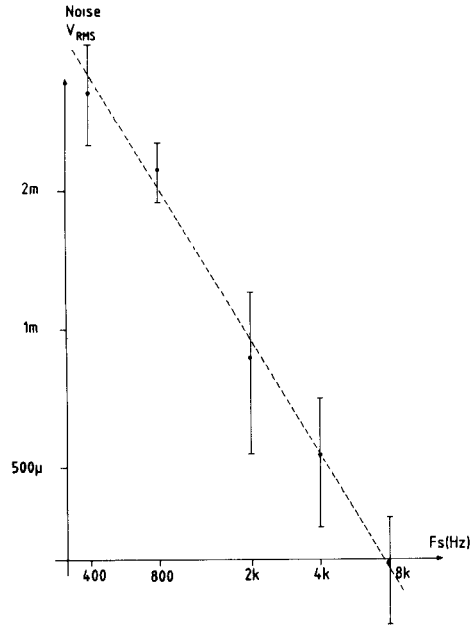


Fig. 9. Equivalent input-referred RMS noise level, as a function of sampling rate F_s; measurement point represent averages over four typical samples.

mechanisms being dependent on impedance levels, design techniques described in [17] are advised.

We also have measured equivalent offset as a function of sampling frequency, showing the effect of charge transfer inaccuracy on the offset compensation process. These measurements are shown in Fig. 10 for two typical samples. When F_s approaches and surpasses the design spec of 8 kHz, the offset voltages rapidly deviate from their initially very promising values, indicating that this actual test circuit has been designed with a relatively small tolerance in the OTA settling time.

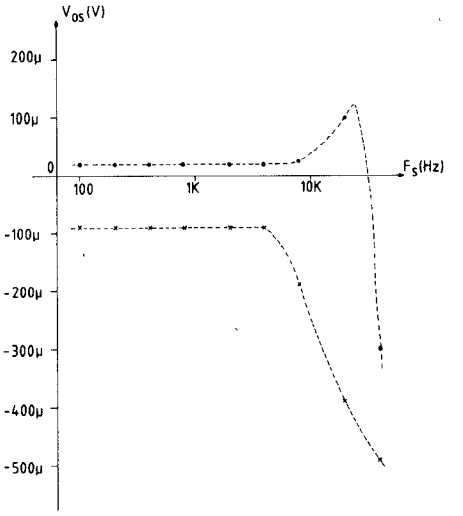


Fig. 10. Equivalent offset voltage as a function of sampling rates F_s, for two typical samples.

IV. Conclusion

An area and power efficient CMOS microcircuit for IA applications has been presented; the design rules are described, and measurements on typical samples are shown. A very low equivalent offset voltage of only 100 μV is realized, on an active area of 0.7 mm^2. It is shown how offset and CMRR are influenced by resistive source unbalance. Noise level is 270 μV_{rms}. A lower noise level would be beneficial in fully exploiting the advantage of the low-dc offset voltage of this IA cell; the 25-pF total capacitance integrated here can be increased within the limits of available chip area and power, to reduce that noise level.

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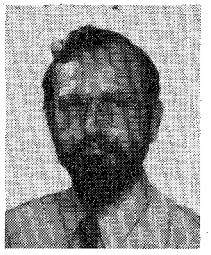
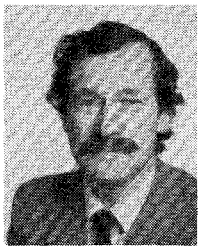


Peter M. Van Peteghem (S'78–M'80) was born in Wilrijk, Belgium, on March 26, 1956. He received the electrical engineering degree from the Katholieke Universiteit Leuven, Heverlee, Belgium, in 1980.

From 1980 to 1982 he was engaged in a project for speech rehabilitation of laryngectomee patients at the University Hospital St. Rafael at Leuven. Since 1982 he has worked as a Research Assistant with the Department of Electrotechnics at the K. U. Leuven, working towards a Ph.D. His research interests are mainly in the design and integration of analog sampled-data circuits, and their incorporation in audio, speech, and biomedical signal-processing systems.

Ingrid Verbauwhede was born in Leuven, Belgium, on October 24, 1961. She received the M.S. degree in electrical engineering from the Katholieke Universiteit Leuven, Heverlee, Belgium, in 1984. Her master's thesis was on the design of a micropower instrumentation amplifier. During the summer of 1983 she worked at the Centre Electronique Horloger (now CSEM), Neuchâtel, Switzerland. In September 1984 she joined the IMEC Laboratory, Heverlee, Belgium, where she is now working towards a Ph.D. on the design of VLSI circuits.



Willy M. C. Sansen (S'66–M'72) was born in Poperinge, Belgium, on May 16, 1943. He received the engineering degree in electronics from the Katholieke Universiteit Leuven, Belgium, in 1967 and the Ph.D. degree in electronics from the University of California, Berkeley, in 1972.

In 1968 he was employed as an Assistant at the Katholieke Universiteit Leuven. In 1971 he was employed as a Teaching Fellow at the University of California. In 1972 he was appointed by the N.F.W.O. (Belgian National Foundation) as a Research Associate, at the Laboratory Elektronika, Systemen, Automatisatie, Technologie, Katholieke Universiteit Leuven, where he is full Professor since 1981. In 1978 he spent the winter quarter as a visiting assistant professor at Stanford University, and in 1981 at the Technical University of Lausanne. His interests are in device modeling, in design of integrated circuits, and in medical electronics.

Dr. Sansen is a member of the Koninklijke Vlaamse Ingenieurs Vereniging (K.V.I.V.), the Audio Engineering Society (A.E.S.), and Sigma Xi. In September 1969 he received a CRB Fellowship from the Belgian American Educational Foundation, in 1970 a G.T.E. Fellowship, and in 1978 a Nato Fellowship.