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Microscopic origin of low frequency noise in MoS_2 field-effect transistors

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We report measurement of low frequency 1/*f* noise in molybdenum di-sulphide (MoS_2) field-effect transistors in multiple device configurations including MoS_2 on silicon dioxide as well as MoS_2-hexagonal boron nitride (hBN) heterostructures. All as-fabricated devices show similar magnitude of noise with number fluctuation as the dominant mechanism at high temperatures and density, although the calculated density of traps is two orders of magnitude higher than that at the SiO_2 interface. Measurements on the heterostructure devices with vacuum annealing and dual gated configuration reveals that along with the channel, metal-MoS_2 contacts also play a significant role in determining noise magnitude in these devices. [http://dx.doi.org/10.1063/1.4895955]

Atomically thin films of MoS_2 have emerged as a promising platform for transparent flexible electronics. In the field-effect geometry, MoS_2 offers several advantages that include large on-off ratio, immunity against short channel effects, and small subthreshold swing.[1,2] These promise MoS_2-based logic devices[3,4] and energy-efficient field-effect transistor,[5–7] although presence of localized band tail due to disorder,[8] and metal-MoS_2 Schottky barriers[1,9] at the contacts were found to severely affect the performance, i.e., mobility of these devices. Low frequency noise, on the other hand, is also considered as one of the basic performance limiting factors in electronic devices, but the effect of the above-mentioned factors on noise is not clearly understood till date. Several groups have recently studied low frequency noise in MoS_2. Sangwan *et al.*[10] showed that noise magnitude increases by two orders of magnitude on exposure to ambient condition, whereas Renteria *et al.*[11] has demonstrated that the noise level considerably increases with prolong exposure to atmospheric condition. Xie *et al.*[12] have performed noise measurement in MoS_2 devices before and after annealing in high vacuum, and showed that noise decreases by a factor of 20 after annealing. These studies mainly focus on the effect of external adsorbates on 1/*f* noise, and a proper understanding of the origin of noise in terms of both internal and external disorder along with contact induced effects is still lacking.

In this letter, we show that along with the channel, contacts also play a crucial role in determining the overall noise magnitude in MoS_2 transistor devices. To show this, we systematically study 1/*f* noise measurement in MoS_2 devices at high vacuum ($\sim 2 \times 10^{-6}$ mbar) where the effect of atmospheric water vapour is minimal. In order to find the effect of lithographic contaminations and residual water vapour, we fabricate MoS_2 devices protected with hexagonal boron nitride. Comparison of 1/*f* noise measurement in protected and unprotected devices before and after annealing indicate that the lithographic polymer, and residual water vapour play a minimal role whereas the transparency of contacts significantly affects the total magnitude of noise in these devices. We also comment on the channel contribution to total noise from our measurement in dual-gated MoS_2 devices.

Bulk MoS_2 crystals were obtained from SPI supplies, and were characterized thoroughly with X-ray photoemission spectroscopy (XPS) and Raman spectroscopy (see Sec. I of the supplementary

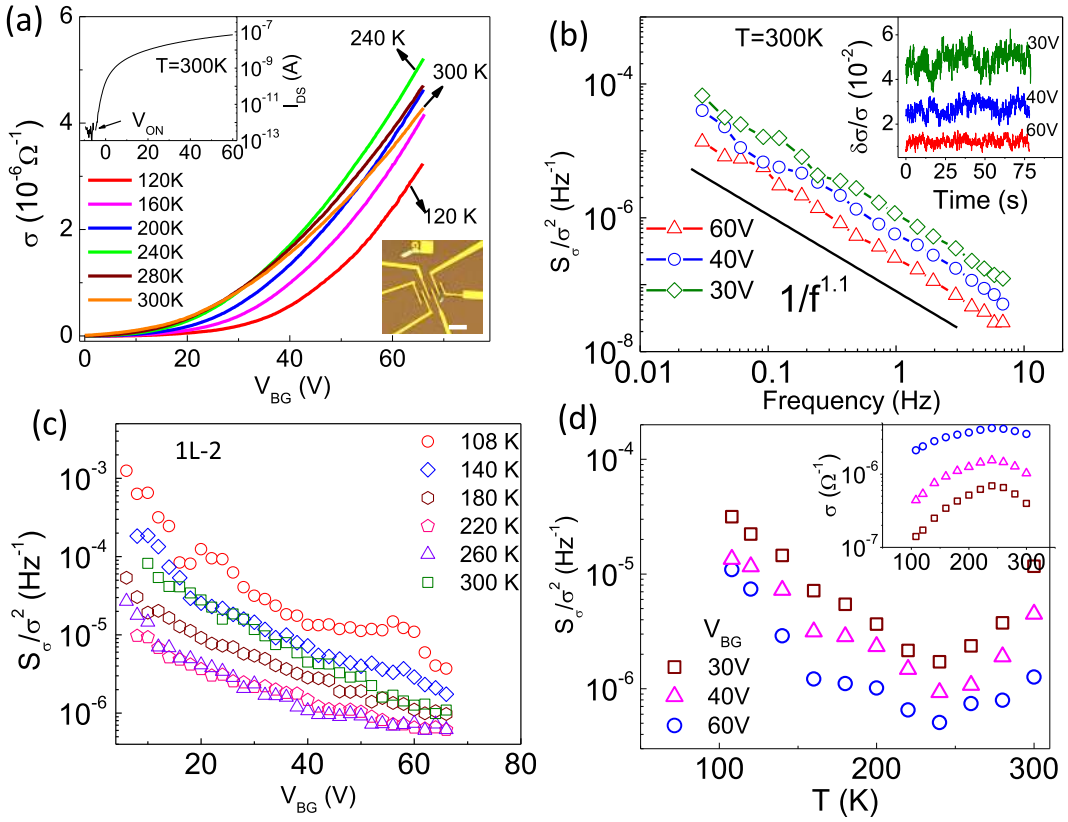

FIG. 1. (a) Conductivity (σ) as a function of backgate voltage (V_{BG}) at different temperature ($V_{DS} = 10$ mV) for a SiO_2-supported single layer device. Inset: Source-drain current (I_{DS}) as a function of V_{BG} at room temperature in log-linear scale (upper left). Optical micrograph of a typical single layer device on Si/SiO_2 substrate. Scale bar 10 μm (lower right). (b) $1/f$ power spectrum of conductivity fluctuations at three different V_{BG}. The inset shows corresponding conductivity fluctuations as a function of time at the same gate voltages. (c) Gate voltage dependence of noise power spectral density S_σ/σ^2 at various T for a typical single layer device. (d) Non-monotonic T dependence of both S_σ/σ^2 at three different V_{BG}. The localized regime was observed below 240 K, and the weak metallic regime for $T > 240$ K. Inset: Non-monotonic T dependence of σ at the same V_{BG}.

material[13]). In this work, we study two different classes of devices: (1) MoS_2 devices on Si/SiO_2 substrate, and (2) MoS_2-hBN heterostructure devices. In case of the former, single and bilayer MoS_2 flakes were exfoliated on 285 nm Si/SiO_2 wafer using the scotch tape technique. Heterostructure devices were fabricated using well known Van der Waals assembly process[14,15] (see Sec. II of the supplementary material[13]). Two different types of heterostructure devices were prepared with MoS_2 being placed either on hBN, or below. We consider the latter as "protected device" since in these devices the channel is never exposed to lithographic polymer residues, and presence of water vapour at the MoS_2-hBN interface is minimal as the transfer process was performed at 120 °C. The degenerately doped Si was used as backgate. Contact pads were designed using standard ebeam lithography, and thermal evaporation of Au (without any adhesive layer, such as Ti or Cr) (see Sec. II of the supplementary material[13]). An optical micrograph of a typical device is shown in bottom-right inset of Fig. 1(a). In all devices (see Table I), the current-voltage ($I_{DS} - V_{DS}$) characteristics were linear at low source-drain bias $V_{DS} \leq 100$ mV, and high back gate voltage (V_{BG}) around room temperature (see Fig. S2 of the supplementary material[13]). We restricted the excitation bias to $V_{DS} \leq$ 100 mV to ensure measurements in linear regime. Both conductivity, and noise measurement were performed in two-probe configuration due to high resistance of the samples using current mode of lock-in amplifier. For noise measurement the sample was biased with an ac voltage ≈10mV (rms) at 777 Hz. The sample current was passed through a low noise preamplifier and measured using lock-in technique.[16] The current fluctuation data were recorded as a function of time as illustrated in the

TABLE I. Details of the devices.

Device	Layer number	Device area (L×W)[a]	Mobility(μ_{FE})[b]
1L-1	1	2 × 2.5	3
1L-2	1	5 × 8	9
1L-3	1	0.8 × 4	3
2L-1	2	2.8 × 2.5	22
2L-2	2	3 × 4.9	11
2L-3	2	1.9 × 2.2	10
2L-BN	2	0.8 × 1.8	3
4L-BN	4	1.7 × 2.7	20
1L-P	1	3 × 4	4

[a]Both dimensions in μm.
[b]In cm^2/V s near room temperature and $\Delta V_{BG} \sim 60V$.

inset of Fig. 1(b), and was Fourier transformed to obtain current noise power spectral density S_I/I^2 as a function of frequency f. For all devices I^2 dependence was checked at every temperature before measurement to avoid any heating induced effect (see Fig. S3 of the supplementary material[13]). Due to linearity, the current power spectral density could be converted to conductivity fluctuation power spectral density S_σ/σ^2 using the relation $S_\sigma/\sigma^2 = S_I/I^2$.

The backgate transfer characteristics of a typical single layer device at various temperatures are shown in Fig. 1(a). We find that from 120 K to 240 K conductivity (σ) increases with increasing temperature indicating a localized transport in this regime.[8] Above 240 K, temperature dependence of conductivity reverses which indicates localized to weak metallic transition (see inset Fig. 1(d)).[9,17] Low frequency noise in our devices showed 1/*f*-type power spectrum (Fig. 1(b)) in the entire gate voltage range down to 80 K. The gate voltage dependence of S_σ/σ^2 is shown in Fig. 1(c). We observed that S_σ/σ^2 decreases monotonically with increasing gate voltage at a fixed temperature. Temperature dependence of S_σ/σ^2 at three different V_{BG} is shown in Fig. 1(d). We observed that noise, like conductivity, is also non-monotonic in temperature. It increases sharply with decreasing temperature below 240 K which can be attributed to the localized state transport, where an exponential increase in noise is predicted due to the broad distribution of the waiting time of the carriers between successive hops.[18] On the other hand, for $T > 240$ K, where σ displays a metal-like transport,[9,17] the noise magnitude slowly increases with increasing temperature similar to diffusive quasi-metallic systems.[19]

In the subsequent sections, we will only discuss the noise behaviour in the diffusive, i.e., high density and temperature regime which is of technological relevance. We first discuss the carrier density dependence of noise in MoS_2 devices on SiO_2 substrate. To obtain carrier density (n), we define V_{ON} (top-left inset of Fig. 1(a)) as the backgate voltage at which the current through the device became measurable (≈1 pA) at $T = 300$ K. The parameter $\Delta V_{BG} = V_{BG} - V_{ON}$ is then approximately proportional to carrier density (n) particularly at high ΔV_{BG}. In Fig. 2(a), we plot ΔV_{BG} dependence of noise for 1L-2 device at various temperature. We find that the dependence slowly becomes $1/(\Delta V_{BG})^2$ as temperature approaches to room temperature. In Fig. 2(b), we plot carrier density dependence of room temperature noise for three different devices on Si/SiO_2 substrate. We observe that at low ΔV_{BG}, the variation differs from one sample to another and may be connected to the details of electron localization. However, at large ΔV_{BG}, *all* devices show $S_\sigma/\sigma^2 \propto 1/\Delta V_{BG}^2$, which is a characteristic feature of *number fluctuation* in semiconductor channels.[20] The interfacial trap states in the SiO_2 substrate close to channel has been quantitatively shown to cause similar scenario in graphene-on-SiO_2[21,22] and Si-MOSFETs.[23] In order to check whether the oxide traps can account for the observed noise, we calculate interfacial trap density D_{it} from observed noise magnitude using[24]

$$S_I = \frac{g_m^2 q^2 k_B T D_{it}}{W L C_{ox}^2 f}, \tag{1}$$

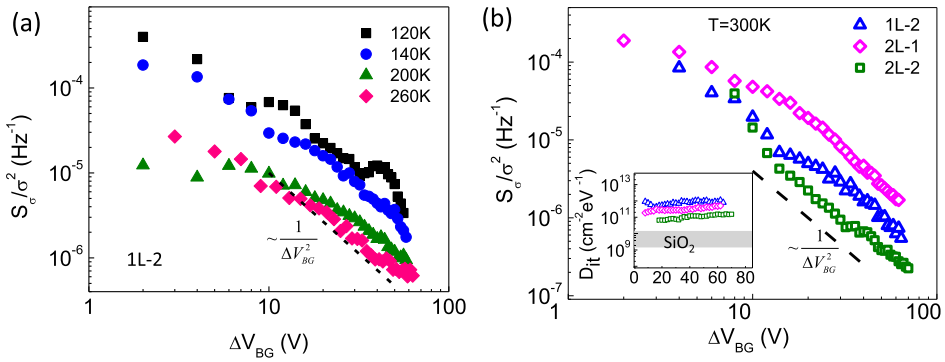

FIG. 2. (a) Carrier density dependence of S_σ/σ^2 for a single layer device at different temperature. The dependence evolves to $1/\Delta V_{BG}^2$ as T approaches room temperature. (b) $1/\Delta V_{BG}^2$ dependence of S_σ/σ^2 at high V_{BG} and near room temperature for three different MoS_2 devices on SiO_2 substrate. Inset: Calculated trap density D_{it} as a function of V_{BG} for 1L-2, 2L-1, and 2L-2 devices on SiO_2 substrate. The SiO_2 interface trap density is indicated by the gray band.

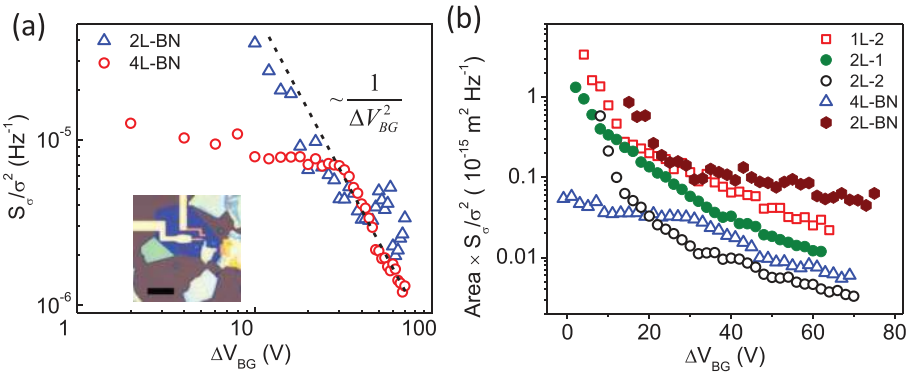

FIG. 3. (a) $1/\Delta V_{BG}^2$ dependence of S_σ/σ^2 at high V_{BG} in MoS_2 on hBN substrate. The inset shows the optical micrograph of an MoS_2 on hBN device. Scale bar 8 μm. (b) Comparison of area-normalized noise magnitude in MoS_2 devices on SiO_2 and hBN substrate at 300 K.

where g_m, L, and W are device transconductance, length, and width, respectively, q is electronic charge, C_{ox} is gate oxide capacitance per unit area. The application of the number fluctuation model here is justified by the observation of nearly constant S_I/g_m^2 in our devices,[25] which also suggests that at high ΔV_{BG} resistance at the MoS_2-Au interface could be mainly due to randomly distributed defects states, rather than a conventional Schottky barriers at the metal-semiconductor interface. Similar conclusion was reached in tunneling spectroscopic study as well.[26] The calculated D_{it} which ranges between 6×10^{10} and 1×10^{12} cm^{-2} eV^{-1} has been plotted in the inset of Fig. 2(b) for three different devices on SiO_2 substrate. We observe that D_{it} is approximately one to two orders of magnitude higher than SiO_2 trap density[24] (see Sec. VI of the supplementary material for details[13]). Recent studies of noise,[11] as well as space charge limited conductivity,[27] yield very similar magnitude of trap density in MoS_2 thin film transistors.

For further understanding on the defects states, we fabricated MoS_2 transistor on crystalline hexagonal boron nitride (hBN) substrate known to be free from surface trap states and dangling bonds.[28] This device architecture eliminates the SiO_2 trap states as a mean to exchange carriers with the channel. Noise measurements on two "MoS_2 on hBN" devices are shown in Fig. 3(a) which also follow $1/\Delta V_{BG}^2$ dependence at high ΔV_{BG}. The area normalized noise magnitude for these two devices are compared with SiO_2-supported devices as a function of carrier density in Fig. 3(b). We find that the noise level in both kinds of devices is similar which indicates that only the interfacial trap charges cannot account for the observed noise magnitude.

The high noise level in as-fabricated devices, as discussed above, can be attributed to several factors. Lithographic polymer residues can act as additional trapping-detrapping source. Localized

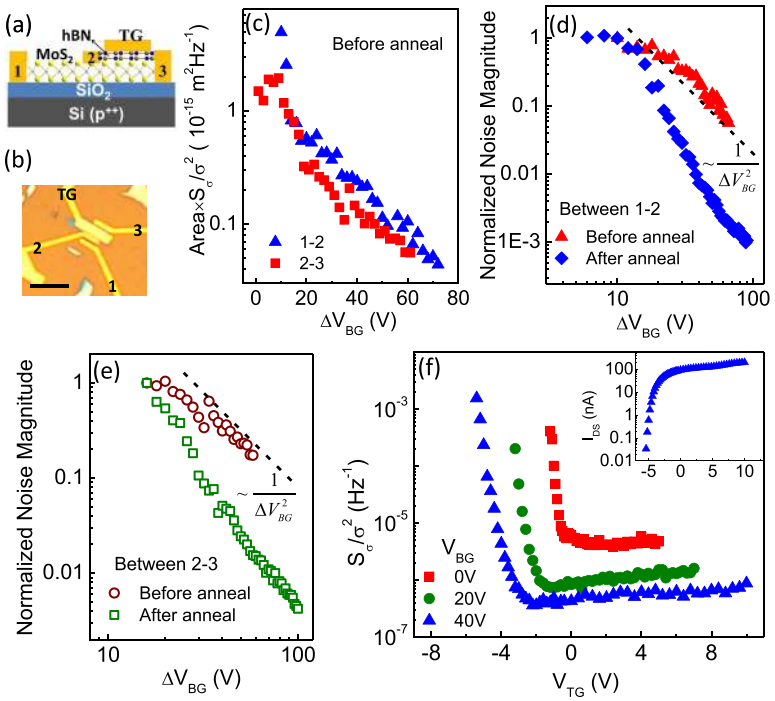

FIG. 4. (a) Schematic and (b) optical micrograph of a device consists of two 2-probe channels on the same flake. The region between 1 and 2 was exposed to external trapping-detrapping agents. The region between 2 and 3 was protected with hBN. (c) Comparison of area-normalized noise magnitude of 1 and 2, and 2 and 3 regions as a function of carrier density before annealing. Comparison of noise magnitude before and after annealing for (d) 1 and 2 (e) 2 and 3 channel regions. The S_σ/σ^2 was normalized with its values at $\Delta V_{BG} = 10$V and 16 V in Figs. 4(d) and 4(e), respectively. The black dashed lines indicate $1/\Delta V_{BG}^2$. (f) S_σ/σ^2 as a function of top gate voltage at different $V_{BG} = 0$, 20, 40 V. Inset: Drain-source current as a function of top gate voltage at fixed $V_{BG} = 40$ V.

trap states inside the channel due to sulphur vacancies can slowly exchange carrier to contribute to noise.[20,29–31] Moreover, as mentioned earlier, all our devices were measured in high vacuum which ensures significant, but not entire, removal of the adsorbed water vapour from the surface of channel, and thus, remaining adsorbate can also affect the noise level. Conductivity fluctuations can also happen at the contact due to presence of spatially inhomogeneous Schottky barrier.[32] In order to address the contribution from the above-mentioned factors, we fabricate devices by transferring a thin (∼20 nm) single crystalline layer of hBN on top of the MoS_2 flake prior to lithography processes. Such encapsulation protects the channel from acrylic residues, and the possibility of the presence of water vapor is also minimal as the transfer was done at 120 °C. Here we present the data from a typical device where two 2-probe channels were fabricated on the same MoS_2 flake. A schematic and an optical micrograph of the device is shown in Figs. 4(a) and 4(b), respectively. The channel between probe 1 and probe 2 was exposed to fabrication-induced atmospheric contaminations, whereas the part between 2 and 3 was protected by hBN. We could not perform noise measurement in ambient condition in the unprotected channel due to large relaxation of I_{DS} in the time scale of noise data acquisition (see Fig. S4 of the supplementary material[13]). Therefore, we evacuated the cryostat to $\approx 10^{-6}$ mbar vacuum, and performed conductivity and noise measurement (see Fig. S5 of the supplementary material[13] for transfer characteristics). The carrier mobilities of the protected and unprotected channels were ∼ 4 and ∼ 3 cm^2/Vs, respectively. The noise magnitude normalized by the device area in both channels are compared at similar carrier density in Fig. 4(c). We observe that the noise from unprotected channel is only slightly ($\lesssim 50\%$) higher than that from the protected channel. This may be because of the contribution from acrylic residues, and residual water vapour remaining on the as-fabricated unprotected channel. In the next step, we anneal the device at 150 °C for 2 h in high vacuum condition. The conductivity and noise measurements were performed

after cooling the device to room temperature. The transfer characteristics for both channels after annealing are shown in the supplementary material[13] (see Fig. S5). We found that in all cases, the V_{ON} shifted towards large (< -60 V) negative gate voltages after annealing. This has been observed previously, but the reason behind this remain controversial.[17] The noise behavior of unprotected, and protected channels before and after annealing are plotted in Figs. 4(d) and 4(e), respectively. For comparison, we plot S_σ/σ^2 normalized to its magnitude at $\Delta V_{BG} \approx 10$ V as a function of ΔV_{BG}. We observe that both the channels, in spite of having very different surface conditions, show $10 - 30$ times decrease in noise magnitude after annealing. Assuming that annealing at 150 °C can only remove residual water vapour, adsorbed molecules, and not polymer residues, such large change cannot be accounted for by the desorption of atmospheric contaminants.

We now discuss two possibilities that may account for the large decrease in noise on annealing: (1) reduction in the localized trap states inside the channel and (2) modifications in the metal-MoS_2 contacts. It is well-known that the defects in MoS_2 arises due to sulphur vacancies and interstitial,[26] and are stable till $\sim$1000°C.[17] Therefore, we exclude the former as the mechanism of noise reduction by annealing. On the other hand, it is well-established that, in the space-charge region of metal-semiconductor interface, random occupancy of the trap states can lead to low-frequency noise, for example, via fluctuations in the Schottky barrier height.[33] In case of MoS_2, however, the defect states created at the metal-MoS_2 interface has been suggested to be intrinsic in nature that could also cause a strong lowering of the local Schottky barrier.[26,29] The sensitivity of transport to annealing indicated these to be significantly lower in energy, the reduction of traps on annealing increases both the transparency of the contacts,[1,9] as well as the overall noise level in these devices.

To obtain a more direct evidence of the role of contacts, we measure the noise in MoS_2 devices with both backgate and top gate (denoted as TG in Fig. 4(b)). The thin (20 nm) hBN layer played the role of top gate dielectric apart from surface protection. The noise measurements were performed as a function of top gate voltage (V_{TG}) keeping the backgate at a constant voltage. The backgate induces carriers in MoS_2 both below the contact pads and the channel region between the contacts, and we used V_{BG} to change the transparency of the contacts. The top gate, on the other hand, influences only the channel region between the contacts, and can drive the transistor on/off due to its stronger capacitative coupling. The transfer characteristics of the device as a function of top gate voltage keeping $V_{BG} = 40$ V is shown in the inset of Fig. 4(f). We observe that the transfer characteristics saturates at high V_{TG} due to contact resistance. The variation of noise as a function of V_{TG} at three different V_{BG} are shown in Fig. 4(f). We observe that at high carrier density, where the transfer characteristics is dominated by the contacts, noise becomes a weak function of V_{TG}.[11] The data at $V_{BG} = 0$, 20, and 40 V (Fig. 4(f)) clearly indicate that the transparency of the contacts significantly affects the measured noise, and can lift the noise level even by orders of magnitude in these devices. Alternatively, in the low V_{TG} regime (for example, $V_{TG} < -2$ V at $V_{BG} = 40$ V), where the channel resistance dominate over contact resistance, we find that even though the contact barriers are highly transparent due to high V_{BG}, noise magnitude increases rapidly with decreasing V_{TG}. This indicates that the channel contribution to noise is dominant in this regime which may originate due to strong localization of carriers in the channel.[8,29]

In conclusion, we investigate the origin of the low frequency $1/f$ noise in MoS_2 devices. Our measurement suggest that, along with the external trapping-detrapping centers, metal-MoS_2 contacts play a significant role in determining the noise magnitude in these devices. The dramatic decrease in noise after vacuum annealing is probably due to large increase in the transparency of the contacts rather than the removal of surface contaminations. We conclude that highly transparent contact along with channel encapsulation is essential to implement MoS_2 in low noise applications.

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