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MICROWATT SWITCHED CAPACITOR CIRCUIT DESIGN†

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The micropower CMOS implementation of the three basic components of switched capacitor circuits is discussed. Switches must be carefully designed to allow low voltage operation and compensation of clock feed-through by dummy transistors. Matched capacitors can be implemented in single polysilicon technologies primarily designed for digital micropower circuits. Excellent micropower amplifiers are realized by using simple one-stage circuits which take advantage of the special behaviour of MOS transistors in weak inversion. Noise is shown to be independent of current level which only influences the settling time. Various ways of improving the settling time while keeping a very low current drain are described. A method of calculating the noise of a biquadratic filter is followed by examples of a filter and of other switched capacitor circuits.

1. INTRODUCTION

Energy must be saved in battery-operated instruments. This is mandatory in electronic watches where the average power available is only a few microwatts. Micropower operation is required or desirable in various other portable instruments such as paging receivers, hearing aids, implanted biomedical devices, and devices for environment and security control.[1]

Switched capacitor circuits have not yet been effectively used in watch circuits, but they start appearing in DC handling circuitry (controlled voltage generation, battery voltage checking). Furthermore, SC filters are considered for word recognition systems to be incorporated in watches. Micropower filters are required to enhance pulses delivered by the heart in pacemakers and will be needed in future portable devices to process analog signal delivered by sensors. A dynamic range of 60 to 80 dB is acceptable in such applications, but the current drain must be kept below 1 to 10 μA with a single supply voltage V_{cc} lower than 3 V.

CMOS is ideally suited for micropower, and Si-gate has some advantages over Al-gate, mainly because of its self-alignment properties.

Analog subcircuits, including SC circuits, must be compatible with standard technologies that are optimized for digital applications.

After a brief review of the behaviour of MOS devices at very low current, this paper will discuss the CMOS implementation of the three basic components of SC circuits (switches, matched capacitors, amplifiers) in the context of low power and low voltage. Some emphasis will be put on the realization of amplifiers and on the trade off between low power, settling time and noise considerations. Large parts of this discussion are derived from reference[2].

The low power realization of complete filters and other SC circuits will be illustrated with specific examples.

2. MOS TRANSISTOR AT LOW CURRENT

When the drain current of a MOS transistor is decreased by reducing the gate voltage, the device eventually enters the weak inversion region of operation where the usual parabolic transfer characteristics are no longer valid. For long channel transistors with a negligible density of fast surface states and negligible leakage current to substrate, the drain current I_D in weak inversion may be expressed as[3]

$$I_D = S\, I_{DO}\, e^{V_G/nU_T} \left(e^{-V_S/U_T} - e^{-V_D/U_T}\right) \quad (2.1)$$

where S is the effective channel width to channel length ratio; V_G, V_S and V_D are the gate, source, and drain potentials with respect to the substrate, and $U_T = kT/q$. The slope factor ($n > 1$) is fairly controllable, whereas the characteristic current I_{DO} is very sensitive to process parameters and temperature. Both n and I_{DO} may be considered constant for all transistors of a chip biased by values of V_S that do not differ too much from each other.

This model expresses the fact that a MOS transistor in weak inversion is a barrier-controlled device very similar to a bipolar transistor. Drain current I_D becomes saturated as soon as V_D-V_S exceeds a few U_T. This behaviour helps to maximize the dynamic range of amplifiers. The saturation value of I_D in-

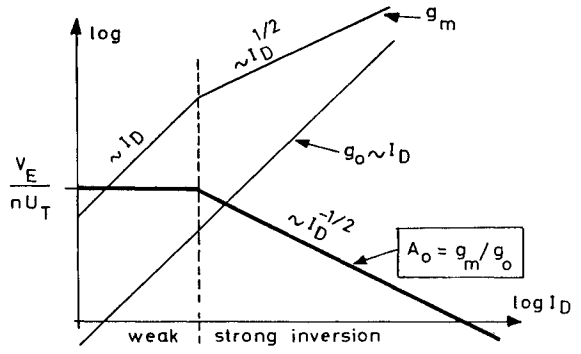


FIGURE 2.1 Amplification factor.

creases exponentially with $-V_S/U_T$ and V_G/nU_T.

The maximum saturation current in weak inversion is roughly given by[3]

$$I_D = \beta U_T^2 \tag{2.2}$$

where $\beta = \mu c_{ox} S$ is the usual transfer parameter in strong inversion. The maximum value of β achievable with a transistor of reasonable size (0.02 mm^2) is about 10 mA/V^2 which corresponds to a maximum possible operating current in weak inversion of a few microamperes. For a typical, minimum-sized transistor, this limit is between 10 and 100 nA.

Small-signal gate to drain transconductance is easily derived from the model as

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{I_D}{nU_T} \tag{2.3}$$

Transconductance is proportioned to drain current I_D in weak inversion, whereas it is proportional to $I_D^{1/2}$ in strong inversion.

For $V_D - V_S \gg U_T$, a source to drain transconductance may be defined as

$$g_{ms} = -\frac{\partial I_D}{\partial V_S} = \frac{I_D}{U_T} \tag{2.4}$$

This transconductance is n times larger than that of the gate and is equal to that of a bipolar transistor operated at the same current.

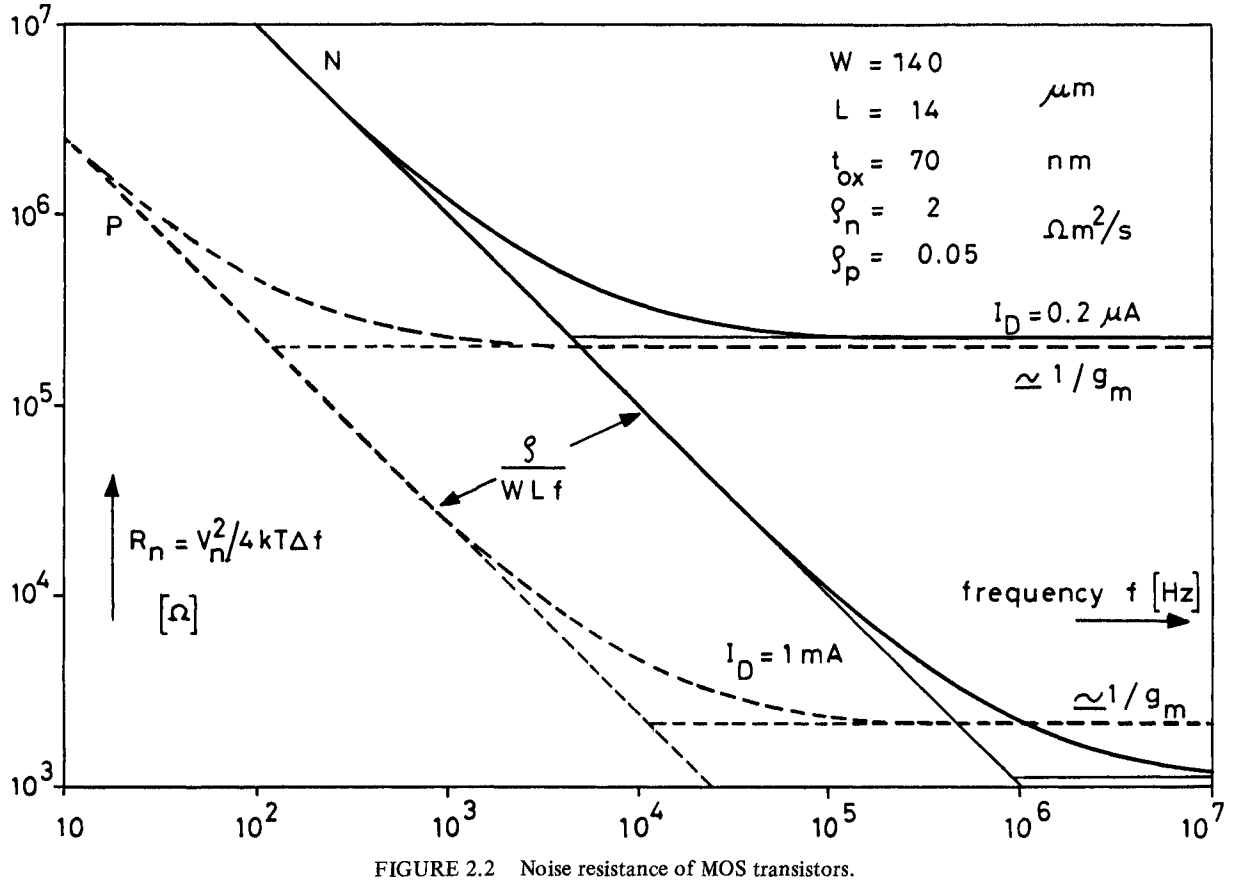


FIGURE 2.2 Noise resistance of MOS transistors.

The maximum small signal amplification achievable with a transistor is limited by the non-zero output conductance g_0 of the device, which is due to channel shortening. This conductance is approximately proportional to drain current and may be characterized by an extrapolated voltage V_E roughly proportional to channel length, with

$$g_0 = I_D/V_E \tag{2.5}$$

As shown in Figure 2.1, the amplification factor $A_0 = g_m/g_0$ has a maximum value

$$A_0 = V_E/nU_T \tag{2.6}$$

in weak inversion, but it decreases like $I_D^{-1/2}$ in strong inversion. This maximum possible gain in weak inversion reflects the maximum of the transconductance-to-current ratio. It may be further increased by increasing the channel length of the transistor.

Noise is a limiting factor for transistors used in amplifiers. It may be conveniently characterized by a frequency dependent noise resistance R_n which is a measure of the input noise voltage spectrum.

Figure 2.2 shows typical noise resistances of large transistors integrated in micropower Si-gate technology.[4,5] At high frequency, shot noise dominates; the noise resistance is independent of frequency and approximately equal to the inverse of transconductance g_m. It increases if drain current is decreased, but it is minimum at a given current if the transistor is in weak inversion.

At low frequencies, flicker noise dominates. The noise resistance is inversely proportional to frequency and to gate area WL. It also depends on the technology through the parameters ρ.

The flicker noise resistance of a p-channel transistor is about 40 times smaller than that of a n-channel transistor of the same size.

3. SWITCHES

Switches in SC-circuits are realized by means of n and/or p channel transistors. They are switched on and off by connecting their gates to the most positive or to the most negative potential available, namely V_{cc} or 0 (Figure 3.1)

For both types of transistors, the on-conductance g of the switch is a function of its voltage level V_L with respect to 0. If the current in weak inversion is neglected, g is given by

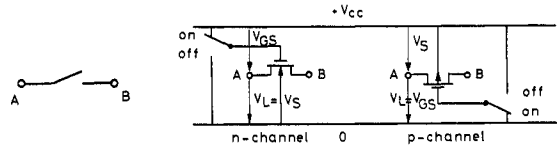


FIGURE 3.1 MOS transistors used as switches.

$$g = \frac{W}{L}\,\mu\, c_{ox}\,(V_{GS} - V_T) \tag{3.1}$$

with

$$V_T = V_{T0} + K\,(\sqrt{2\phi_B + V_S} - \sqrt{2\phi_B}) \tag{3.2}$$

$$\phi_B = U_T \ln \frac{N_B}{n_i} \tag{3.3}$$

$$K = \frac{1}{c_{ox}}\sqrt{2q\,\epsilon_s\,N_B} \tag{3.4}$$

Results for a typical low voltage technology are shown in Figure 3.2 for 2 values of V_{cc}. For V_{cc} = 3 V, a complementary switch can be maintained in the on-state at any level V_L. If V_{cc} is only 1.5 V, there is a range of V_L over which neither of the 2 transistors is conducting. Because of substrate modulation ($K \neq 0$), the critical value of V_{cc} below which this gap appears ($\sim$ 2.3 V in this example) is much higher than the sum of p and n thresholds for $V_S = 0$ (1.3 V in this example).

Operation at 1.5 V can be achieved if c_{ox} is increased to 450 pF/mm^2, which reduces V_{T0} and K for both types of transistors.

Current leakage to ground is smaller than 1 pA at room temperature and is usually negligible compared to residual channel current in the off-state of the switch. This residual current may be as high as a few 10^{-10} A for low values of V_T, and puts a lower limit on the clock frequency.

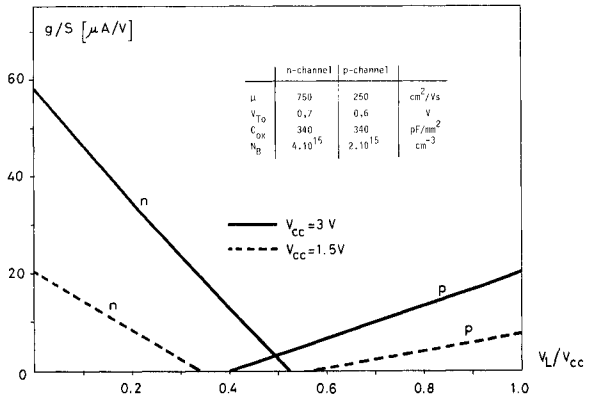


FIGURE 3.2 On-conductance of p and n switches.

Clock feed-through is usually not bothersome with respect to AC signals, but it may be a serious limitation to the capability of handling small DC signals. It may be reduced by means of a dummy transistor,[6] under the assumption that half the parasitic charge stays at each end of the switched-off transistor.

The validity of this assumption may be examined by the simple circuit of Figure 3.3.

The gate voltage is assumed to decay linearly with time t from its initial value V_{Go} : $v_G = V_{Go} -$ at (3.5)

A rough model of this circuit valid for small values of v_1 and v_2 is shown in Figure 3.4. where

$$I_c = \frac{a\, C_{Gmax}}{2} \quad (v_G > V_T) \tag{3.6}$$

is the current due to clock feed-through, assumed to be equally injected into both ends of the transistor as long as there is an inverted channel. The overlapping capacitances which remain for $v_G < V_T$ inject an additional but symmetrical charge which can be considered independently.

$$g = \beta(v_G - V_T) \tag{3.7}$$

is the conductance of the transistor, which is responsible for an undesired exchange of charge between C_1 and C_2 during the decay of gate voltage.

By introducing 3.5, 3.6, and 3.7 in the equations of the network, one obtains the normalized equation:

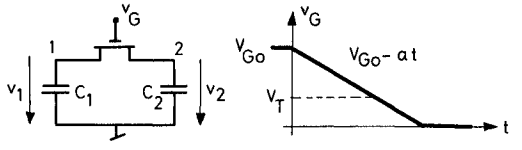


FIGURE 3.3 Switch connecting two capacitors.

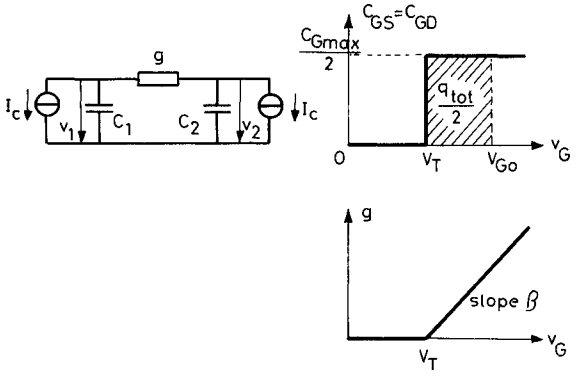


FIGURE 3.4 Model for calculation of clock feed-through.

$$\frac{dV_1}{dT} = (T - B)\,[(1 + R)\,V_1 + 2\,RT] - 1 \tag{3.8}$$

with

$$V_1 = v_1 \Big/ \frac{C_{Gmax}}{2}\sqrt{\frac{a}{C_1\beta}} \tag{3.9}$$

$$T = t/\sqrt{\frac{C_1}{a\beta}} \tag{3.10}$$

$$B = (V_{Go} - V_T)\sqrt{\frac{\beta}{aC_1}} \tag{3.11}$$

$$R = \frac{C_1}{C_2} \tag{3.12}$$

One may assume V_1 (= V_2) = 0 for T = 0. The final value $V_{1\infty}$ of V_1 is obtained by numerical integration of 3.8 with T increasing from 0 to B. The result is plotted as a function of B in Fig. 3.5 for various values of the capacitance ratio R.

A symmetrical distribution of total charge q_{tot} is ensured if $C_1 = C_2$,[7] but such a symmetrical structure is not always realizable. For $C_1 \neq C_2$, a symmetrical distribution is only achieved for low values of the parameter B.

Experimental results confirm this behaviour, provided $|v_1 - v_2| \ll U_T$. If this condition is not fulfilled, the effect of the longitudinal field in the channel cannot be neglected with respect to that of diffusion, and a charge larger than $q_{tot}/2$ flows in the larger capacitor even for a very small B (abrupt transition of v_G).

The power needed to drive the switches is of the order of a few nanowatts per transistor for V_{cc} = 3 V and a clock frequency of 32 kHz. It may generally be neglected.

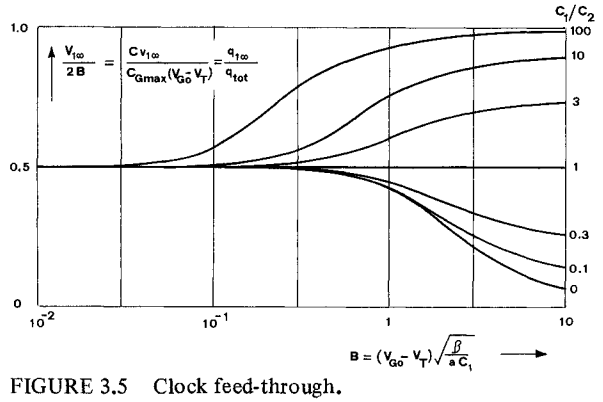


FIGURE 3.5 Clock feed-through.

4. MATCHED CAPACITORS

In metal gate technology, the best capacitor available

is the gate to diffusion structure, which has a fairly high specific value (300-500 pF/mm^2) due to the thin gate oxide.

This capacitor is not available in standard Si-gate technology, due to self-alignment of gate and diffusion.

The gate-to-p-well capacitor suffers from the well-known dip characteristic of any MOS capacitor and therefore cannot be used for the implementation of accurate capacitance ratios. The only possibility which remains in standard Si-gate technology (single poly-silicon layer) is the polysilicon-to-aluminium capacitor shown in Figure 4.1. It has a specific value of the order of 100 pF/mm^2. To each capacitor is associated a parasitic capacitor C_p of about 30 pF/mm^2 between polysilicon layer and ground.

The accuracy of the ratio of two physically identical capacitors has been measured as a function of the value of these capacitors. Results are shown in Figure 4.2.

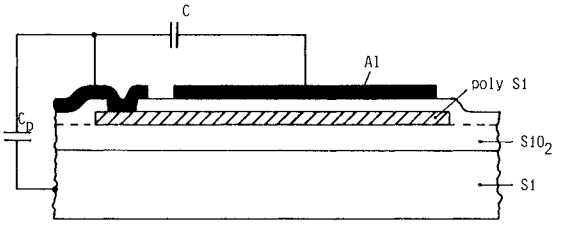
Accurate values of capacitance ratio different from 1 are obtained by grouping different numbers of identical elementary capacitors. The accuracy will then be mainly determined by the smaller of the 2 resulting capacitors.

Switching noise associated with every switched capacitor may be explained by means of Figure 4.3. The charge transferred from voltage source V_A to voltage source V_B during each cycle of the switch is equal to $C(V_A - V_B) + C(\delta V_a - \delta V_B)$, where δV_A and δV_B are instantaneous thermal noise voltages of resistances R_A and R_B in the bandwidth limited by C. Since the switch stays in both positions for a period of time longer than $R_{A(B)}C$, δV_A and δV_B both have a variance equal to kT/C.

Since they are not correlated, the noise charge transferred during each cycle has a variance 2 kT C. Noise voltage samples of variance

$$V_n^2 = 2\,kT/C \qquad (4.1)$$

are thus added to the signal by each switched capacitor



C = 70-150 pF/mm^2
C_p/C = 0,2 to 0,5

FIGURE 4.1 Aluminium-polysilicon capacitor.

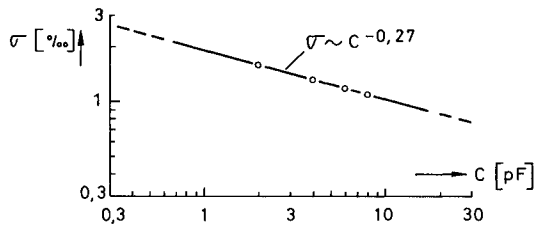


FIGURE 4.2 Matching of 2 identical capacitors.

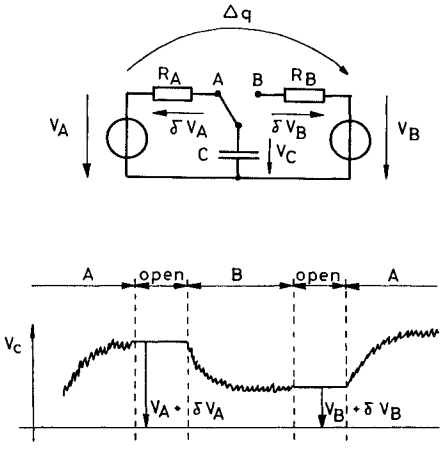


FIGURE 4.3 Switched capacitor.

of value C. This source of noise may become predominant if values of capacitors are kept low in order to limit the size of the circuit and the current level in the amplifiers.

It may be noted that the noise voltage given by 4.1 is equal to that of the equivalent resistance $1/f_cC$ (f_c is the clock frequency) in the bandwidth $f_c/2$.

5. AMPLIFIERS

Most of the power of a SC circuit is consumed in the operational amplifiers. They must therefore be specially designed for very-low-power applications. One basic principle is to use simple circuits which take advantage of the excellent behaviour of MOS transistors in weak inversion. Furthermore, battery operation allows more relaxed requirements on power supply rejection, since all power noise is generated on the chip and may be more easily filtered out at very low current.

A first amplifier which has been used in micro-power SC filters is shown in Figure 5.1. It combines a n-channel differential pair $T_1 - T_3$ and a p-channel current mirror $T_2 - T_4$ to achieve voltage amplifica-

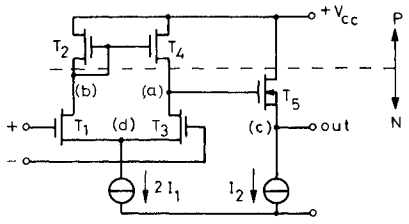


FIGURE 5.1 Single stage amplifier.

tion at a high impedence node (a). A n-channel source follower T_5 provides a low output resistance. This transistor must be put inside a separate p-well connected to its source to avoid any reduction of gain and voltage swing by bulk modulation.

Figure 5.2 shows the measured frequency dependence of the gain A of such an amplifier driven at the negative input, with $2I_1 = 0.1\ \mu A$, $I_2 = 1\ \mu A$ and a total capacitive load $C_c = 5$ pF at the output node C. This circuit behaves essentially as an integrator with a time constant

$$\tau_1 = C_a/g_{m1} \tag{5.1}$$

where C_a is the capacitance loading node (a) and g_{m1} the transconductance of transistors T_1 and T_5. It has a significant pole due to the time constant

$$\tau_2 = C_c/g_{m5} \tag{5.2}$$

at output C.

The high frequency gain may thus be approximated by

$$A = \frac{1}{s\tau_1(1 + s\tau_2)} \tag{5.3}$$

The DC gain A_0 is limited by channel shortening effects on transistors T_4 and T_3. Due to weak inversion operation, this single stage amplifier achieves a gain close to 60 dB with channel lengths of T_3 and T_4 of the order of 20 μm. The gain can be easily increased to more than 80 dB by replacing each one of transistors T_3 and T_4 by cascode pairs.[8]

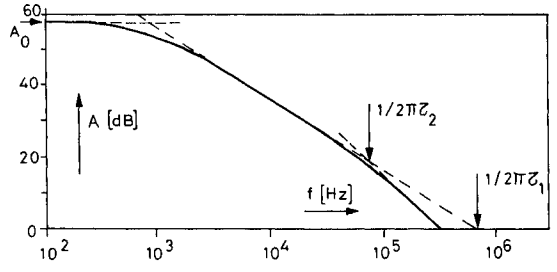


FIGURE 5.2 Measured gain of amplifier.

Amplifiers of SC circuits operate with an amount of voltage feedback β close to unity.

The settling time T_s necessary to reach equilibrium with a residual error ϵ, after application of a small unit step, may be easily computed if the gain is given by relation 5.3. Results are shown in Figure 5.3 for 2 values of ϵ.

The solution is oscillatory for $\beta\tau_2/\tau_1 > 0.25$ (5.4)

The settling time T_s may be approximated on either side of this limit by:

$$T_s \cong 2\,\tau_2 \ln \epsilon^{-1} \text{ (oscillatory)} \tag{5.5}$$

$$T_s \cong \frac{\tau_1}{\beta} \ln \epsilon^{-1} \tag{5.6}$$

The maximum useful settling accuracy is obtained when $\epsilon < 1/A_0$. It can be pointed out that no compensation capacitor is required to insure stability of such a single stage amplifier. If the amplitude ΔV_i of the input step is large, the settling time is increased by the maximum possible slewing rate of nodes (a) or (c). This additional time T_{sr} is approximately given by the larger of

$$T_{sr} = \frac{C_a}{2\beta I_1}\Delta V_i \text{ or } \frac{C_c}{\beta I_2}\Delta V_i \tag{5.7}$$

and may be significant for ΔV_i larger than a few tenths of a volt.

Figure 5.4 shows the input noise voltage spectral density, measured on the same amplifier.

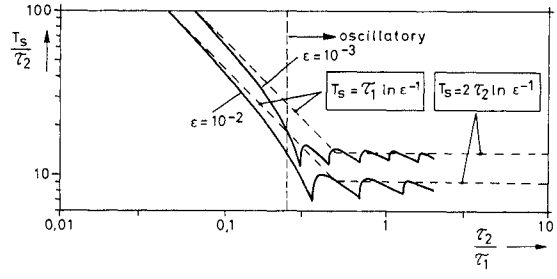


FIGURE 5.3 Small signal settling time.

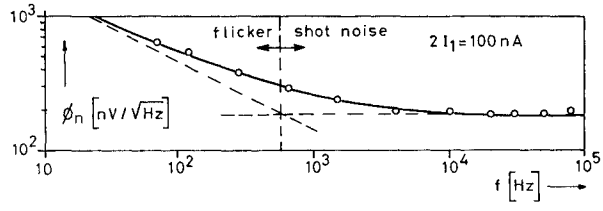


FIGURE 5.4 Input noise of the amplifier.

At low frequencies, flicker noise of input transistors T_1 and T_3 dominates. The noise voltage in the range 1 Hz to 3 kHz is approximately 20 μV.

At high frequencies, shot noise dominates and is independent of frequency. We have seen previously that the equivalent noise resistance at the input of a single transistor has a value close to the inverse of its transconductance. The input noise voltage of the amplifier in a bandwidth Δ f may thus be expressed as

$$V_n^2 = 4\,\gamma kT\,\Delta f/g_{m1} \tag{5.8}$$

where γ is a factor ranging from 1 to 4 in most practical situations. In a SC filter, all the high frequency noise is transposed to low frequencies by undersampling.

The noise bandwidth Δf is therefore that of the amplifier which is given by

$$\Delta f = \int_0^\infty |1 + 1/A\beta|^{-2}\,df \tag{5.9}$$

With a gain A given by relation 5.3, integration of 5.9 yields

$$\Delta f = \beta/4\,\tau_1 \tag{5.10}$$

The noise bandwidth is independent of the time constant τ_2. Combination of 5.10, 5.8 and 5.1 gives the input noise (variance of voltage noise samples at the input of the amplifier):

$$V_n^2 = \gamma\beta kT/C_a \tag{5.11}$$

The amount of shot noise introduced by the amplifier is thus inversely proportional to the capacitance C_a at node (a), but *independent* of the currents I_1 and I_2.

Noise can thus be reduced by increasing C_a, but this increases the settling time T_s given by 5.6. In any case, T_s must be shorter than the half clock period $1/2\,f_c$; this puts a limit on the minimum input noise. It can be obtained by combining 5.1, 5.6 and 5.11:

$$V_n^2 > 2\,kT\,\frac{f_c}{g_{m1}}\,\gamma \ln \epsilon^{-1} \tag{5.12}$$

Due to the requirement on settling time, the minimum noise is thus inversely proportional to transconductance g_{m1}; it is therefore increased at low current. If input transistors T_1 and T_3 operate in weak inversion, this limit reaches a minimum value (for I_1 fixed):

$$V_n^2 > \frac{2\,q\,f_c}{I_1}\,U_T^2\,n\,\gamma \ln \epsilon^{-1} \tag{5.13}$$

It is interesting to point out that $I_1/2\,q\,f_c$ is the number of elementary charges which flow through the input transistors during every half clock period.

An increased value of the external capacitive load affects τ_2 and increases therefore the settling time T_s as soon as $\tau_2 > \tau_1/4\,\beta$ (according to relation 5.4). However, it has no effect on the equivalent input noise which can only be reduced by increasing the capacitive load at the high-impedance amplifying node (a). This suggests that one achieves voltage amplification at the output node, or in other words, uses an operational transconductance amplifier (OTA).

Figure 5.5 shows a micropower OTA.[9] It includes a cascode output stage which only reduces the output swing by about 200 mV (since V_{DSsat} < 100 mV in weak inversion), but achieves a DC gain larger than 95 dB. For V_{cc} = 3 V and a supply current of 2.5 μA, the gain-bandwidth product is 135 kHz with a 10 pF load, but the slew rate is only 0.1 V/μs.

All these amplifiers are able to settle in closed loop within a short period of time inspite of their very low power consumption. However, for large input steps, the settling time may be increased considerably by the very small slew rate limited by the small bias current.

This fundamental limitation can be circumvented by means of amplifiers which operate in class AB, and are therefore able to supply currents much larger than their standby bias current.

As first possibility, one may use adaptive biasing schemes such as the one shown as an example in Figure 5.6.

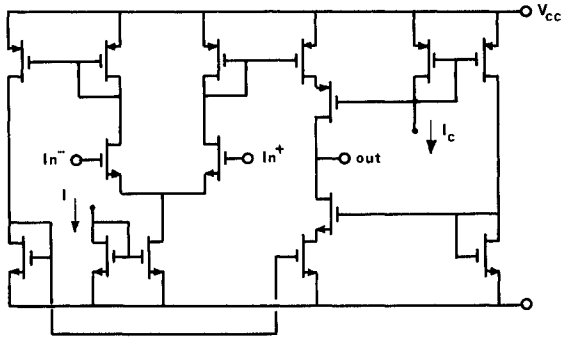


FIGURE 5.5 Cascode OTA.

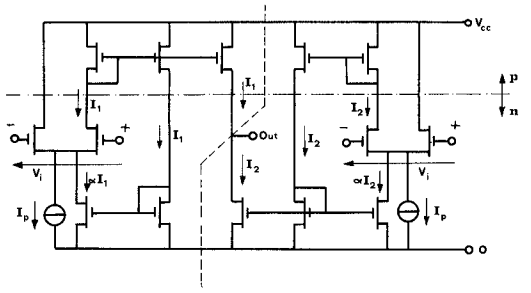


FIGURE 5.6 Adaptive biasing amplifier.

This amplifier combines two symmetrical variable current sources I_1 and I_2. Each of them includes a differential pair, the long tail current of which is the sum of a constant bias current I_p and a current αI_1 (αI_2) which is proportional to its output current.

When the differential input voltage $V_i = 0$,

$$I_{1(2)} = \frac{1}{2}(I_p + \alpha I_{1(2)})$$

thus

$$I_1 = I_2 = I_0 = \frac{I_p}{2-\alpha} \qquad (5.14)$$

Stability is ensured if $\alpha < 2$.

When $V_i > 0$, I_1 increases. Due to positive feedback, I_1 may reach a value much larger than I_0. This is true as well for I_2 when $V_i < 0$. For operation in weak inversion, simple calculations yield

$$I_{1(2)} = \frac{I_p}{(1-\alpha) + e^{-(+)V_i/nU_T}} \qquad (5.15)$$

which is represented in Figure 5.7 for various values of α.

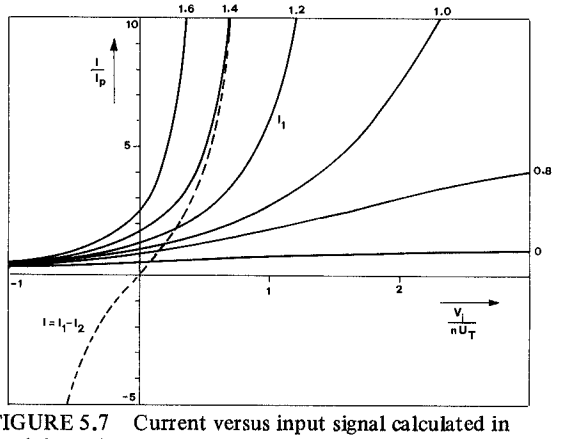


FIGURE 5.7 Current versus input signal calculated in weak inversion.

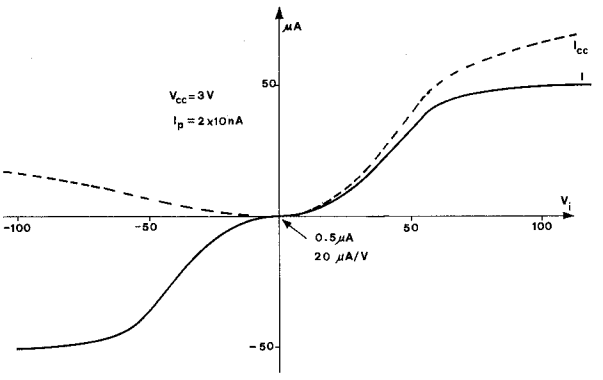


FIGURE 5.8 Experimental results.

The efficiency of the circuit can be improved by increasing the width to length ratio of the output transistors.

Experimental results on such a circuit are shown in Figure 5.8.

Another kind of amplifier operating in class AB is based on the simple CMOS inverter as explained by Figure 5.9.[10]

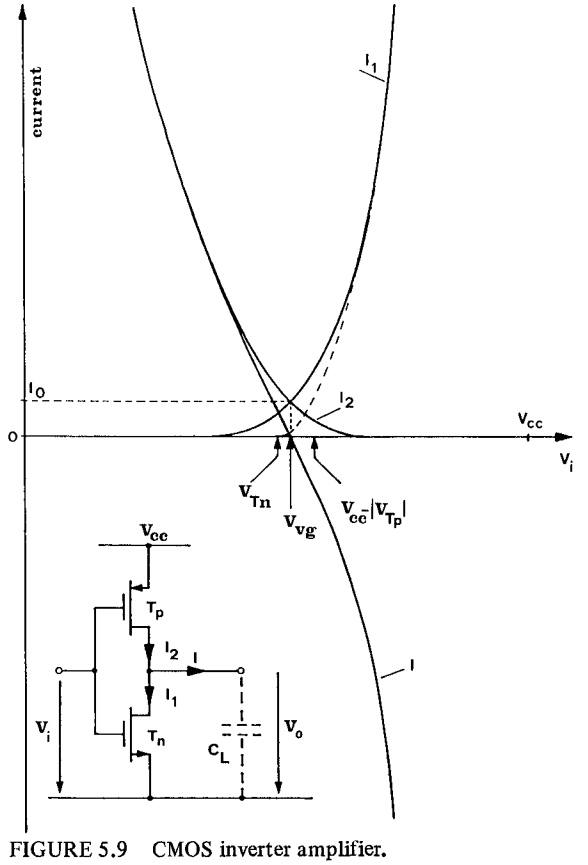


FIGURE 5.9 CMOS inverter amplifier.

The variation of drain currents I_1 and I_2 of the two complementary transistors T_p and T_n of an inverter are plotted in this figure as functions of input voltage V_i, for any value of output voltage V_o that insures saturation of both transistors. For small values of V_i, T_n operates in weak inversion and I_1 increases exponentially. When V_i approaches the threshold V_{Tn} of T_n, operation gradually changes to strong inversion characterized by the usual parabolic law shown by a dotted line. I_2 behaves similarly with respect to V_{cc}-V_i.

$I = I_2 - I_1$ is the current available to charge or discharge a capacitive load C_L. For $V_i = V_{vg}$, $I_1 = I_2 = I_0$. V_{vg} is thus the virtual ground potential of this transconductance amplifier.

For small variations around V_{vg}, the amplifier behaves linearly with a transconductance g_m equal to the sum of the transconductances of T_n and T_p biased at I_0. Its phase margin is 90° for any value of C_L, which insures a non-oscillatory settling behaviour, with a unity-gain time constant $\tau = C_L/g_m$.

The ratio g_m/I_0 is maximum if both transistors are in weak inversion at current I_0. This results in a maximum voltage gain, as well as minimum noise and time constant τ achievable with a current I_0.

Furthermore, both transistors remain saturated for very low values of drain to source voltage, which allows an output voltage swing close to V_{cc}. Voltage gain may be further increased by the addition of cascode transistors.

For large input steps V_i-V_{vg}, output current |I| may widely exceed I_0. This eliminates any slew rate limitation.

Some circuitry must be added to the basic CMOS inverter-amplifier in order to control its bias current I_0, and to attenuate the effect of power supply variations.

A first possibility is depicted in Figure 5.10. The supply voltage V_{cc} of all amplifiers in a filter is maintained at the required value by means of an identical inverter T_{no}-T_{po} biased with current I_0. The ground potential V_{vg} is available from this reference inverter. Additional grounds may be obtained by short-circuiting input and output of some of the amplifiers. The whole circuit must be fed at a voltage higher than V_{cc} to allow correct operation of the follower-amplifier A.

The value of V_{cc} for small signal bias in weak inversion is approximately equal to the sum of p and n-channel thresholds.

The link between threshold voltages and supply voltage is eliminated in the circuit represented in Figure 5.11. Bias current I_0 is imposed independently of V_{cc} by a current mirror T_b-T_p ($T_b \equiv T_p$). The behaviour of this circuit is similar to that of an

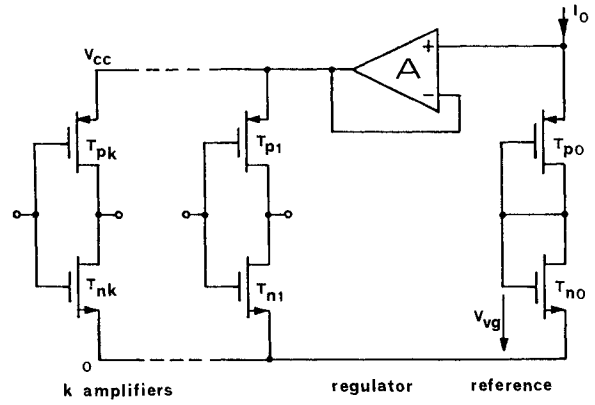


FIGURE 5.10 Regulation of V_{cc}.

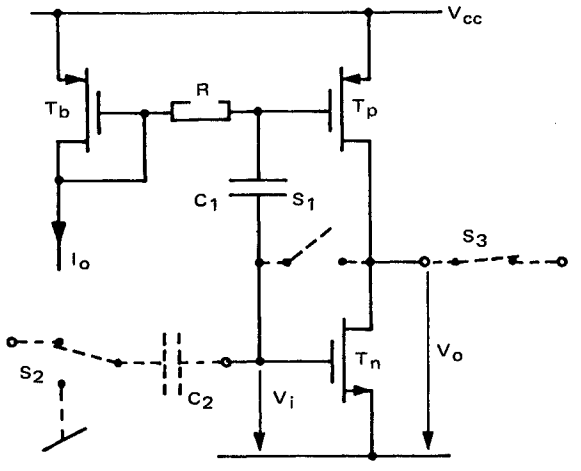


FIGURE 5.11 AC coupled CMOS inverter-amplifier.

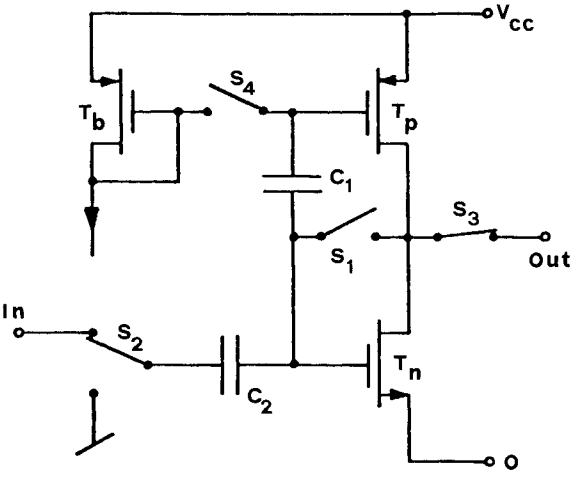


FIGURE 5.12 CMOS inverter-amplifier with dynamic bias.

inverter for input signals of frequencies much higher than $1/RC_1$. The high value resistance R may be implemented by means of lateral diodes in the polycrystalline gate layer.[3] The value of V_{vg} is close to V_{Tn}. It may be moved to the desired level by the addition of a capacitor C_2 and switches S_1, S_2 and S_3. A biasing phase is provided during which S_1 is closed, S_3 is opened and S_2 is connected to the required ground level.

This circuit cannot reject supply voltage variations at frequencies above $1/RC_1$. This drawback is eliminated in the slightly different circuit shown in Figure 5.12.

Resistance R has been replaced by a switch S_4 which is closed during the biasing phase.

The current drain I_{cc} of amplifiers which operate in class AB is approximately given by

$$I_{cc} = I_0 + f_c C_L \Delta V_0 \qquad (5.16)$$

where I_0 is the standby bias current, C_L the capacitive load and ΔV_0 the average output swing.

6. MICROPOWER SC FILTERS

In order to minimize the power consumed in the amplifiers, their load capacitance must be as low as permitted by noise considerations. The value of all fixed and switched capacitors must therefore be low. Structures which are insensitive to stray capacitances are therefore required to achieve accurate filtering characteristics.

The dynamic range of the whole filter is limited by the amplifiers. It is usually maximum when the signal level is the same at the output of all amplifiers.

The transfer function from any branch i of a filter to its output may be expressed as

$$W_i(z) = \sum_{k=0}^{\infty} w_{ik} z^{-k} \qquad (6.1)$$

where w_{ik} is the k^{th} term of the impulse response from this branch. Thus, if successive samples of a noise source V_{ni} in branch i are not correlated, the contribution V_{no}^2 to output noise of this source is given by

$$\frac{V_{no}^2}{V_{ni}^2} = \sum_{k=0}^{\infty} w_{ik}^2 = \frac{1}{2\pi j} \oint_{\substack{\text{unit} \\ \text{circle}}} W_i(z)\, W_i(z^{-1})\, z^{-1}\, dz \qquad (6.2)$$

If W(z) is biquadratic, given by

$$W_i(z) = \frac{a_2 z^2 + a_1 z + a_0}{z^2 + b_1 z + b_0} \qquad (6.3)$$

application of the residue theorem to integral 6.2 yields:

$$\frac{V_{no}^2}{V_{ni}^2} = \sum_{k=0}^{\infty} w_{ik}^2 = \qquad 6.4$$

$$\Big((1+b_0)(a_0^2+a_1^2+a_2^2) - 2a_1 b_1 (a_0+a_2) + a_0 a_2$$
$$(1+1/b_0)(b_1^2 - b_0^2 - 1)\Big) / (1-b_0)(1-b_1+b_0)$$
$$(1+b_1+b_0)$$
$$+ \frac{a_0 a_2}{b_0}$$

Figure 6.1 shows as an example the circuit diagram of a second-order stray-insensitive low-pass filter which has been realized for micropower applications.[2]

The various noise sources V_{ni} are also represented on this diagram. V_{n1} and V_{n2} are input noise sources of the amplifiers which may be calculated by relation 5.11 if shot noise dominates. V_{n3} and V_{n5} are switching noise sources of the capacitors. They are given by relation 4.1.

This circuit has been realized with $C_1 = 5.2$ pF and $C_2 = 1$ pF. Special care has been taken to insure very good accuracy of capacitance ratios

$$\alpha_1 = 0.5000 \quad \alpha_2 = 0.6427 \quad \alpha_3 = 0.05672$$

Results which have been obtained with amplifiers of Fig. 5.1 are summarized in Table 1.

Calculations show that 95% of the noise power is due to shot noise in the amplifiers. This is due to the very small value of capacitance C_a in the amplifiers. Much better results have been recently reported with

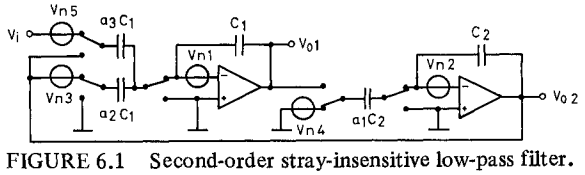


FIGURE 6.1 Second-order stray-insensitive low-pass filter.

TABLE I

	Calculations	Measurements
Clock frequency f_c [Hz]	16384	16384
Resonant frequency f_o [Hz]	1440	1437 (σ = 0.25%)
Quality factor Q	19.2	18.2 (σ = 0.8 %)
Output noise [mV-RMS]	1.6	2
Dynamic range		51 dB
Total power [μw]		7

the improved amplifier shown in Figures 5.11.[12]

7. OTHER SC SOURCES

Other kinds of circuits based on the SC concept are being implemented in micropower. They use the same basic components as the filters.

As an example, Figure 7.1 shows the principle of an integrator suited to handle correctly the DC component of input voltage V_i. It has a reset phase during which offset voltage ΔV is stored in the integrating capacitance C. Subsequent steps of integration are insensitive to ΔV. Integration is altered by any unwanted charge added to input node N.

Switch S_2 must therefore be carefully compensated against clock feedthrough. Furthermore, care must be taken so that no charge can escape from node N by conduction of the junctions associated with S_2.

Switched capacitors can be used for accurate weighting and algebraic addition of several voltages as shown in Figure 7.2. At the end of phase b:

$$V_0 = \sum_{i=1}^{k} \alpha_i (V_i^+ - V_i^-) \qquad (7.1)$$

This result is independent of stray capacitances and of offset voltage.

One application of this circuit is a bandgap voltage reference according to the principle shown in Figure

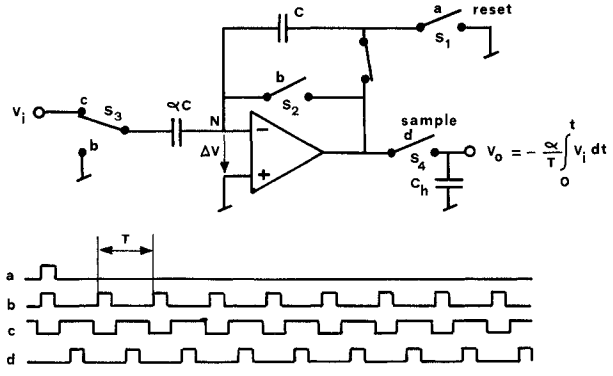


FIGURE 7.1 Accurate integrator.

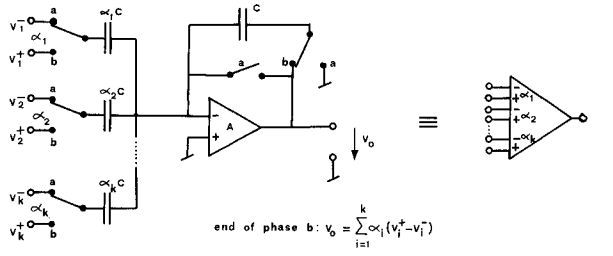


FIGURE 7.2 Weighting and summing circuit.

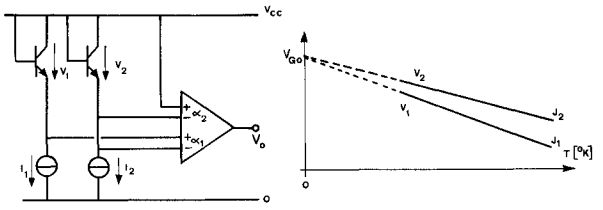


FIGURE 7.3 Principle of a SC bandgap reference

7.3. Voltages V_1 and V_2 are base-emitter voltages of two n^+ diffusion-p-well-n substrate bipolar transistors biased at 2 different current densities J_1 and J_2. Weighting factors α_1 and α_2 are chosen to obtain

$$V_0 = \alpha_2 V_2 + \alpha_1 (V_2 - V_1) \equiv \alpha_2 V_{GO}. \qquad (7.2)$$

Accuracy may be improved by using a single junction biased alternately by currents I_1 and I_2, or a single current source flowing alternately through two transistors with different emitter areas.

The same principle may be applied to implement on-chip calibrated thermal sensors.

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