Millimeter-Wave Diode-Grid Frequency Doubler

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Abstract—**Monolithic diode grids have been fabricated on 2-cm square gallium–arsenide wafers in a proof-of-principle test of a quasi-optical varactor millimeter wave frequency multiplier array concept. An equivalent circuit model based on a transmission-line analysis of plane wave illumination was applied to predict the array performance. The doubler experiments were performed under far-field illumination conditions. This approach facilitates detailed comparison between theory and experiment. A second harmonic conversion efficiency of 9.5 percent and output powers of 0.5 W were achieved at 66 GHz when the diode grid was pumped with a pulsed source at 33 GHz. This grid had 760 Schottky barrier varactor diodes. The average series resistance was 27 Ω, the minimum capacitance was 18 fF at a reverse breakdown voltage of −3 V. The measurements indicate that the diode grid is a feasible device for generating watt-level powers at millimeter frequencies, and that substantial improvement is possible by improving the diode breakdown voltage. The excellent agreement between experiment and the predictions of the theoretical model provide confidence in predictions of achievable CW output power levels of 2.5 W at a frequency of 188 GHz with an edge-cooled grid containing 1000 diodes.**

I. INTRODUCTION

AT MILLIMETER wavelengths, harmonic frequency multipliers are widely used to produce local oscillator power for heterodyne receivers; multipliers with one or two diodes are highly developed. Recently, Archer demonstrated a dual-diode doubler with an output power of 26 mW at 105 GHz [1]. However, many applications in radar and imaging arrays require significantly more power than is available from one or two diodes. We therefore proposed to use a diode grid as a high-power harmonic generator [2]. This approach is attractive because a grid is monolithically integrated with thousands of gallium–arsenide Schottky diodes, thereby resulting in potentially low-cost fabrication and small-size realization. In addition, this approach overcomes the power limitations of a single-diode multiplier because power is distributed among many diodes, making possible watt level CW output power throughout the millimeter wave region. The grid designs for electronic beam-steering and frequency multiplication were described in [2]. Subsequently, a phase shift of 70° at 93 GHz was reported on this grid structure, and the diode-grid model of an inductor in series with a diode was verified experimentally over a frequency range of 33 to 141 GHz [3].

This paper consists of a report of proof-of-principle experiments on the viability of the diode grid for frequency multiplication. An equivalent circuit model based on a transmission-line analysis of plane wave illumination, in conjunction with computer-aided analysis of the nonlinear varactor impedance, was used to predict the doubler circuit performance. The experiments were performed under far-field illumination conditions. This approach facilitates detailed comparison between theory and experiment.

Fig. 1 shows the quasi-optical doubler array design [2] where power at the fundamental frequency enters from the left, through a tuner and filter. The power then arrives at the diode grid, and the nonlinear capacitance of the diodes generates harmonics. The second harmonic leaves on the right, through another filter and tuning network. The filters consist of a wire polarizing grid with a half-wave plate designed for the fundamental. The half-wave plate separates the fundamental from the second harmonic because it rotates the fundamental polarization by 90°, but does not alter the second harmonic polarization. This allows the polarizing grid to select the desired frequency. The tuner is a pair of fused quartz slabs, its configuration similar to the tuner in Archer's quasi-optical waveguide multiplier design [4]. The slabs behave in a similar manner to the familiar double stub tuner in a coaxial line or waveguide. The tuning slabs, filters, and grid were all mounted on micrometers, so they can be easily positioned relative to each other. Earlier work embodying a number of these basic concepts has been discussed by Kraemer *et al.* [5], where up to four packaged varistor diodes were employed in a quasi-optical doubler utilizing an overmoded rectangular waveguide.

The quasi-optical multiplier design has several advantages. It is more rugged than a conventional whisker-contacted varactor in a crossed waveguide. Since no waveguides are necessary, the design and modeling are simpler and the losses due to the waveguide wall are eliminated. However, care must be taken to reduce the losses due to diffraction. The input and output filters act effectively as a

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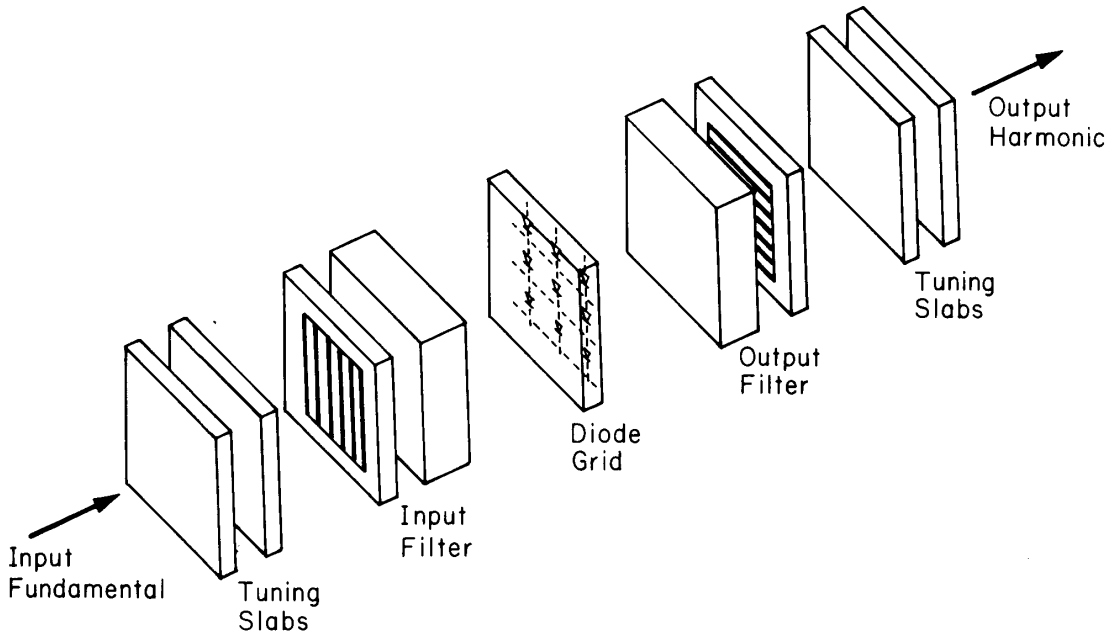

Fig. 1. Proposed millimeter-wave diode-grid frequency doubler array (reference [2]).

mirror for the second harmonic and for the fundamental, respectively. Therefore, tuning is done independently at the input and output, with dual dielectric slabs. The power handling capability increases as the size of the grid increases. Using only edge cooling at the GaAs substrate, calculation indicates that CW output power levels of several watts are possible. An additional attractive feature is that the design can also be easily scaled to higher frequencies.

II. Fabrication

Four grids were fabricated in the course of the proof-of-principle experiments. To determine the fabrication yield, all the diodes on the grid were tested separately with a curve tracer. Diodes that were shorted or with a breakdown voltage of less than -1 V were eliminated with an ultrasonic probe. The diode series resistance, saturation current, and barrier-height were measured with an HP 4145B semiconductor parameter analyzer. Parameters including the zero bias capacitance and the capacitance exponent were measured with an HP 4280A capacitance meter. Since the diode parameters were nonuniform throughout the wafer, 2–3 percent of the diodes in the grid were sampled to determine the average values. Generally, the measured parameters have a standard deviation of 20–40 percent from their average values. The barrier height is about 0.6 ± 0.05 V for these four grids. The other measured diode parameters are shown in Table I, where $f_c = 1/(2\pi R_s C_{\min})$, V_b is the diode breakdown voltage, and γ is the capacitance exponent.

TABLE I
The Average Diode Parameters for the Four Grids

Diode Grid	Yield (%)	R_s (Ω)	C_{min} (fF)	f_c (GHz)	Active Diodes	γ	V_b (V)
#1	90	26±7	32±12	191	1211	0.5±0.1	−3.0±0.1
#2	62	*26±13	18±13	340	760	0.4±0.1	−2.7±0.3
#3	89	76±19	15±6	140	1840	0.4±0.1	−5.0±2.0
#4	93	107±19	14±5	106	1540	0.5±0.1	−2.3±0.8

*Only five diodes were sampled for this measurement.

III. Experimental Arrangement

The doubler experiments were performed under far field illumination conditions, so that the equivalent circuit model based on the transmission-line analysis of plane wave illumination could be applied. The power incident on the grid can be calculated accurately using the familiar antenna gain formulas [6]. In addition, the losses associated with the collimating lens, such as lens spillover and reflections from the lens surface, can be eliminated in the preliminary tests.

In the experimental tests, the doubler circuit was placed at the far field of both the transmitting horn and the receiving horn (Fig. 2.; for simplicity, only the diode grid is shown). The pump source was a 50 kW pulsed magnetron operating at 33 GHz. Here, it should be stressed that although the tests were performed using a pulsed source for convenience, the diode grid is designed for completely CW operation using only edge cooling. The temperature distribution on a grid of 2 by 2 centimeter square (substrate thickness of 250 μm) was calculated. Assuming a perfect heat sink at the four edges of the substrate, the highest temperature rise at the center of the substrate is only about 51°C above room temperature for 8 W of CW power absorbed by the grid. Face cooling would further reduce this number. An appropriate arrangement

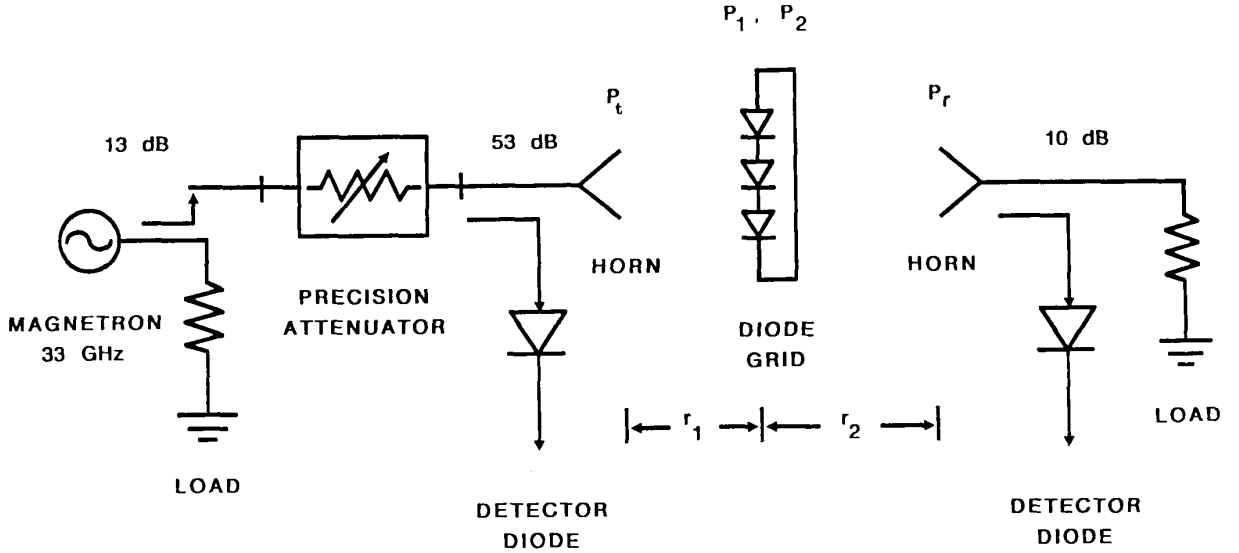

Fig. 2. The arrangement for the diode-grid doubler experiment.

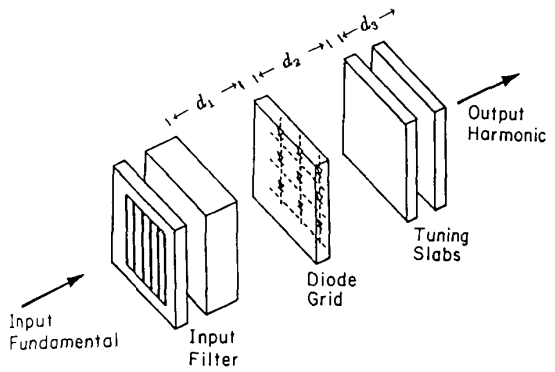

Fig. 3. A simplified version of the doubler circuit.

of directional couplers and attenuators was used to provide the desired power-level incident plane wave pump at the diode grid. A helium–neon laser was used to align the system.

The doubling efficiency of a grid is calculated using the following relation:

$$\eta_2 = \left(\frac{4\pi r_1 r_2}{A_d}\right)^2 \left(\frac{P_r}{P_t G_1 G_2}\right) \tag{1}$$

where P_t is the power transmitted by the source, G_1 is the gain of the source antenna, A_d is the area of the diode grid, r_1 is the distance between the source antenna and the diode grid, P_r is the power measured by the output horn, r_2 is the distance between the diode grid and the output horn, and G_2 is the gain of the output horn. The transmitted and received powers were measured with calibrated detector diodes. The measured gain for the input horn is 19.5 dB, which compares well with the calculated gain [6] of 19.4 dB for $r_1 = 33$ cm. The measured gain for the output horn is 23.0 dB and the calculated gain is 23.1 dB for $r_2 = 25.4$ cm.

In the preliminary tests, in order to simplify the tuning as well as the analysis of the equivalent circuit model, we decided to employ a simplified doubler design (Fig. 3). It consists only of an input filter and two quarter-wave tuning slabs at the fundamental. The input filter passes the fundamental power, but reflects the second harmonic to the output. Because the tuning slabs appear as half-wave plates at the second harmonic, moving the slabs allows one to vary the fundamental impedance without affecting the second harmonic impedance. Although this doubler circuit is not as versatile as the one shown in Fig. 1, it does greatly ease tuning and alignment problems albeit at the cost of a more restricted impedance matching capability.

IV. Characterizing the Doubler Circuit

The doubler equivalent circuit model is based on a transmission-line analysis assuming plane-wave illumination. The substrate, tuners, and filters are represented as sections of transmission line, and their characteristic impedances are equal to the wave impedance in the dielectric. The circuit embedding impedance is calculated as the parallel combination of the impedances looking out to the left and right of the grid.

The diode-grid doubling efficiency and its effective impedance are obtained from the large-signal multiplier analysis program, which was developed by Siegel, Kerr, and Hwang [7]. The optimum grid efficiency is computed by sampling the fundamental and second harmonic embedding impedances for maximum output power. The complex conjugate of these optimum embedding impedances is taken as the diode-grid impedances. In the simulation, the third and fourth harmonic embedding impedances are assumed to be open circuited. We found that with the fundamental and second harmonic embedding impedances at their optimum values, the doubling efficiency could still vary by 48 percent as the third harmonic impedance was

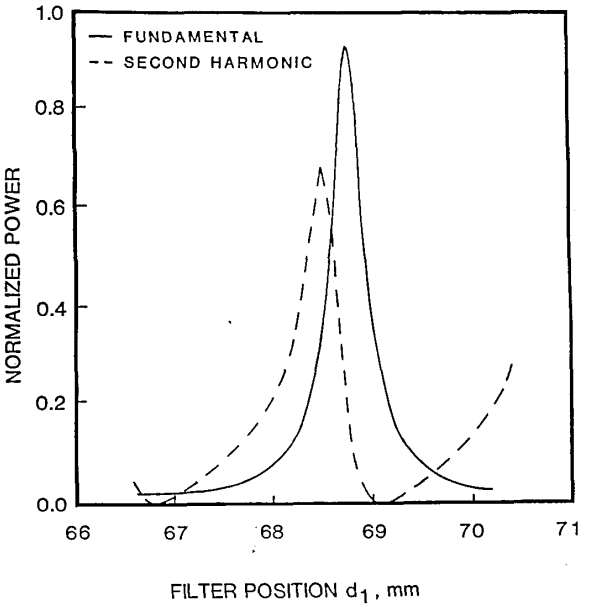

Fig. 4. Calculated power absorbed by grid 3 for the fundamental and second harmonic equivalent circuit as a function of the spacing d_1 (see Fig. 3).

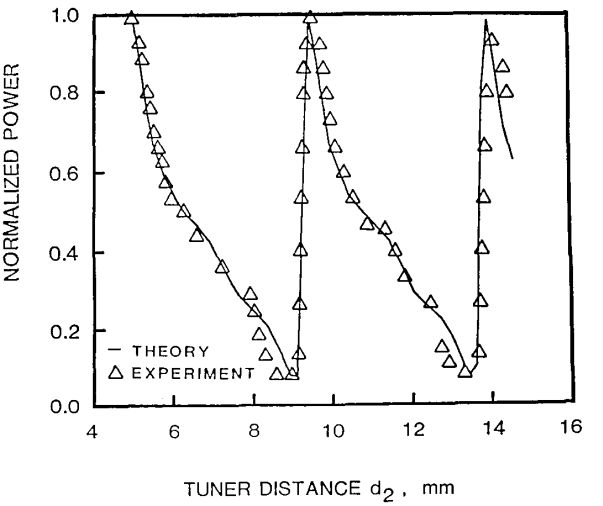

Fig. 5. A comparison of the measured second harmonic output power and the calculated pump power versus slab position d_2 for grid 3. Powers were normalized relative to the maximum.

sampled from short to open circuit. However, with the third harmonic impedance open circuited, the doubling efficiency varied only by less than 3 percent as the fourth harmonic impedance was sampled from short to open circuit. Therefore, the fifth and sixth harmonic impedances can be expected to have even less effect on the doubler performance. In addition, it was found that for f_0/f_c (f_0 is the input frequency) ≥ 0.1, the multiplier program often could not converge if the fifth and sixth harmonic impedances were open circuited or were very large values. Therefore, in the simulations we took a small value for the fifth and sixth harmonics embedding impedances ($10+j10\ \Omega$). The grid inductance is included as part of the diode series reactance. For our grid, the inductance calculated is 277 pH [3], which gives a reactance of 54 Ω at 33 GHz, and 108 Ω at 66 GHz, etc.

Grid 3 was used to verify the equivalent circuit model. Although this grid is not the most efficient one among the four, the area of the wafer (6 cm^2) is the largest, so that diffraction effects should be small. Also, its diode parameters are very well documented. The computed diode efficiency for diode-grid 3 is 9.1 percent for 5 mW per diode input power at a bias level of −0.5 V. The diode-grid impedances are $96-j103\ \Omega$ at the fundamental, and $96+j35\ \Omega$ at the second harmonic frequency. However, the highest doubling efficiency measured using the simplified matching circuit was only about 3 percent. This discrepancy can be explained from the equivalent circuit model. Shown in Fig. 4 is the absorbed pump power and the second harmonic power calculated using the transmission-line equivalent circuit model. These values are plotted as a function of the grid–filter separation d_1 (see Fig. 3). According to the curves, at $d_1 = 68.8$ mm, only 58 percent of the input power is absorbed by the grid, and 61 percent of the second harmonic power is coupled out of the grid. If we multiply the computed 9.1 percent efficiency by the product of these input and output coupling efficiencies, we would obtain about 3.2 percent, which is close to the measured 3 percent value. The equivalent circuit model is constructed using the experimental measured values of d_2 and d_3, which are 5.95 mm and 16.47 mm, respectively. However, d_1 was measured to be 67.1 mm, which departs by about 2.5 percent from the calculated optimum d_1 value, perhaps due to measurement errors.

To verify the accuracy of the effective diode impedance that was computed using the large signal multiplier program [7], the relative input power absorbed by the diode grid as a function of the tuning slab position was measured and compared with the calculation based on the equivalent circuit model. This is done because varying the tuning slab position d_2 or d_3 (see Fig. 3) only changes the fundamental impedance but not the second harmonic impedance (the slabs correspond to a quarter wavelength at the fundamental, but a half wavelength at the second harmonic). Therefore, measuring the relative second harmonic power generated by the grid is equivalent to measuring the relative input power absorbed by the grid. Fig. 5 shows the measured second harmonic power as a function of the tuning slab spacing d_2 for grid 3, where d_1 was measured to be 74.8 mm, and d_3 was 11.5 mm. The power is normalized to the maximum power measured. The theoretical line represents the calculation of the absorbed pump power by the grid based on the equivalent circuit model; it compares reasonably well with the normalized measured results.

The filter–grid separation d_1 and the tuner separation distances d_2 and d_3 (see Fig. 3) were measured during the

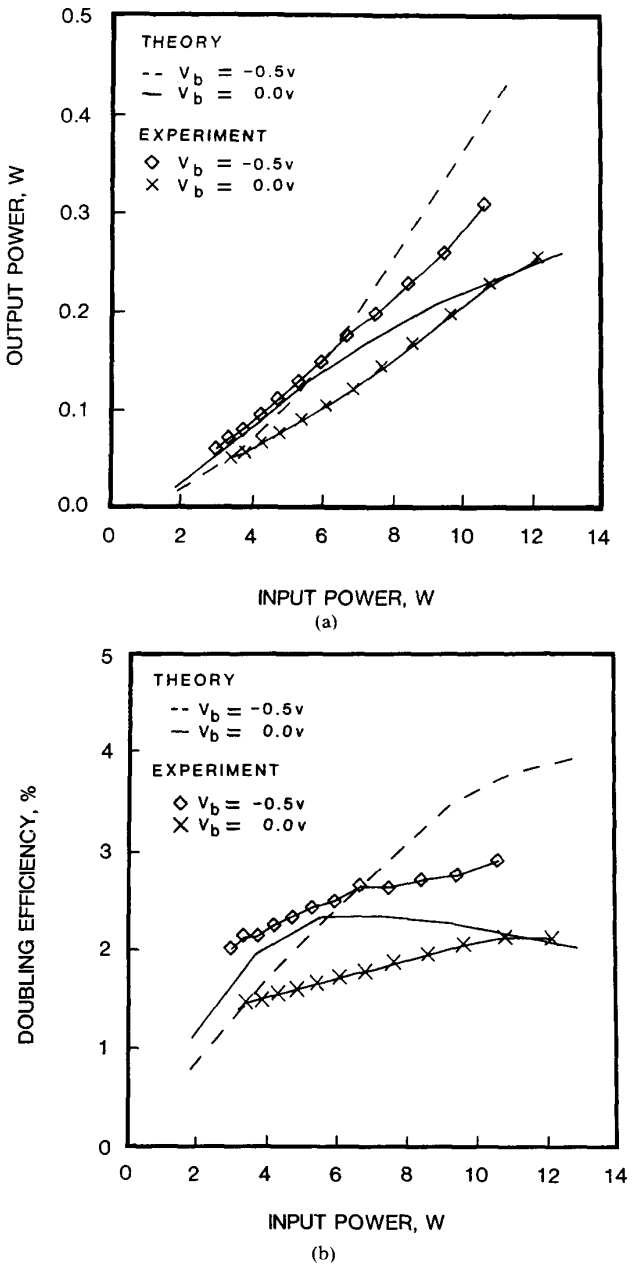

Fig. 6. A comparison between the measured output power of grid 3 and the simulated output power based on the multiplier program. (a) Output power as a function of input power. (b) Doubling efficiency as a function of input power.

experiment so that the grid embedding impedances at the fundamental and up to the fourth harmonic frequencies could be calculated based on the equivalent circuit model. These values were subsequently employed in the multiplier program [7], and the corresponding doubling efficiency computed was compared with the measured results. In the simulations, the output power of the grid is found by multiplying the computed output power of a single diode by the number of diodes on the grid. The doubling efficiency of the grid is calculated by dividing the output power by the input power available to the diodes. Fig. 6(a) shows the measured and computed second harmonic output power as a function of the input power for grid 3. The computed second harmonic power compares reasonably well with the measured results at bias levels of -0.5 V and 0 V. This implies that the embedding impedances calculated by the transmission line model are quite accurate. Fig. 6(b) shows the corresponding doubling efficiency as a function of the input power.

V. Power Measurements

After verifying the equivalent circuit model using the simplified circuit, we proceeded to test the original doubler circuit (see Fig. 1). In this configuration, filters and tuning slabs are available for both the input and output frequencies, so that the circuit has a wider impedance tuning range. Although grids 1 and 2 were more efficient, their diode breakdown voltages were quite low, -3 V. Unfortunately, they consequently burned-out during these tests, since more than 7 mW was inadvertently pumped into each diode. Therefore, the only doubling efficiency results we obtained from the complete circuit configuration were using grid 3, where the diodes have a -5 V breakdown voltage. Since the series resistance of the diodes is quite high, 76 Ω, the doubling efficiency is not predicted to be as high as for grids 1 and 2. Fig. 7(a) compares the measured output power from these two doubler circuits for grid 3 at a bias level of 0 V. It is seen that with the output filter and tuners added into the system, the diode grid indeed generates 40 percent more output power than with the simplified circuit. In addition, it agrees better with the optimized results computed by the multiplier program, where the fundamental and second harmonic embedding impedances are the sampled optimum values. The corresponding doubling efficiency results are shown in Fig. 7(b).

The highest doubling efficiency results were obtained from grid 2, since its cutoff frequency is the highest among the four grids ($f_c = 340$ GHz). Fig. 8(a) shows the measured 66 GHz output power for grid 2 with the simplified circuit (see Fig. 3) under three different bias conditions. The highest output power was 0.5 W at a bias voltage of -0.5 V. Fig. 8(b) shows the corresponding doubling efficiency as a function of the input power. The highest efficiency measured was 9.5 percent with 2.5 W input power. A small strip section of this grid was completely open circuited due to a wafer defect, so that only 86 percent of the grid area contained active diodes. Nevertheless, we used the entire grid area in performing the efficiency and output power calculations. This provides a conservative estimation and eliminates questions of the distribution of power to the remaining active diodes which are mounted in an antenna structure. This diode grid was also used in the phase-shift measurement at 93 GHz [3], so there was a quarter wave-matching layer of 434 μm fused quartz plated behind it.

Table II shows the highest second harmonic power and doubling efficiency measured using the simplified circuit

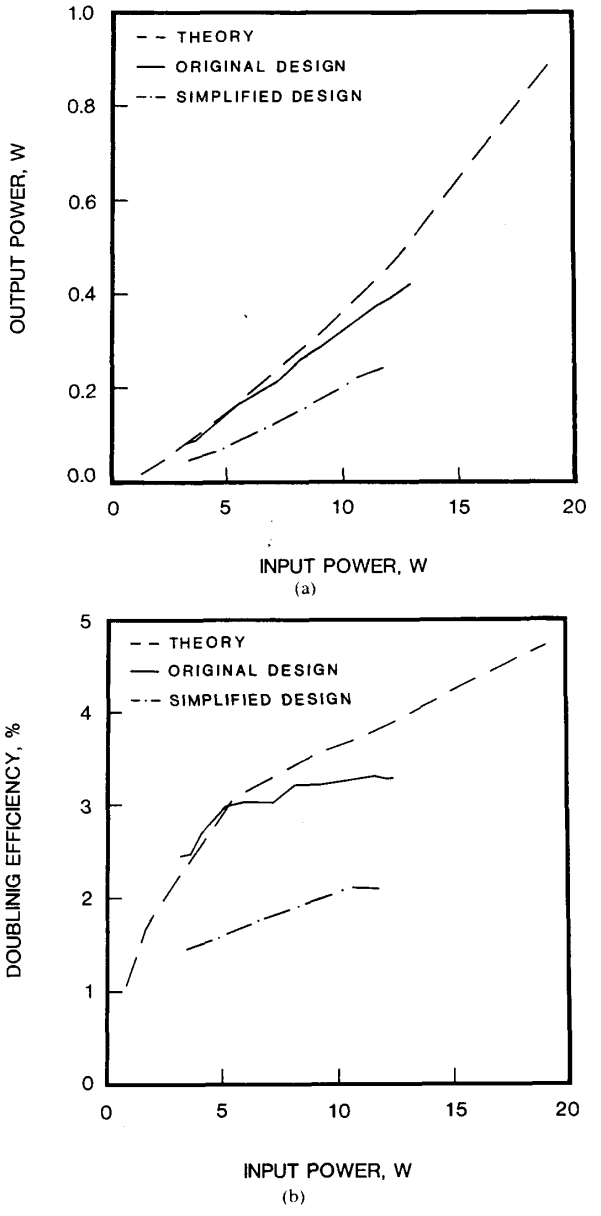

Fig. 7. A comparison of the measured output power of grid 3 using the two doubler circuit designs (see Figs. 1 and 3) and the simulated optimum results. (a) Output power as a function of the input power at zero bias. (b) Corresponding efficiency as a function of the input power.

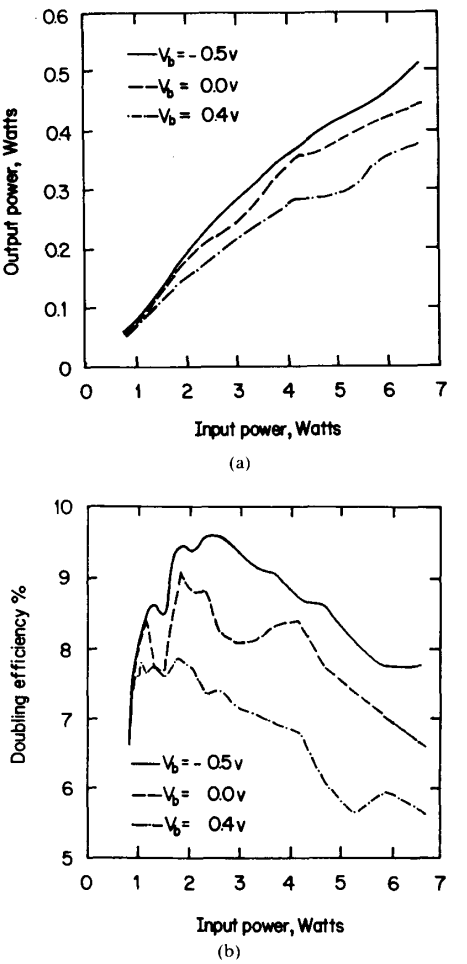

Fig. 8. (a) Measured output power at 66 GHz as a function of the input power at 33 GHz for grid 2. (b) Measured doubling efficiency as a function of the input power.

TABLE II
THE MEASURED DOUBLING EFFICIENCY AND POWER

Diode Grid	P_2 (W)	η_2 (%)
#1	0.32	5.8
#2	0.50	9.5
#3	0.32	3.0
#4	0.10	1.5

for these four grids. Fig. 9 compares these measured highest doubling efficiency results with the theoretical predictions for an abrupt junction varactor doubler provided by Penfield and Rafuse [8]. This is a reasonable comparison, since although our diode was designed to have a hyper-abrupt-junction doping profile of $\gamma = 0.8$, the measured doping profile was closer to an abrupt-junction diode with $\gamma \simeq 0.5$. The measured doubling efficiencies of the grids are significantly lower than the optimum predicted values, because the input and output coupling efficiency calculated by the equivalent circuit model shows that the simplified circuit cannot provide the optimum embedding circuit for the grid (see Fig. 4). To provide support for this contention, we can correct the experimental data for the nonoptimum coupling geometry. Specifically, if we divide

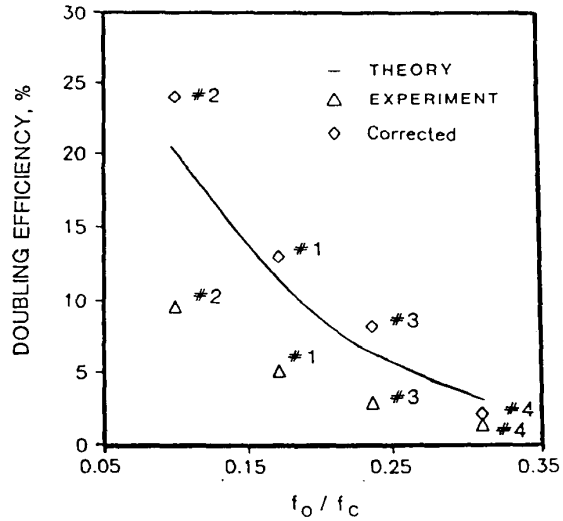

Fig. 9. A comparison of the measured and corrected (for coupling losses) doubling efficiency with the Penfield and Rafuse theoretical prediction.

the measured grid doubling efficiency by the product of these input and output coupling efficiencies, the resulting corrected values for each grid (also shown in Fig. 9) are comparable to the optimum values predicted by Penfield and Rafuse [8]. Therefore, we conclude that the measured grid efficiencies are lower than the predicted optimum results because the simplified circuit cannot provide the optimum embedding impedances, and with a better matching circuit such as the complete circuit configuration shown in Fig. 1, grids 1 and 2 should have produced doubling efficiencies close to 12 and 20 percent, respectively.

VI. Conclusions

The grids fabricated in these proof-of-principle experiments are limited in their harmonic output power by the diode breakdown voltage and in their losses by the series resistance. However, the agreement between the calculated and measured results indicate that our transmission-line model is sufficiently accurate to predict the performance of a frequency-multiplier array. It is therefore appropriate to extrapolate the multiplier results to account for current monolithic diode fabrication technology. Researchers have reported monolithic diodes with a series resistance as low as 5 Ω and a breakdown voltage of 10 V [9], [10], so that it appears that a watt-level millimeter doubler array is definitely feasible. Fig. 10 shows the computed doubling efficiency and the second harmonic power as a function of the input power for a grid containing 1000 Schottky barrier diodes. The input frequencies are 33, 65, and 94 GHz. The simulations assumed that the diode breakdown voltage is -5 V, and the diode is biased at -1 V. The diode series resistance is 20 Ω, and the zero bias capacitance is 25 fF ($f_c = 1.4$ THz, for $\gamma = 0.8$) [2]. The embedding impedances were optimized with respect to the maximum input power. These simulations predict that it is possible to generate 2.5 W at an output frequency of 188 GHz with

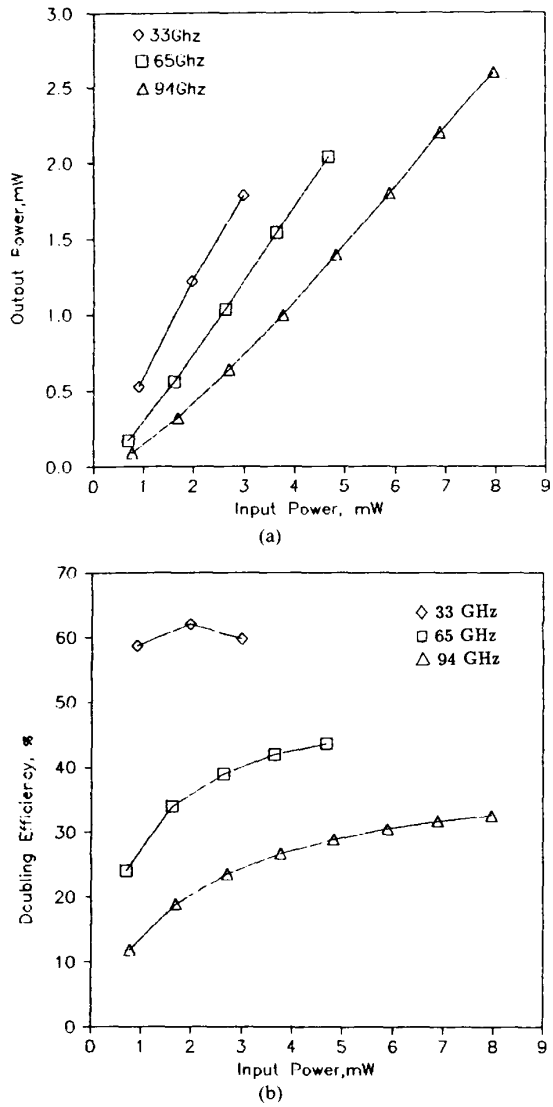

Fig. 10. Projected doubler performance at input frequencies of 33, 65, and 94 GHz. (a) Second harmonic power as a function of the input power at -1 V bias. (b) The doubling efficiency as a function of the input power.

30 percent doubling efficiency, 2 W of power at a 130 GHz output frequency with 43 percent doubling efficiency, or 1.7 W of power with 60 percent doubling efficiency at 66 GHz. The grid power-handling capability is limited by the diode breakdown voltage and is proportional to the input frequency [8]. Although the tests were performed using a pulsed source for convenience, the diode grid is designed for a completely CW operation using only edge cooling. The calculations show that several watts of CW operation should be possible.

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