Minimization of the Capacitor Voltage Fluctuations of a Modular Multilevel Converter by Circulating Current Control

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***Abstract*— The modular multilevel converter (MMC) is one of the most potential converter topologies for medium/high power/voltage applications. One of the main technical challenges of an MMC is to eliminate/minimize the circulating currents within the legs. Circulating currents, if not properly controlled, increase the amplitude of capacitor voltage variations, rating values of the converter components and converter losses. This paper proposes a closed-loop circulating current control strategy for an MMC to specifically minimize the amplitude of capacitor voltage variations. The proposed strategy is based on adding an offset signal to the modulating signal of each arm. To minimize the amplitude of the capacitor voltage oscillations, an optimal circulating current component is determined and used as a reference signal for the current control of each MMC leg. Performance of the proposed control strategy is evaluated based on simulation studies in the MATLAB/Simulink environment. The reported study results demonstrate effectiveness of the proposed strategy to reduce the amplitude of the capacitor voltage oscillations.**

I. Introduction

Multilevel converters have attracted significant interests for medium/high power applications. Among various multilevel converter topologies [1], [2], the modular multilevel converter (MMC) [3] [4], offers several salient features which make it a potential candidate for various applications including high-voltage direct current (HVDC) transmission systems [5], [6], flexible alternating current transmission system (FACTS) controllers [7], and motor drives [8].

The most attractive features of an MMC are (i) its modularity and scalability to different power and voltage levels, and (ii) its capacitor voltage balancing task which is relatively simple [9], [10].

Proper operation of an MMC necessitates an active voltage balancing scheme to carry out the voltage balancing task among the capacitors of each phase. Capacitor voltage balancing of an MMC does not have the limitations and complexities associated with other multilevel converters [6]. However, it is mutually coupled with the circulating currents within each leg of the MMC, which if not properly controlled, can have adverse impacts on semiconductor ratings, losses, and also the magnitude of the capacitor voltage fluctuations.

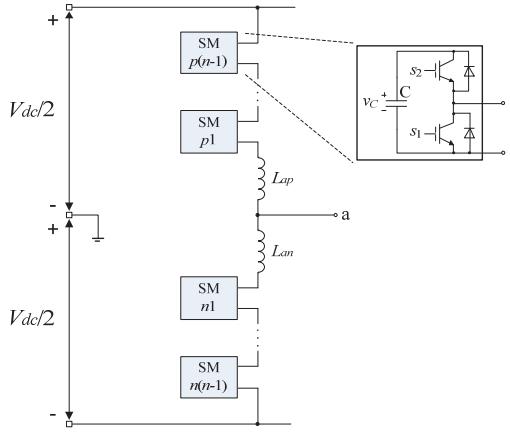

Fig. 1. Circuit diagram of one leg of an *n*-level MMC leg.

Analysis of the circulating currents of an MMC has been reported in the technical literature and, correspondingly, various open-loop and closed-loop remedial measures have been proposed to minimize/eliminate them [11]-[13]. The open-loop strategies rely on the exact parameters of the MMC which are not realistic under the practical conditions [12]. In [13], a closed-loop control strategy based on elimination of the second order harmonic of the arm currents has been proposed. However, the proposed strategy reduces the amplitude of the capacitor voltage fluctuations only under specific operating

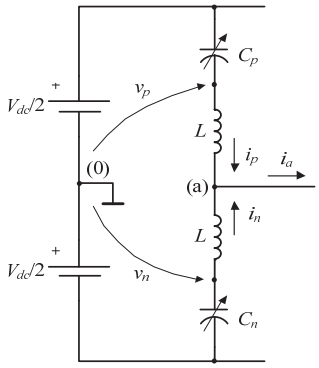

Fig. 2. Equivalent circuit of the MMC of Fig. 1 with an infinite number of SMs.

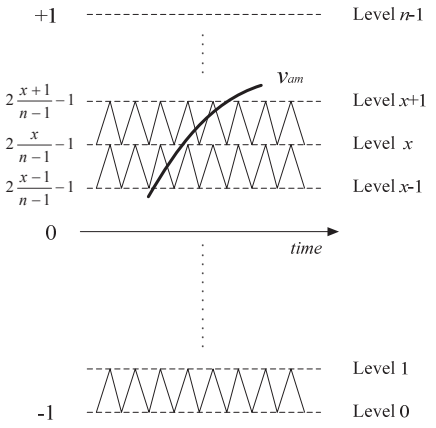

Fig. 3. The modulating and carrier waveforms of a PD-SPWM strategy.

conditions.

In this paper, a new closed-loop control strategy for the circulating currents of an MMC is presented. Based on the mathematical model of an MMC developed in [14], a circulating current control strategy is proposed. The proposed strategy is realized by adding an offset signal into the modulating signal of each arm. To minimize the amplitude of the capacitor voltage oscillations, an optimal circulating current component is determined and used as a reference signal for the current control of MMC legs. The effectiveness of the proposed strategy in terms of reducing the amplitude of the capacitor voltage oscillations for a five-level MMC is presented. The studies are carried out based on simulations in the MATLAB/Simulink environment for various operating conditions. The analysis and conclusions of this paper are general and applicable to an *n*-level MMC.

The rest of this paper is organized as follows. Section II, briefly presents the developed mathematical model of an MMC in [13]. Section III discusses the SPWM and capacitor voltage balancing strategies. Section IV proposes the new current control strategy. Section V reports the simulation results, and Section VI concludes this paper.

II. Mathematical Model of an MMC

Fig. 1 depicts a circuit diagram of one leg of an MMC. The MMC consists of two arms per phase where each arm comprises *n*-1 series-connected, identical, SubModules (SMs) and a series arm inductor *L*. Each SM consists of a half-bridge circuit and a capacitor. The output voltage of each half-bridge circuit is either equal to its capacitor voltage, when the SM is switched on, or zero, when the SM is switched off. The arm inductors are to limit the circulating current within each leg and also the fault currents.

The equivalent circuit of the MMC of Fig. 1 with an infinite number of SMs, i.e. $n\to\infty$ is shown in Fig. 2. In [14], a mathematical model for an MMC with an infinite number of SMs is developed. A SPWM switching strategy and a sinusoidal output current waveform are assumed,

$$v_{am} = m_a \cos(\omega t), \tag{1}$$

$$i_a = \hat{I}_a \cos(\omega t + \varphi), \tag{2}$$

where v_{am} and m_a represent the MMC modulating signal and modulation index, respectively. Based on the results from [14], and assuming no inductor and parasitic resistor in the MMC arms, the arm currents are expressed by

$$i_p = \frac{\hat{I}_a}{2}\cos(\omega t+\varphi)+\frac{m_a\hat{I}_a}{4}\cos(\varphi)+\frac{m_a\hat{I}_a}{4}\cos(2\omega t+\varphi), \tag{3}$$

$$i_n = \frac{\hat{I}_a}{2}\cos(\omega t+\varphi)-\frac{m_a\hat{I}_a}{4}\cos(\varphi)-\frac{m_a\hat{I}_a}{4}\cos(2\omega t+\varphi). \tag{4}$$

Based on (3) and (4), the arm currents consist of three components: (i) a fundamental component which is half of the output current; (ii) a dc component associated with the active power exchange; and (iii) a second order harmonic component which transfers energy between the SMs.

In [14], a mathematical model is developed to determine the average values of the arm currents of an MMC with a finite number of SMs. The developed model is based on two assumptions: (i) the arm inductors are included to limit the arm currents, and (ii) a capacitor voltage balancing strategy is embedded in the SPWM strategy. The corresponding developed equations to determine the average values of the arm currents are [14]:

$$\bar{i}_p = \frac{\bar{i}_a}{2}+\frac{1}{2L}\int_0^t\left(\bar{v}_p-\bar{v}_n\right)dt + I_{pn0}, \tag{5}$$

$$\bar{i}_n = \frac{\bar{i}_a}{2}-\frac{1}{2L}\int_0^t\left(\bar{v}_p-\bar{v}_n\right)dt - I_{pn0}, \tag{6}$$

where v_p and v_n , as shown in the equivalent circuit of Fig. 2, represent the voltages generated by the SMs in the upper and

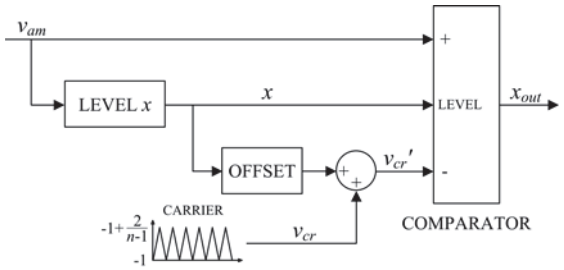

Fig. 4. Block diagram of the PD-SPWM modulator.

lower arms with respect to the dc-side mid-point, respectively. The variables with a bar line in (5) and (6) denote the locally-averaged values of the corresponding variables over one switching period. I_{pn0} represents

$$I_{pn0} = \frac{I_{p0} - I_{n0}}{2}, \tag{7}$$

where I_{p0} and I_{n0} denote the initial values of the upper and lower arm currents, respectively.

Adopting a proper capacitor voltage balancing strategy, the capacitor voltages of the upper arm SMs are kept ideally equal. Similarly, the capacitor voltages of the lower arm SMs are also kept equal. It is shown in [14] that, by using a SPWM-based capacitor voltage balancing strategy, the average values of the SM capacitor voltages of the upper and lower arms can be expressed by:

$$\bar{v}_{Cp} = \frac{1}{C}\int_0^t \bar{i}_p \frac{1 - v_{am}}{2} dt + V_{Cp0}, \tag{8}$$

$$\bar{v}_{Cn} = \frac{1}{C}\int_0^t (-\bar{i}_n) \frac{1 + v_{am}}{2} dt + V_{Cn0}. \tag{9}$$

III. SPWM and Capacitor Voltage Balancing Strategies

A. SPWM Strategy

To synthesize an n-level waveform at the ac-side of the MMC, a phase disposition (PD)-SPWM strategy is applied. The PD technique requires n-1 in-phase carrier waveforms displaced symmetrically with respect to the zero-axis, as illustrated in Fig. 3 [6]. The modulating signal is compared with the n-1 carrier waveforms to determine the required voltage level at the ac-side of the MMC.

To implement the PD-SPWM strategy of Fig. 3, a carrier waveform v_{cr} with a constant amplitude in the range of [-1,-1+A_{cr}] is generated. A_{cr} is

$$A_{cr} = \frac{2}{n-1}. \tag{10}$$

To generate all of the n-1 carriers, offset signals will be added to v_{cr}. Based on the instantaneous value of the modulating signal, the voltage level x is determined by

$$x = int\left(\frac{v_{am} + 1}{2/(n-1)}\right), \tag{11}$$

where *int*() is a lower rounded integer function. The resultant level shifted carrier signal is expressed by

$$v_{cr}' = v_{cr} + x\frac{2}{n-1}. \tag{12}$$

The modulating signal is compared with the new generated level shifted carrier in a classical way to generate the PD-SPWM voltage level, i.e., when the modulating signal is lower than the corresponding carrier waveform, the output level is x, otherwise the output level is x+1, as expressed by

$$x_{out} = \begin{cases} x & v_{am} < v_{cr}' \\ x+1 & v_{am} \geq v_{cr}' \end{cases} \tag{13}$$

Fig. 4 shows the block diagram of the PD-SPWM strategy.

B. Capacitor Voltage Balancing

Capacitor voltage balancing is achieved based on the SM capacitor voltages and also the direction of the arm currents. To carry out the capacitor voltage balancing task of the SMs of each arm, during each PD-PWM period, the SM capacitor voltages of each arm are measured and sorted in descending order. If the upper (lower) arm current is positive, out the n-1 SMs of the upper (lower) arm, the required number of the SMs with the lowest (highest) voltages are identified and switched on. The details of the adopted capacitor voltage balancing strategy are explained in [6] and are not repeated here.

IV. Leg Current Control

As shown in Section II, based on the simplified model of an MMC, the arm currents include three components which are expressed by (3) and (4). In practice, circulating currents through the arms include other even order harmonic components as well [13]. To improve the internal dynamic/performance of an MMC, the circulating current components need to be controlled. This section proposes a circulation current control strategy which aims at reducing the amplitude of the capacitor voltage fluctuations.

A. Mathematical Formulation of the Control System

As shown in Fig. 2, the circuit diagram of an MMC includes a series arm inductor. The voltages generated by the SMs in the upper and lower arm with respect to the dc-side mid-point are

$$v_p = \frac{V_{dc}}{2} - v_{SMp} \quad \text{and} \tag{14}$$

$$v_n = -\frac{V_{dc}}{2} + v_{SMn}, \tag{15}$$

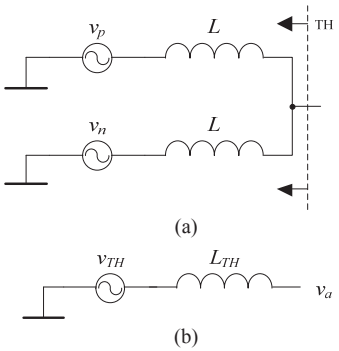

Fig. 5. (a) Simplified equivalent circuit of one leg of the MMC, and (b) its ac-side Thévenin equivalent circuit.

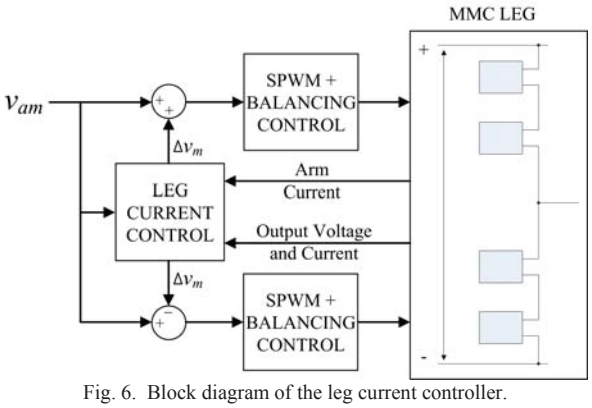

Fig. 6. Block diagram of the leg current controller.

where v_{SMp} and v_{SMn} represent the total voltages generated by the switched-on SMs in the upper and lower arms, respectively.

Based on the Thévenin's Theorem, the ac-side equivalent circuit of one leg of the MMC is shown in Fig. 5 where,

$$v_{th} = \frac{v_p + v_n}{2}, \tag{16}$$

$$L_{th} = \frac{L}{2}. \tag{17}$$

Assuming a voltage offset signal Δv, equation (16) can be re-written as

$$v_{th} = \frac{(v_p + \Delta v) + (v_n - \Delta v)}{2}. \tag{18}$$

Equation (18) shows that modifying the generated voltages of the upper and lower arms by $v_p+\Delta v$ and v_n-Δv, respectively, does not impact the MMC ac-side leg voltage v_{th}. This modification is used as a basis to develop a current control strategy based on the block diagram of Fig. 6.

Since the arm voltages v_p and v_n are generated based on the modulating signal v_{am}, v_{am} is modified by an offset control signal Δv_m as

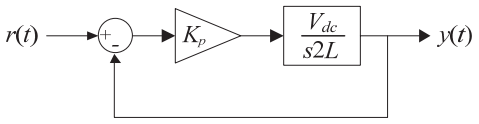

Fig. 7. Block diagram of the current control loop.

$$v_p = \frac{V_{dc}}{2}\left(v_{am} + \Delta v_m\right), \tag{19}$$

$$v_n = \frac{V_{dc}}{2}\left(v_{am} - \Delta v_m\right). \tag{20}$$

Equations (19) and (20) show that the generated voltages in the upper (lower) arm of the MMC can be modified by adding (subtracting) an offset signal Δv_m to (from) the modulating waveform. In the next section, the transfer function between the leg current and the offset voltage is determined and used to control the circulating current of the MMC leg.

B. Determination of the Transfer Function and Controller Design

To design a circulating current controller, the first step is to determine the transfer function of the system. Hereinafter, the design procedure is explained for the upper arm current controller. Because of symmetry, the lower arm current is indirectly controlled by the control variable determined for as the upper arm (Δv_m).

The input, $u(t)$, and the output, $y(t)$, are defined as

$$y(t) = i_p - \frac{i_a}{2} = i_{HARM} + i_{dc}, \tag{21}$$

$$u(t) = \Delta v_m, \tag{22}$$

where $y(t)$ comprises all of the upper arm components except the fundamental one. Replacing for i_p from (5) into (21) and considering (19) and (20), (21) is re-written as

$$y(t) = \frac{1}{2L}\int\left(v_p - v_n\right)dt = \frac{V_{dc}}{4L}\int\left(v_{am} + u(t) - v_{am} + u(t)\right)dt. \tag{23}$$

Re-writing (23) in the Laplace domain, we obtain

$$y(s) = \frac{V_{dc}}{s2L}u(s). \tag{24}$$

From (24), the system open-loop transfer function is yielded as

$$G_p(s) = \frac{y(s)}{u(s)} = \frac{V_{dc}}{s2L}. \tag{25}$$

The system transfer function has only one pole at zero. Using a proportional controller with a gain of K_p, the system closed-loop transfer function is expressed by

$$\frac{y(s)}{r(s)} = \frac{1/s\tau}{1 + 1/s\tau}, \tag{26}$$

where the time constant τ is

$$\tau = \frac{2L}{V_{dc} K_p}. \tag{27}$$

By adjusting K_p, the arm current can track its reference value with a negligible error. The block diagram of the current control loop is shown in Fig. 7.

C. Arm Current Reference

Based on (21), $y(t)$ does not contain the fundamental component of the arm current. Therefore, a reference signal $r(t)$ for the current control strategy is generated as

$$r(t) = i_{dc}^{*} + i_{HARM}^{*}. \tag{28}$$

The dc component of the reference current $r(t)$, i.e., i_{dc}^{*} is determined based on the steady state value of i_{dc}. Assuming a lossless converter and based on the power balance equation, the following equations are deduced

$$p_{ac} = \frac{1}{T/2} \int_{t-T/2}^{t} v_a i_a \, dt, \quad p_{dc} = V_{dc} i_{dc} \quad \text{and} \tag{29}$$

$$p_{ac} = p_{dc}. \tag{30}$$

Consequently, an estimated value for i_{dc} is determined by

$$i_{dc} = \frac{p_{ac}(t)}{V_{dc}}. \tag{31}$$

However, in order to regulate the sum of the SM capacitor voltages to the desired value, converter power losses have to be considered. This is achieved by including a PI controller whose output is added to the estimated dc current given by (31). Then, the final dc current reference i_{dc}^{*} is obtained. This procedure is shown in the block diagram of Fig. 8.

The ac component of the reference current $r(t)$, i.e., i_{HARM}^{*} which comprises the even order harmonics, can be determined based on a set of criteria. In this paper, the criterion is to reduce the amplitude of the capacitor voltage oscillations. Therefore, i_{HARM}^{*} can be formulated in a general form as

$$i_{HARM}^{*}(t,\varphi) = \frac{m_a \hat{I}_a}{4} K_h(\varphi) \cos\left(h\omega t + \varphi_h(\varphi)\right). \tag{32}$$

Equation (32) depends on the output current phase angle φ, which can be calculated based on real and apparent power by

$$\varphi = \cos^{-1}\left(\frac{P}{S}\right) \quad \text{and} \tag{33}$$

$$S(t) = \frac{\hat{V}_a \hat{I}_a}{2}. \tag{34}$$

The procedure to determine the harmonic components of the reference current is shown in the block diagram of Fig. 8.

D. Optimal Current

Since the objective of circulating current control in the MMC arm is to reduce the amplitude of capacitor voltage variations, the most significant circulating current components which

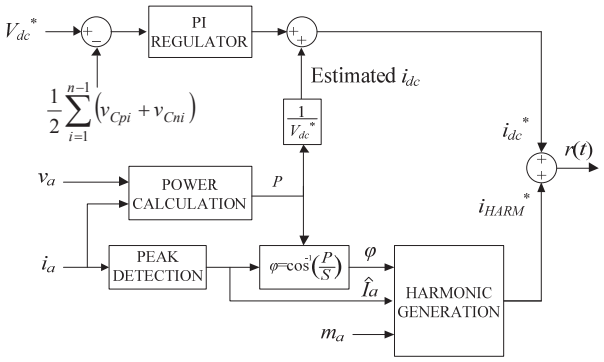

Fig. 8. Block diagram of the arm current reference generator.

contribute to the capacitor voltage oscillations need to be identified.

Based on (8), variation of a capacitor voltage over a one period, $\Delta\bar{v}_{Cp}$ is

$$\Delta\bar{v}_{Cp} = \frac{1}{C}\int_{0}^{T} \bar{i}_p \frac{1-v_{am}}{2} \, dt. \tag{35}$$

To reduce the capacitor voltage variations, an objective function f_{opt} is defined as

$$f_{opt} = \int_{0}^{T} \left(\bar{i}_p \frac{1-v_{am}}{2} \right)^2 dt. \tag{36}$$

Equation (36) does not represent the amplitude of the capacitor voltage variations. However, if the quadratic function $\Delta\bar{v}_{Cp}$ is minimized, as a consequence its amplitude is minimized as well.

Since the harmonic components of the arm currents include even order harmonics, various harmonic components can be included and evaluated. In this paper, only the second order harmonic is considered as it is the most dominant/significant component which contributes to the capacitor voltage fluctuations. Considering the second order harmonic component in the arm current and substituting for the arm current in (36), we deduce

$$f_{opt}(K_2,\varphi_2) = \int_{0}^{T} \left(\left(\frac{\hat{I}_a}{2}\cos(\omega t+\varphi) + \frac{\hat{I}_a \cdot m_a}{4}\cos(\varphi) + \right.\right.$$
$$\left.\left. + K_2(m_a,\varphi)\frac{\hat{I}_a m_a}{4}\cos(\omega t+\varphi_2(m_a,\varphi)) \right) \frac{1-m_a\cos(\omega t)}{2} \right)^2 dt \tag{37}$$

By minimizing the objective function in (37), i.e.,

$$\nabla f_{opt}(K_2,\varphi_2) = 0, \tag{38}$$

the optimal values for the phase angle and the amplitude of the second order harmonic of the arm current are determined.

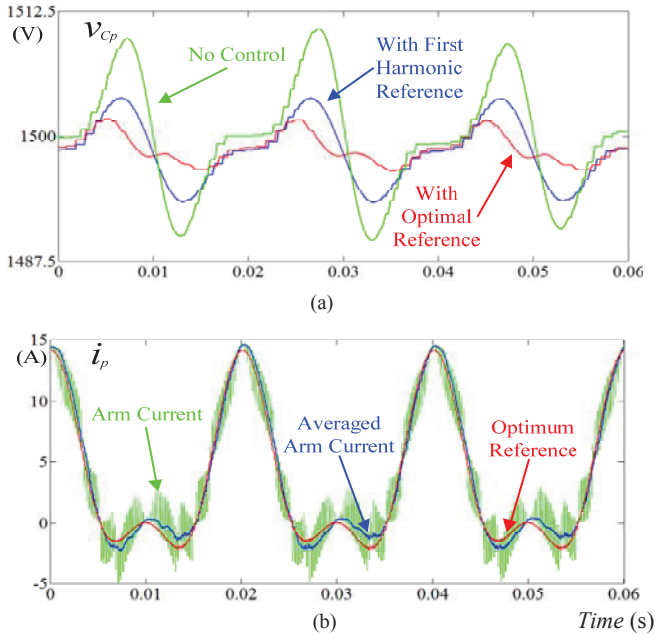

Fig. 9. Converter waveforms: (a) capacitor voltages, and (b) upper arm current.

V. Simulation Results

Performance of a five-level (n=5) MMC that operates based on the proposed current control strategy is evaluated based on simulation studies conducted in the MATLAB/Simulink environment. The dc-side of the MMC is supplied by a constant dc source of V_{dc}=6 kV and the ac-side current is provided by a single-phase current source. The SM capacitors and the arm inductors are C=1.36 mF and L=6 mH. The switching frequency and the fundamental frequency are f_{sw}= 4 kHz and f=50 Hz.

Fig. 9 shows the converter waveforms at an ac-side operating point corresponding to power factor 1 and m_a=1 under three scenarios: (i) without any leg current control, (ii) with a leg current control based on a fundamental component reference current, and (iii) with a current control based on an optimal second harmonic component as a reference current. Fig. 9(a) shows the amplitude of the capacitor voltage oscillations and highlights the capability of the proposed current controller to reduce the voltage variations of the SM capacitor. Fig. 9(b) shows the converter upper arm current. The proposed current controller adjusts the magnitude and the phase angle of the second order harmonic to reduce/minimize the capacitor voltage variations.

Fig. 10 compares the effectiveness of the proposed arm current control strategy in reducing the amplitudes of the capacitor voltage oscillations for various operating conditions, i.e., modulation index and ac-side power factor. The capacitor voltages of all of the graphs in Fig. 10 are normalized with respect to:

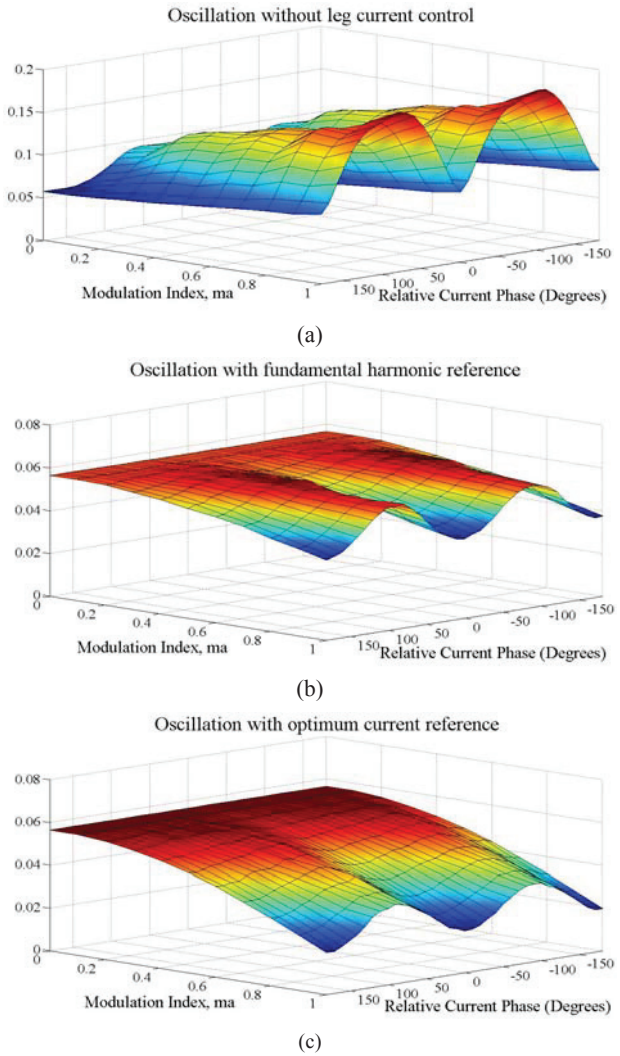

Fig. 10. Normalized amplitude of the capacitor voltage oscillations for various operating conditions, i.e., modulation index and output current phase angle: (a) without any leg current control, (b) with a leg current control based on a fundamental component reference current, and (c) with a current control based on an optimal second harmonic component as a reference current.

$$\frac{\Delta V_{C\,norm}}{2} = \frac{\Delta V_C / 2}{I_{a\,rms} / f\,C} \,. \tag{39}$$

Figs. 10(a), (b), and (c) shows the normalized amplitudes of the capacitor voltages under three operating scenarios, respectively: (i) without any arm current control strategy, (ii) when the fundamental component of the arm current is controlled, i.e., the reference current of arm current controller has only a fundamental component, and (iii) when the fundamental and second harmonic components of the arm current are controlled, i.e., the reference current of arm current controller is generated based on the optimized values of the magnitude and phase angles. Fig. 10 highlights the capability of the proposed current controller to reduce the amplitudes of

the capacitor voltage variations under all operating conditions, and not just for specific cases.

VI. Conclusion

This paper proposes a circulating current control strategy to reduce the amplitude of the capacitor voltage fluctuations of an MMC. The strategy is based on modification of the modulation waveforms of an MMC by adding an offset signal to the modulating signal of each arm. To minimize the amplitude of the capacitor voltage oscillations, an optimal circulating current component is determined and used as a reference signal for the current control of each MMC leg. Effectiveness of the proposed current control strategy for a five-level MMC under various operating conditions, based on simulation studies in the MATLAB/Simulink environment is evaluated. Simulation results conclude that the proposed current control strategy is able to reduce the amplitude of the capacitor voltages under all operating conditions. This salient feature is of significance for sizing the SM capacitors which leads to the smaller footprint and reduced cost of an MMC-based system.

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References

[1] L.G. Franquelo, J. Rodríguez, J.I. León, S. Kouro, P. Portillo, and M.A.M. Prats, "The age of Multilevel converters arrives", *IEEE Ind. Electron. Magazine*, vol. 2, no. 2, pp. 28.39, June 2008.

[2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L.G. Franquelo, B. Wu, J. Rodríguez, M.A. Pérez, and J.I. León, "Recent advances and industrial applications of multilevel converters", *IEEE Tran. Ind. Electron.*, vol.57, no. 8, pp. 2553-2580, Aug. 2010.

[3] A. Lesnicar and R. Marquardt, "A new modular voltage source inverter topology", in *Proc. European Conference on Power Electronics and Applications (EPE)*, Toulouse, France, 2003.

[4] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a large power range", in *Proc. IEEE Bologna PowerTech Conference*, 23-26 June 2003, Bologna, Italy.

[5] K. Friedrich, "Modern HVDC PLUS application of VSC in modular multilevel converter topology", in *Proc. IEEE International Symposium on Industrial Electronics (ISIE)*, 4-7 July 2010, Bari, Italy, pp. 3807-3810.

[6] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system", *IEEE Trans. Power Delivery,* vol. 25, no. 4, pp 2903-2912, Oct. 2010.

[7] H.M. Pirouz and M.T. Bina, "New transformerless medium-voltage STATCOM based on a half-bridge cascaded converters", in *Proc. Power Electronic and Drive Systems and Technologies Conference (PEDSTC),* 17-18 Feb. 2010, Tehran, Iran, pp. 129-134.

[8] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter", *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1786-1799, July 2010.

[9] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless scalabale modular multilevel converters for HVDC transmission", in *Proc. IEEE Power Electronics Specialists Conference (PESC),* 15-19 June, Rhodes, Greece, pp. 174-179.

[10] R. Marquardt, "Modular multilevel converter: an universal concept for HVDC-networks and extended DC-bus-applications", in *Proc. IEEE International Power Electronics Conference (IPEC)*, 21-24 June 2010, Sapporo, Japan, pp. 552-557.

[11] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters", *IEEE Tran. Power Electron.*, vol. 24, no. 7, July 2009, pp. 1737-1746.

[12] A. Antonopoulos, L. Ängquist, and H.-P. Nee, "On dynamics and voltage control of the modular multilevel converter," in *Proc. European Conference on Power Electronics and Applications (EPE),* Sept. 2009, pp. 1–10.

[13] Q. Tu, Z. Xu, and L. Xu, "Reduced-switching frequency modulation and circulating current suppression for modular multilevel converters", *IEEE Tran. Power Delivery*, vol. 26, no. 3, pp. 2009-2017, July 2011.

[14] S. Ceballos, J. Pou, S. Choi, M. Saeedifard, and V. Agelidis, "Analysis of voltage balancing limits in modular multilevel converters", in *Proc. IEEE Industrial Electronics Conference (IECON'11)*, 7-10 Nov. 2011, Melbourne, Australia, pp. 4397-4402.