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N. Badereddine, Patrick Girard, Serge Pravossoudovitch, Christian Landrault ...+2 more authors

Institutions: University of Montpellier, Vienna University of Technology

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Minimizing Peak Power Consumption during Scan Testing: Test Pattern Modification with X Filling Heuristics

Nabil Badereddine, Patrick Girard, Serge Pravossoudovitch, Christian Landrault, Arnaud Virazel, Hans-Joachim Wunderlich

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Nabil Badereddine Patrick Girard Serge Pravossoudovitch Christian Landrault Arnaud Virazel

Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier – LIRMM
Université de Montpellier II / CNRS
161, rue Ada – 34392 Montpellier Cedex 5, France
Email: <name>@lirmm.fr URL: http://www.lirmm.fr/~w3mic

Hans-Joachim Wunderlich

Institut für Technische Informatik - Universität Stuttgart
Pfaffenwaldring 47 – 70569 Stuttgart, Germany
Email: wu@informatik.uni-stuttgart.de URL: http://www.ra.informatik.uni-stuttgart.de

***Abstract*—Scan architectures, though widely used in modern designs, are expensive in power consumption. In this paper, we discuss the issues of excessive peak power consumption during scan testing. We show that taking care of high current levels during the test cycle (i.e. between launch and capture) is highly relevant to avoid noise phenomena such as IR-drop or ground bounce. We propose a solution based on power-aware assignment of don't care bits in deterministic test patterns. For ISCAS'89 and ITC'99 benchmark circuits, this approach reduces peak power during the test cycle up to 89% compared to a random filling solution.**

***Keywords*—**DfT, Scan Testing, Power-aware Testing, Peak Power Consumption.

I. INTRODUCTION

While many techniques have evolved to address power minimization during the functional mode of operation, it is now mandatory to manage power during test mode. Circuit activity is substantially higher during test than during functional mode, and the resulting excessive power consumption can cause structural damage or severe decrease in reliability of the circuit under test [1, 2, 3, 4]. In the context of scan testing, the problem of excessive power during test is much more severe as the application of each test pattern requires a large number of shift operations that contributes to unnecessarily increasing the switching activity [2].

Power consumption must be analyzed from two different perspectives. Average power consumption is, as the name implies, the average power utilized over a long period of operation or a large number of clock cycles. Instantaneous power is the amount of power required during a small instant of time such as the portion of a clock cycle immediately following the system clock rising or falling edge. The peak power is the maximum value of the instantaneous power.

Average power consumption during scan testing can be controlled by reducing the scan clock frequency – a well known solution used in industry. In contrast, peak power consumption during scan testing is independent of the clock frequency and hence is much more difficult to control. As reported in recent industrial experiences [3], scan patterns in some designs may consume much more peak power over the normal mode and may result in failures during manufacturing test. Combined with high speed, excessive peak power during test also causes high rates of current (di/dt) in the power and ground rails and hence leads to excessive power and ground noise (V_{DD} or Ground bounce). This may erroneously change the logic state of some circuit nodes or flip-flops and cause some good dies to fail the test, thus leading to unnecessary loss of yield. Similarly, IR-drop and crosstalk effects are phenomena that may show up an error in test mode but not in functional mode. With high peak current demands during test, the voltages at some gates in the circuit are reduced. This causes these gates to exhibit higher delays, possibly leading to test fails and yield loss [5].

The problem of excessive peak power during scan testing can be divided in two sub-problems: excessive peak power during load/unload cycles and excessive peak power during the test cycle, denoted as TC and defined as the clock cycle between launch and capture.

Several techniques have been proposed for reducing test power dissipation during load/unload cycles [6]. Most of them are initially targeted for reducing average power but they usually can reduce peak power as well. The low power scan architectures proposed in [7, 8] reduce the clock rate on the scan cells during shift operations thus reducing the power consumption without increasing the test time. The technique presented in [9] consists in splitting the scan chain into a given number of length-balanced segments and in enabling only one scan segment during each clock cycle of the scan process. The solutions proposed in [10, 11]

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consist in assigning don't care bits of the deterministic test cubes used during test in such a way that it can reduce the peak power.

Compared to load/unload cycles, peak power reduction during TC is a less researched yet more challenging area. In this case, the problem is that TC is generally operated at-speed for high defect detection while load/unload cycles are generally operated at a lower speed for power consumption reason. Therefore, a high peak power during TC may lead to a situation where gates in the circuit exhibit higher delays [5], so that erroneous data may be captured in the scan chain at the end of TC. A possible solution to reduce peak power during TC is to use scan cell reordering [12, 13]. The main drawback of this technique is that power-driven chaining of scan cells cannot guarantee short scan connections and prevent congestion problems during scan routing. Another solution proposed in [11] is based on appropriately filling Xs of deterministic test cubes with values that can ensure low switching activity during TC. However, this technique is only applicable to specific and non classical clock schemes such as the launch-off-capture clock scheme used to target delay faults during scan.

Therefore, we propose in this paper a solution based on power-aware assignment of don't care bits in patterns of the deterministic test sequence (X filling techniques). X filling techniques have been already shown to be efficient to reduce power during test [5]. From a deterministic test sequence including don't cares, the Xs are filled with specific values (adjacent, 0 or 1) that minimize the occurrence of transitions and hence the peak power during TC. Compared to other solutions, such a filling technique has the advantage to be applicable after the end of the design process and does not require any modifications of the circuit. For ISCAS'89 and ITC'99 benchmark circuits, this approach reduces peak power during TC up to 89% compared to a random filling solution.

The remainder of the paper is organized as follows. In the next section, we discuss peak power issues during scan testing. In Section 3, we analyze peak power during the test cycles of scan testing and we highlight the importance of reducing this component of the power. In Section 4, we present the X filing heuristics and the flow used for the peak power evaluation. Section 5 presents the results obtained in terms of peak power reduction and test length. Section 5 concludes this paper.

II. PEAK POWER ISSUES

Power consumption must be analyzed from two different perspectives. Average test power consumption is, as the name implies, the average power utilized over a long period of operation or a large number of clock cycles. Instantaneous power or peak power (which is the maximum value of the instantaneous power) is the amount of power required during a small instant of time such as the portion of a clock cycle immediately following the system clock rising or falling edge. In [4], it is reported that test power consumption tends to exceed functional power consumption in both of these measures.

Average power consumption during scan testing can be controlled by reducing the scan clock frequency – a well known solution used in industry. In contrast, peak power consumption during scan testing is independent of the clock frequency and hence is much more difficult to control. Among the power-aware scan testing techniques proposed recently (a survey of these techniques is given in [6] and [14]), only a few of them relates directly to peak power. As reported in recent industrial experiences [3], scan patterns in some designs may consume much more peak power over the normal mode and can result in failures during manufacturing test. While, temperature-related or heat dissipation problems are more relate to excessive average power than peak power, the main problem with increased peak power concerns yield reduction and is explained in the sequel.

With high speed, excessive peak power during test causes high rates of current (di/dt) in the power and ground rails and hence leads to excessive power and ground noise (V_{DD} or Ground bounce). This can erroneously change the logic state of some circuit nodes and flip-flops and cause some good dies to fail the test, thus leading to unnecessary loss of yield. Similarly, IR-drop and crosstalk effects are phenomena that may show up an error in test mode but not in functional mode. IR-drop refers to the amount of decrease (increase) in the power (ground) rail voltage due to the resistance of the devices between the rail and a node of interest in the CUT. Crosstalk relates to capacitive coupling between neighboring nets within an IC. With high peak current demands during test, the voltages at some gates in the circuit are reduced. This causes these gates to exhibit higher delays, possibly leading to test fails and yield loss [5]. This phenomenon is reported in numerous reports from a variety of companies, in particular when at-speed transition delay testing is performed [3].

III. ANALYSIS OF PEAK POWER DURING SCAN

During scan testing, each test vector is first scanned into the scan chain(s). After a number of load clock cycles, a last shift in the scan chain launches the test vector. The scan enable (SE) signal is switched to zero, thus allowing the test response to be captured/latched in the scan chain(s) at the next clock pulse (see Figure 1). After that, SE is switched to one, and the test response is scanned out as the next test vector is scanned in.

There can be a peak power violation (the peak power exceeding a specified limit) during either the load/unload cycles or during TC. In both cases, a peak power violation can occur because the number of flip-flops that change value in each clock cycle can be really higher than that during functional operation. In [4], it is reported that only 10-20 % of the flip-flops in an ASIC change value during one clock cycle in functional mode, while 35-40 % of these flip-flops commutate during scan testing.

In order to analyze when peak power violation can occur during scan testing, we conducted a set of experiments on benchmark circuits. Considering a single scan chain composed of *n* scan cells and a deterministic test

sequence for each design, we measured the current consumed by the combinational logic during each clock cycle of the scan process. We pointed out the maximum value of current during the *n* load/unload cycles of the scan process and during TC (which is the last during a single clock cycle). Note that current during TC is due to transitions generated in the circuit by the launch of the deterministic test vector V_n (see Figure 1).

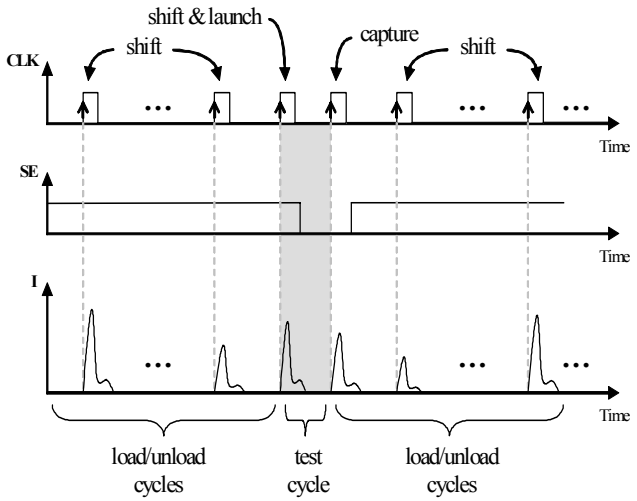

Figure 1. Scan testing and current waveform

Identification of peak power violation cannot be done without direct comparison with current (or power) measurement made during functional mode. However, this would require knowledge of functional data for each benchmark circuit. As these data are not available, the highest values of current we pointed out are not necessarily peak power (current) violations. There are simply power (current) values that can lead to peak power (current) violation during scan testing. Reports made from industrial experiences have shown that such violations occur during manufacturing scan testing [3, 4].

The benchmarking process was performed on circuits of the ISCAS'89 and ITC'99 benchmark suites. We report in Table 1 the main features of these circuits. For each experimented circuit we give the number of scan cells, the number of gates, the number of deterministic test patterns and the associated fault coverage (FC). All experiments are based on deterministic testing from the ATPG tool "TetraMAX™" of Synopsys [15]. The missing faults in the FC column are redundant or aborted faults. Primary inputs and primary outputs were not included in the scan chain, but were assumed to be held constant during scan-in and scan-out operations. Random initial logic values were assumed for the scan flip-flops.

Results concerning peak power consumption are given in Table 2. We have reported the peak power (expressed in milliWatts) consumed during the load/unload cycles (second column), and that consumed during TC (third column). These values represent the maximum over the entire test sequence. Power consumption in each circuit was estimated by using PowerMill® of Synopsys [16], assuming a power supply voltage of 2.5 Volts and technology parameters extracted from a 0.25µm digital CMOS standard cell library.

Table 1. Features of experimented circuits

Circuit	# scan cells	# gates	# patterns	FC (%)
b04s	66	512	58	99.08
b09	28	129	28	100
b10	17	155	44	100
b11s	31	437	62	100
b12	121	904	94	100
b13s	53	266	30	100
b14s	245	4444	419	99.52
b17s	1415	22645	752	98.99
s1196	18	529	137	100
s5378	179	2779	151	100
s9234	228	5597	161	99.76
s13207	669	7951	255	99.99
s38417	1636	22179	145	100

These results show that peak power consumption is always higher during the load/unload cycles than during TC. This result was quite predictable as the number of clock cycles during the load/unload phase is much more than one. More importantly, these results show that even if peak power is higher during the load/unload cycles, peak power during TC is in the same order of magnitude. This may lead to problematic noise phenomena during TC.

Table 2. Peak power during scan testing

Circuit	Peak power consumption (mW)	
	load / unload	*test cycle*
b04s	77.50	59.60
b09	34.43	30.48
b10	27.88	23.71
b11s	50.42	41.27
b12	113.84	101.46
b13s	61.09	52.92
b14s	395.55	319.83
b17s	1038.35	1118.68
s1196	66.89	10.03
s5378	197.76	179.66
s9234	359.68	339.88
s13207	499.68	483.30
s38417	1121.80	1074.33

Let us consider again the IR-drop phenomenon. As discussed earlier, it is due to a high peak current demand that reduces the voltages at some gates in the CUT and hence causes these gates to exhibit higher delays. The gate delays do not affect the load/unload process as no value has to be captured/stored during this phase. Conversely, the gate delays can really affect TC because the values of output nodes in the combinational logic have to be captured in the scan flip-flops. As this operation is generally performed at-speed, this phenomenon is therefore likely to occur during this phase and negatively impact test results and thus yield. We can therefore conclude that taking care of peak power

during TC and trying to minimize the switching density of the circuit during this phase are really relevant and require new development of dedicated techniques.

IV. NON-RANDOM FILLING HEURISTICS

Considering the fact that minimizing peak power during TC is needed, we present in this section a power-aware assignment of don't care bits in patterns of a deterministic test sequence. Then, we present the results in terms of peak power reduction during TC and test time.

In conventional ATPG, don't care bits (Xs) are filled in randomly, and then the resulting completely specified pattern is simulated to confirm detection of all targeted faults and to measure the amount of "fortuitous detection" – faults which where not explicitly targeted during pattern generation but were detected anyway. It is interesting to note that the fraction of don't care bits in a given pattern is nearly always a very large fraction of the total available bits [17, 18]. This observation remains true despite the application of state-of-the-art dynamic and static test pattern compaction techniques. The presence of significant fraction of don't care bits presents an opportunity that can be exploited for power minimization.

In order to avoid congestion problems inherent to scan chain modification techniques and to allow at-speed testing, pattern modification techniques can be used to reduce peak power during TC. Here, the idea is to use a test generation process during which non-random filling is used to assign values to don't care bits (Xs) of each test pattern of a deterministic test sequence. Classical non-random filling heuristics are:

- Adjacent filling also called MT-filling (Minimum Transition filling): all don't care bits in a test pattern are set to the value of the last encountered care bit (working from left to right).When applying MT-filling, the most recent care bit value is used to replace each `X' value. When a new care bit is encountered, its value is used for the adjacent X's.
- 0-filling: all don't care bits in a test pattern are set to '0'.
- 1-filling: all don't care bits in a test pattern are set to '1'.

For example, consider the single test pattern 0XXX1XX0XX0XX. If we apply each of the three non-random filling heuristics, the resulting pattern will be:

- 0000111000000 with MT-filling.
- 0000100000000 with 0-filling,
- 0111111011011 with 1-filling,

These non-random filling heuristics (among few others) have been evaluated in [5] to measure the reduction in average power consumption during scan shifting (load/unload cycles). Results reported in [5] indicate that the MT-filling technique does an excellent job of lowering overall switching activity while still maintaining a reasonably increase in pattern volume.

From our side, we have evaluated these heuristics to measure the reduction in peak power consumption during TC with respect to a random filling of don't care bits. The evaluation of the proposed heuristics was done with the flow presented in Figure 2. We first start with a deterministic test generation with non-random filling. The Xs of each pattern are assigned according to the heuristics. Then, the resulting test sequences are minimized by removing the unnecessary patterns. We also generate a test sequence with standard ATPG options on which the Xs are filled randomly. At the end, we have to compute the peak power consumed by the test sequence generated with a random filling option and that obtained with the non-random filling heuristics. The comparisons are done on the peak power consumption as well as on the test length.

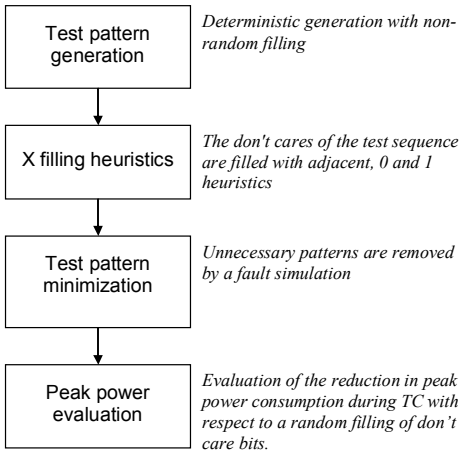

Figure 2. Peak power evaluation flow

V. EXPERIMENTAL RESULTS

Experiments performed on ISCAS'89 and ITC'99 benchmark circuits have been done to estimate the reduction in peak power obtained during TC. A sample of these results is shown in Table 3. For each circuit, we report the peak power during TC obtained first from a deterministic test sequence with random filling and next with the MT-filling, 0-filling and 1-filling heuristics. For the evaluation in both cases, the deterministic test sequences presented in Table 1 were used assuming random initial logic values for the scan flip-flops. Peak power is expressed in milliWatts and the values reported for each circuit are a mean of peak power (or instantaneous power) consumed during each test cycle of the scan process. Note that these values differ from those in Table 2 which represent a maximum over the entire test sequence. For each heuristic, the columns "reduct." in Table 3 give the reduction achieved. The values in bold correspond to the best results. Complete results on benchmark circuits have shown that peak power reduction up to 89% can be achieved with the MT-filling technique.

These results show the efficiency of the used heuristics in terms of peak power reduction in the circuit. Most of the time, the MT-filling heuristic performed better than the others as it ensures less activity in the scan chain. But this is not always true as the structural properties of a given circuit

Table 3. Peak power saving in the CUT during the test cycles

Circuits	Random Filling	MT-Filling		0-Filling		1-Filling	
	peak [mW]	*peak [mW]*	*reduct. (%)*	*peak [mW]*	*reduct. (%)*	*peak [mW]*	*reduct. (%)*
b04s	44.03	31.32	28.9	22.18	**49.6**	40.88	7.1
b09	19.80	15.56	**21.4**	15.99	19.3	16.31	17.6
b10	14.74	8.79	**40.4**	13.67	7.3	11.29	23.4
b11s	28.43	22.59	**20.6**	22.98	19.2	26.28	7.6
b12	82.21	26.69	67.5	26.16	**68.2**	34.68	57.8
b13s	39.04	15.62	**60.0**	21.89	43.9	19.62	49.7
b14s	178.0	131.23	26.3	123.30	**30.7**	197.08	-10.7
b17s	961.86	191.07	**80.1**	214.09	77.7	233.35	75.7
s1196	4.71	0.97	**79.3**	1.97	58.2	1.6	66.1
s5378	146.97	37.9	**74.2**	47.71	67.5	43.03	70.7
s9234	240.02	80.39	**66.5**	132.89	44.6	140.04	41.6
s13207	402.62	42.33	**89.5**	62.61	84.4	48.46	87.9
s38417	978.1	275.8	71.8	171.30	82.5	155.34	**84.1**

may sometimes favor one heuristic rather than another. For example, as circuit b14s exhibits a majority of AND/NAND gates (more than 500 gates) connected to the flip-flops compared to only 80 OR/NOR gates, it was highly predictable that the 0-filling heuristic performs better for this circuit. This is confirmed by results in Table 3 where the 0-filling induces a 30.7% reduction instead of a 10.7% increase for the 1-filling. This observation should be used to propose more efficient but more complicated X filling heuristics.

Another important point that has to been taken into account is the test length. In fact, a non-random filling solution may increase the resulting test sequence compared to the initial one using random filling assignment of don't cares. Table 4 reports the increase of test length obtained with the three non-random filling heuristics compared to the initial test sequence with random filling.

Table 4. Test sequence increase with non-random filling heuristics

Circuit	% of additional patterns		
	MT-filling	*0-filling*	*1-filling*
b04s	0	1.81	-1.81
b09	0	0	0
b10	0	0	-2.32
b11s	0	1.66	-1.66
b12	7.52	6.45	6.45
b13s	10	16.66	10
b14s	1.22	1.46	1.46
b17s	4.19	6.79	6.64
s1196	2.34	4.68	2.34
s5378	15.17	13.79	33.1
s9234	5.66	9.43	0.62
s13207	0	6.29	3.54
s38417	13.88	138.19	151.38

These comparisons clearly show that for small circuits the non-random filling heuristics are not costly in terms of test time. For bigger circuits, the number of additional patterns in the test sequence remains low compared to the peak power reduction achieved. We obtain a mean of 12% on the overall pattern volume. We have also to notice that, for circuit s38417, the resulting test length is twice the one with random-filling when applying 0-filling or 1-filling. This problem is due to scarce defined test vectors. For such vectors, filling the Xs by a 0 (1) results in an almost 0 (1) test vectors with low fault detection capability. This observation should be accounted for more efficient but more complex X filling heuristics.

These X filling heuristics can be used to reduce the peak power during TC in order to avoid noise phenomena provoked by IR-drops or ground bounces. We have also evaluated the peak power reduction during load/unload cycles achieved by these X filling techniques. A sample of these results is shown in Table 5. For each heuristics, we report the reduction achieved. For ISCAS'89 and ITC'99 benchmarks circuits, these heuristics reduce peak power during load/unload cycles up to 58% (with a mean of 27%) compared to a random filling solution. Through these results, we can see that problems as flipping of scan data due to a high peak power consumption during load/unload are also avoid by these X filling heuristics.

Table 5. Peak power saving in the CUT during load/unload cycles

Circuit	reduct. (%)		
	MT-filling	*0-filling*	*1-filling*
b04s	20.65	33.73	12.42
b09	19.66	14.64	18.71
b10	20.75	11.33	12.39
b11s	10.87	19.13	2.46
b12	58.43	57.17	51.05
b13s	39.72	42.79	32.56
b14s	19.53	42.44	6.31
s1196	7.84	9.35	11.09
s5378	52.58	45.04	57.24
s9234	34.06	31.33	30.51

Pattern modification techniques are therefore promising solutions to reduce peak power during TC. In addition,

these techniques require no modification of the basic design of the circuit and no additional DfT features are required to implement these solutions. Finally, at-speed testing is possible so that the defect coverage of the initial test sequence can be maintained.

VI. CONCLUSION

In this paper, we have shown that excessive peak power consumption during all test cycles of scan testing has to be controlled to avoid noise phenomena such as IR-drop or ground bounce. Without caution, these phenomena may lead to yield loss during manufacturing test as test cycles are generally operated at-speed. In this paper, our target was to minimize the peak power consumption during test cycles.

The reduction of peak power during TC can be addressed from different perspectives. In this paper, we have proposed a solution based on a power-aware assignment of don't care bits in deterministic test patterns. Our future work will consist in investigating much more on this type of solutions in order to develop an X filling heuristic based on a structural analysis of the circuit.

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