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Minimum Cost Fault Tolerant Adder Circuits in Reversible Logic Synthesis

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***Abstract*—Conventional circuit dissipates energy to reload missing information because of overlapped mapping between input and output vectors. Reversibility recovers energy loss and prevents bit error by including Fault Tolerant mechanism. Reversible Computing is gaining the popularity of various fields such as Quantum Computing, DNA Informatics and CMOS Technology etc. In this paper, we have proposed the fault tolerant design of Reversible Full Adder (RFT-FA) with minimum quantum cost. Also we have proposed the cost effective design of Carry Skip Adder (CSA) and Carry Look-Ahead Adder (CLA) circuits by using proposed fault tolerant full adder circuit. The regular structures of *n*-bit Reversible Fault Tolerant Carry Skip Adder (RFT-CSA) and Carry Look-ahead Adder (RFT-CLA) by composing several theorems. Proposed designs have been populated by merging the minimization of total gates, garbage outputs, quantum cost and critical path delay criterion and comparing with exiting designs.**

***Index Terms*—Reversible Logic, Fault Tolerant, Carry Skip Adder, Full Adder, Quantum Cost**

I. Introduction

Higher level of integration and use of fabrication processes have dramatically reduced the heat loss over the last decades. Landauer [1] proved that logic computation that are not reversible, necessarily generate kT*log2 joules energy per bit information loss, where k means Boltzman's constant and T is the absolute root temperature where computation is performed. Reversible circuit doesn't loss information by considering a unique mapping between input and output. By using reversible computation zero power dissipation circuits is possible [2]. Reversible circuits are fundamentally different from traditional irreversible and are used to emphasis future technology. However reversible computation admits to generate multiple functions simultaneously. Quantum Computation is also gaining popularity as some exponentially hard problem can be solved in polynomial time and reversibility can be used to construct Quantum circuits [3].

Different arithmetic operations were realized by using reversible primitives since few decades earlier. Existing designs of Full Adder circuit were proposed in [4], [5], [6], [7] and finally generalized by [3] but any of these designs has no fault detection capability. Fault Tolerant full adder circuit was proposed in [8], [9], [10] without any generalization or cost effective structure. We have achieved more compact design of *n*-bit adder circuit which shows better performance than existing designs [6], [7], [8], [9], [12], [11]. Here we have pictured the regular structure of Fault Tolerant adder circuits by using Fault Tolerant gates (Fig. 1 shows the design of Fredkin (FRG) [13] and New Fault Tolerant (NFT) [14] gates).

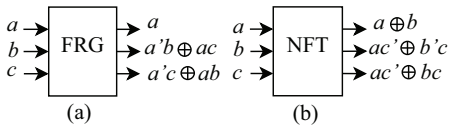

Fig. 1. (a) Fredkin Gate and (b) New Fault Tolerant Gate

Rest of the paper is organized as follows: Section II discusses the construction of Reversible Logic, Fault Tolerant method, Quantum realization and Arithmetic Full Adder circuit. Section III illustrates the proposed cost effective design of Reversible Fault Tolerant Full Adder (RFT-FA), Carry Skip Adder (RFT-CSA) and Carry Look-Ahead Adder (RFT-CLA) by attaching the comparison with existing designs. Section IV describes a brief overview of the performance of proposed designs. Section V ends the paper with concluding remarks.

II. Background Study

In this section, we have discussed about the basic definitions and properties of Reversible Logic, Fault Tolerant mechanism and Quantum realization of reversible circuit.

A. Reversible Logic

Reversible Logic always retrains an unique mapping between input and corresponding output vectors.

Definition 1. The unit logic entity of reversible circuit is called **Reversible Gate** where the number of inputs is equal to the number of outputs and there is an one to one mapping between input and output vectors [3].

Let, the input vector, $I_v = \{I_1, I_2, \ldots, I_n\}$ and output vector, $O_v = \{O_1, O_2, \ldots, O_n\}$ then according to the above definition the relationship is $I_v \leftrightarrow O_v$.

Definition 2. The input vector, I_v and output vector, O_v for 2×2 **Feynmen Gate (FG)** [15] is defined as follows:

$$I_v = \{a,\ b\} \text{ and}$$
$$O_v = \{a,\ a \oplus b\}$$

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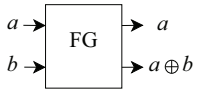


Fig. 2. 2×2 Feynman/CNOT Gate

TABLE I
TRUTH TABLE OF FEYNMAN GATE

Input		Output	
a	*b*	*a*	*a*⊕*b*
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Fig. 2 shows the block diagram of Feynman Gate and Table I shows the unique mapping between input and output vectors of Feynman gate.

Definition 3. The **Garbage Output** of any reversible gate or circuit is unwanted or unused output which will not be used in future rather than for checking reversibility [3].

For example, the Exclusive-OR operation can be realized by using only one Feynman Gate which produces an extra dummy output (a) along with its principle output signal ($a \oplus b$) to preserve reversibility (shown in Fig. 2).

Definition 4. Delay of any circuit is the number of maximum gate(s) from any input to any output where both ends preserve a continuous communication line. Total delay to generate EX-OR function is 1 (shown in Fig. 2) [3].

Definition 5. The input vector, I_v and output vector, O_v of 3×3 **Fredkin Gate (FRG)** [13] is defined as follows:

$$\begin{aligned} I_v &= \{a,\ b,\ c\} \text{ and} \\ O_v &= \{a,\ \bar{a}b \oplus ac,\ \bar{a}c \oplus ab\} \end{aligned}$$

The block representation of FRG is shown in Fig. 1(a).

Definition 6. The 3×3 dimensional **Feynman Double Gate (F2G)** [16] is another reversible gate where the input vector, I_v and the output vector, O_v are defined as follows:

$$\begin{aligned} I_v &= \{a,\ b,\ c\} \text{ and} \\ O_v &= \{a,\ a \oplus b,\ a \oplus c\} \end{aligned}$$

The Block Diagram and the unique mapping between input and output vectors of Feynman Double (F2G) gate can be shown as Fig. 3 and Fig. 4 respectively.

Definition 7. The input vector, I_v and output vector, O_v of 3×3 **New Fault Tolerant (NFT) gate** [14] as follows:

$$\begin{aligned} I_v &= \{a,\ b,\ c\} \text{ and} \\ O_v &= \{a \oplus b,\ a\bar{c} \oplus \bar{b}c,\ a\bar{c} \oplus bc\} \end{aligned}$$

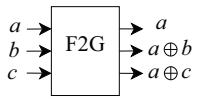


Fig. 3. 3×3 Feynman Double Gate

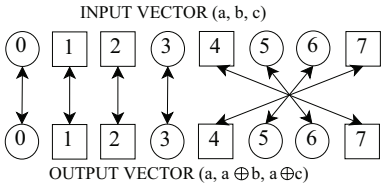


Fig. 4. Feynman Double Gate (F2G) preserves Fault Tolerance over input-output unique mapping

The block diagram of NFT gate is shown in Fig. 1(b).

Definition 8. The input and output vectors of 4×4 **Modified TSG (MTSG) gate** [3] are I_v and O_v respectively and can be defined as follows:

$$\begin{aligned} I_v &= \{a,\ b,\ c,\ d\} \text{ and} \\ O_v &= \{a,\ a \oplus b,\ ab \oplus c,\ (a \oplus b)c \oplus ab \oplus d\} \end{aligned}$$

Another popular reversible gates are Peres Gate (PG) [18], Toffoli Gate (TG) [17] and New Gate (NG) [19] etc.

B. Fault Tolerant Method

Reversibility recovers bit loss but is not able to detect bit error in circuit. Fault Tolerant reversible circuit is capable to prevent error at outputs.

Definition 9. Fault Tolerant (FT) gate, also called Conservative Reversible Gate [9] which means the Hamming weight of its input and output are equal.

Let, the input and output vectors of any Fault Tolerant gate are I_v= $\{I_0, I_1, \ldots, I_{n-1}\}$ and O_v= $\{O_0, O_1, \ldots, O_{n-1}\}$ where the following equations (1) and (2) must be preserved:

$$I_v \leftrightarrow O_v \quad (1)$$

$$I_0 \oplus I_1 \oplus \ldots \oplus I_{n-1} = O_0 \oplus O_1 \oplus \ldots \oplus O_{n-1} \quad (2)$$

For example, the Fault Tolerance property of Feynman Double gate (shown in Fig. 3) can be verified from Fig. 4 where square and circle represents ODD and EVEN parities respectively and the equivalent decimal values of input-output vectors are represented as corresponding decimal number (0-7).

F2G, FRG and NFT are 3×3 dimensional and MIG is 4×4 dimensional fault tolerant gate having unique mapping between Input and Output vectors. The input and corresponding output parities of Fault Tolerant gates are same [16]. In early, fault tolerant Gate is also called Parity Preserving Gate.

C. Quantum Realization

Quantum realization is another fact to judge the efficiency of reversible circuit which uses matrix multiplication rather than conventional Boolean operations. In Quantum Mechanics, the states of a particle is represented by qubits instead of bits. The operations over on qubits are matrix multiplication specified by using quantum gates (shown in Fig. 5) [20].

Definition 10. Quantum Cost (QC) of any reversible circuit is the total number of 2×2 quantum primitives that are used to realize equivalent quantum circuit [3], [21].

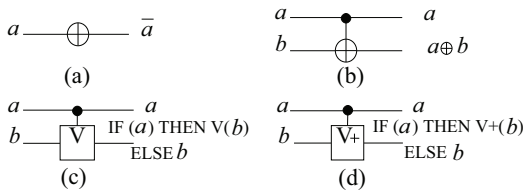


Fig. 5. Elementary Quantum Logic gates: (a) NOT, (b) Exclusive-OR, (c) Square Root of NOT (SRN) and (d) Hermitian matrix of SRN

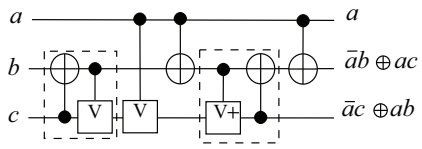


Fig. 6. Quantum circuit realization of Fredkin gate [13]

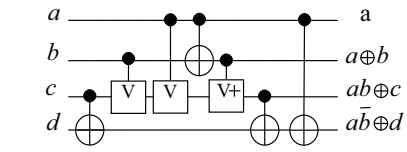
For example, the quantum cost of Feynman gate (shown in Fig. 2) is one because single 2×2 Quantum EX-OR gate is enough to realize its operations. The quantum circuit of several reversible gates is presented in [3]. Fig. 6 shows the quantum representation of Fredkin gate and the cost is 5.

Here we have proposed the quantum realization of reversible fault tolerant Modified IG (MIG) [8] and New Fault Tolerant (NFT) [14] gates by using quantum EX-OR, Square Root of NOT (SRN or V) and Hermitian of SRN (V^+) gates as shown in Fig. 7. According to design, the quantum cost of Modified IG (MIG) (New Fault Tolerant (NFT)) gate is 7(5).

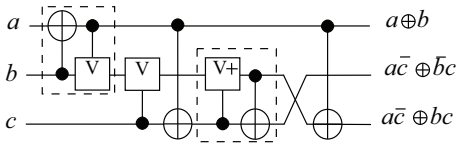
D. Arithmetic Adder Circuit

Adder is an essential part of digital circuits to implement most of the mathematical operations. Single bit adder or Full Adder is the unit entity of any kind of computing devices.

Definition 11. A **Full Adder** is a digital circuit which takes two bits from two operands and carry bit from prior stage as input and generates the summation of three bits and corresponding carry as output [3].



(a) Modified IG gate, Quantum Cost= 7



(b) New Fault Tolerant Gate, Quantum Cost = 5

Fig. 7. Quantum equivalent circuit realization of MIG [8] and NFT [14] by using quantum primitives

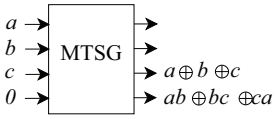


Fig. 8. Full adder Realization by using MTSG [3]

Let, a and b both are the single bit operand and c_{in} is the carry of previous stage then outputs of full adder circuit, Sum (s) and Carry (c_{out}) can be defined as follows:

$$\begin{aligned} s &= a \oplus b \oplus c_{in} \\ c_{out} &= ac_{in} \oplus bc_{in} \oplus ab \end{aligned}$$

For example, single MTSG gate able to realize reversible full adder circuit as shown in Fig. 8.

Following section has described the proposed designs of Fault Tolerant Full Adder (RFT-FA) circuit followed by Carry Skip Adder (RFT-CSA) and Carry Look-ahead Adder (RFT-CLA) by including their performances over existing designs.

III. Proposed Design

In this section, first we have described the proposed design of cost effective Reversible Fault Tolerant Full Adder by using New Fault Tolerant (NFT) and Feynman Double (F2G) gates. Then we have described the design of Fault Tolerant Carry Skip (RFT-CSA) and Carry Look-ahead (RFT-CLA) adders by using proposed design of Fault Tolerant Full Adder.

A. Fault Tolerant Full Adder Design

The quantum cost of New Fault Tolerant (NFT)(shown in Fig. 7(b)) and Fredkin (FRG) gates are same i.e. 5. But the quantum cost of Feynman Double (F2G) gate is 2. We have used New Fault Tolerant (NFT) and Feynman Double (F2G) gates because of reusability of proposed adder circuit for Carry Skip Adder and Carry Look-ahead Adder.

Definition 12. Single NFT Full Adder (SNFA) is a Fault Tolerant full adder circuit which consists of one New Fault Tolerant (NFT) gate and three Feynman Double (F2G) gates where the quantum cost is 11 and the total number of garbage output is 3 (shown in Fig. 9).

Theorem 1: The minimum number of garbage bit to realize Reversible Fault Tolerant Full Adder circuit is 3.

Proof: Let, a, b and c_{in} are the inputs of a full adder circuit where s and c_{out} are the corresponding outputs. There are three different states at the inputs (a, b and c_{in}) where the outputs (s and c_{out}) produce same patterns as shown in Table II. For any parity preserving reversible circuit, total number of EVEN or ODD parity at input or output is equal. Table II shows that the all input patterns are EVEN but the corresponding output patterns are ODD. Turning three ODD patterns at output into EVEN by adding two extra bits is not possible. Because two bits can represent 2^2 different states where 00 and 11 (01 and 10) are EVEN (ODD) only. So, Reversible Full Adder circuit requires at least 3 garbage bits to make itself Reversible Fault Tolerant Full Adder.

TABLE II
INPUT-OUTPUT PATTERNS OF FULL ADDER

Input			Output	
a	b	c_{in}	s	c_{out}
0	1	1	0	1
1	1	0	0	1
1	0	1	0	1

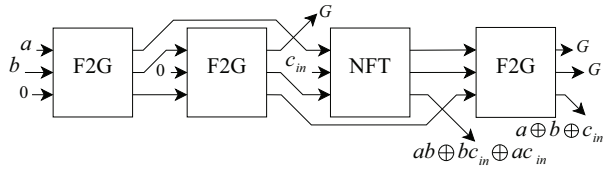


Fig. 9. Proposed design of Fault Tolerant Single NFT Full Adder (SNFA)

TABLE III
COMPARISON BETWEEN PROPOSED AND EXISTING DESIGNS OF REVERSIBLE FAULT TOLERANT FULL ADDER

Fault Tolerant Full Adder	Total Gates		GB	QC
	3×3	4×4		
Proposed	4	0	3	11
Existing [8]	0	2	3	14
Existing [9]	5	0	4	25
Existing [10]	6	0	6	18

GB= Garbage bits, QC= Quantum Cost

The performance analysis between the proposed design and all other existing designs is shown in Table III.

Table III shows that the Ref. [8] uses two gates and the corresponding quantum cost is 14 where proposed design uses low dimensional four gates and the quantum cost is only 11.

B. Fault Tolerant Carry Skip Adder

Fast carry emission is the main concern of Carry Skip Adder and it depends on: firstly, if any operand is equal to logical 1 then the full adder propagates c_{in} to c_{out} and secondly, it also generates carry itself (c_{out} independent on c_{in}).

Definition 13. Propagate is a simple XOR operation between two operands which is responsible for only bypassing the carry of previous stage to next stage [6].

Let, X= (x_0, x_1, x_2, …, x_{n-1}) and Y= (y_0, y_1, y_2, …, y_{n-1}) are two n-bit operands where Propagate p_i of i^{th} stage can be defined from x_i and y_i as follows:

$$p_i = x_i \oplus y_i$$

Definition 14. Generate is an AND operation which enables current stage of adder to generate carry for next stage [6]. So the Generate of i^{th} stage as follows:

$$g_i = x_i y_i$$

Definition 15. Reversible Fault Tolerant Carry Skip Adder (RFT-CSA) consists of SNFAs and FRGs to perform summation and propagate carry respectively which reduce the delay or bypassing carry due to the recalculation of carry for the next stage. If any input is equal to a logical 1, then it propagates the carry input to the carry output [9].

Proposition 1. n-bit RFT-CSA can be realized by using (3n+1) F2Gs, n FRGs and n NFTs.

Proof: Let, n SNFAs are needed to realize n-bit RFT-CSA (each SNFA consists of three F2Gs and one NFT) to generate sum (s_i) and Propagate (p_i) where i= 0, 1, 2, …, (n-1). And n FRGs are needed for performing AND operation among n Propagates with c_{in}. So the calculation of the number of NFT (NFT_{CSA}), the number of FRG (FRG_{CSA}) and the number of F2G ($F2G_{CSA}$) to implement n-bit RFT-CSA is as follows:

$$\begin{aligned} NFT_{CSA} &= n, \\ FRG_{CSA} &= n \text{ and} \\ F2G_{CSA} &= 3n \end{aligned}$$

But RFT-CSA needs another extra F2G to generate final carry, c_{out} by performing EXOR operation between c_{n-1} and ($p_{n-1}p_{n-2}\ldots p_0 c_{in}$).

$$F2G_{CSA} = 3n + 1$$

So, n-bit RFT-CSA can be realized by using (3n+1) F2Gs, n FRGs and n NFTs.

Proposition 2. n-bit RFT-CSA can be realized with (n+5) Critical Path Delay.

The proposed design of 4-bit RFT-CSA is shown in Fig. 10 which uses proposed full adder (SNFA) circuit.

Finally, the total garbage (GB_{CSA}) and Quantum Cost (QC_{CSA}) of n-bit RFT-CSA can be written as follows:

$$\begin{aligned} GB_{CSA} &= 4n \\ QC_{CSA} &= 5 * 2n + 2 * (3n + 1) \\ &= 16n + 2 \end{aligned}$$

The comparison between proposed RFT-CSA and existing designs is shown in Table IV. Carry Skip Adder is more reliable in case of hardware implementation where circuit cost is another factor of design with respect to Delay. In Table IV, the QC of proposed design is 66 which is minimum than all existing designs. Although the number of 3×3 gates of [7] is about equal to proposed design but QC of proposed design has been improved 20% because of using cost effective Feynman Double gate (QC of Feynman Double gate is only 2). The proposed cost-effective design of Fault Tolerant CSA (RFT-CSA) has improved cost factor having fault detection as well.

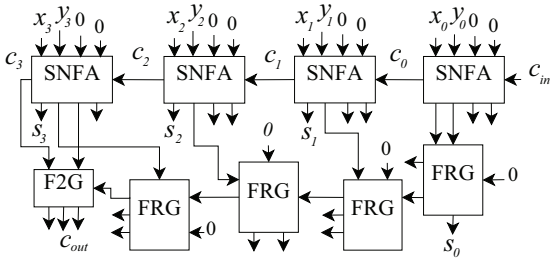


Fig. 10. Proposed design of Reversible Fault Tolerant Carry Skip Adder

TABLE IV
COMPARISON BETWEEN PROPOSED AND EXISTING DESIGNS OF CARRY SKIP ADDER

Carry Skip Adder	Total Gates		GB	DL	QC
	3×3	4×4			
Proposed†	21	0	16	9	66
Existing [7]§	22	0	26	16	88
Existing [8]†	6	8	19	13	80
Existing [9]§	24	0	23	14	120

† Fault Tolerant, § with fan-out
GB= Garbage bits, DL= Delay, QC= Quantum cost

TABLE V
COMPARISON BETWEEN PROPOSED AND EXISTING DESIGN [8] OF FAULT TOLERANT CARRY LOOK-AHEAD ADDER

Fault Tolerant Carry Look-ahead Adder	Total Gates		GB	DL	QC
	3×3	4×4			
Proposed (4-bit)	16	0	12	7	44
Existing [8] (2-bit)	15	4	28	12	73

GB= Garbage bits, DL= Delay, QC= Quantum cost

C. Fault Tolerant Carry Look-ahead Adder Circuit

This section introduces the design of Reversible Fault Tolerant Carry Look-ahead Adder (RFT-CLA) circuit overlaps the performance of all existing designs. Proposed design of RFT-CLA is based on New Fault Tolerant (NFT) and Feynman Double (F2G) gates where the carry is generated before sum.

Definition 16. Reversible Fault Tolerant Carry Look-ahead Adder (RFT-CLA) consists of serial attachment of n SNFAs but the work as a carry generator itself where the carry output of i^{th} stage (c_i) is produced before sum s_i where i= 0, 1, 2, …, (n-1).

Proposition 3. n-bit RFT-CLA can be realized by using the combination of n NFTs and n F2Gs.

Proposition 4. The Delay of n-bit Reversible Fault Tolerant CLA ($D_{RFT-CLA}$) can be minimized to (n+3).

Proof: According to Definition 4, the Delay of any circuit is the number of maximum gates laying on contiguous path of any input to output. The Delay of SNFA, D_{SNFA}= 4 to generate sum not carry. Delay of parallel adder circuit depends on carry propagation (from c_{in} to c_{out}) of every stage. Any n-bits RFT-CLA needs n SNFAs where Delay of RFT-CLA, $D_{RFT-FA} \neq 4n$. Because carry input (c_i) of i_{th} stage is generated by spending 1 units Delay where i= 0, 1, 2, …, (n-1). In first stage, extra two units Delay is added because of first carry output (c_0) generation is related to operands at first stage. On the other hand, last stage has extra single unit Delay because the final sum is generated after one stage of generation of final carry (c_{out}). So the Delay calculation for n-bits RFT-CLA is as follows:

$$D_{RFT-FA} = n + 3$$

Therefore an n-bit RFT-CLA can be realized by using (n+3) unit Delay.

Proposition 5. An n-bit Reversible Fault Tolerant Carry Look-ahead Adder (RFT-CLA) can be realized with minimum Quantum Cost 11n.

Proposition 6. An n-bit Reversible Fault Tolerant Carry Look-ahead Adder (RFT-CLA) can be realized with minimum Garbage 3n.

Fig. 11 shows the proposed design of 4-bit Reversible Fault Tolerant Fast Adder and Table V shows the performance of proposed design by comparing with existing [8] design of 2-bit reversible Fault Tolerant Carry Look-ahead Adder.

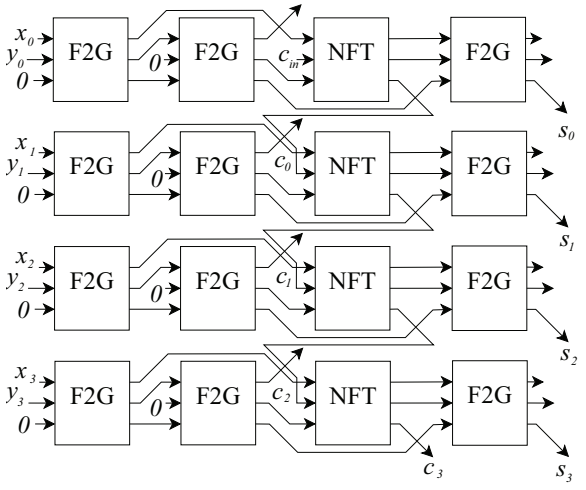


Fig. 11. Efficient Design of 4-bit Reversible Fault Tolerant Carry Look-ahead Adder

IV. PERFORMANCE ANALYSIS

Previous two sections have discussed about the design of Reversible Fault Tolerant Full Adder, Carry Skip Adder and Carry Look-ahead Adder and the comparison of corresponding existing designs. This section have presented an abstract overview of proposed designs and the complexity analysis for n-bit Reversible Fault Tolerant Adder circuits. Fig. 12 represents that the performance of proposed 4-bit Reversible Fault Tolerant Carry Skip Adder is better compared to existing [8]. The number of gates in proposed design is greater than existing design [8] because of dimensional impact (lower dimension is preferable) which can be treated as negligible because of other factors (delay, garbage and quantum cost). Table VI describes the another evolutionary observation between proposed n-bit Reversible Fault Tolerant Carry Skip Adder and Carry Look-ahead Adder designs. We have already given the comparative study between proposed and existing designs of reversible fault tolerant Carry Skip Adder (Carry Look-ahead Adder) in Table IV (Table V) individually. Proposed designs of CSA and CLA demand better performance than existing designs in terms of number of gates, garbage outputs, delay and quantum cost. Along with the lower dimensional (3×3) fault tolerant gates our proposed designs have got more flexibility in reversible CMOS [22] realization. Pictorial representation of performance evaluation of Reversible Fault Tolerant Carry Look-ahead adder circuit over Carry Skip Adder circuit is shown in Fig. 13.

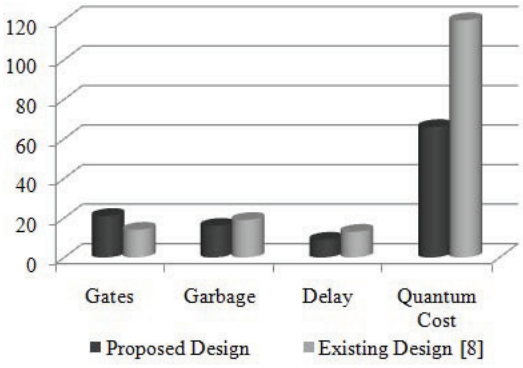


Fig. 12. Comparison between Proposed design and Existing design [8] of 4-bit Carry Skip Adder

TABLE VI
COMPARISON AMONG PROPOSED REVERSIBLE FAULT TOLERANT FAST, CARRY SKIP AND CARRY LOOK AHEAD ADDER

Proposed Adder Cirucits	Total Gates		GB	DL	QC
	FRG	F2G			
RFT-CLA †	n	$3n$	$3n$	n+3	$11n$
RFT-CSA	$2n$	$3n$+1	$4n$	n+5	$16n$+2

† Minimum Delay and Minimum cost
GB= Garbage bits, DL= Delay, QC= Quantum cost

V. CONCLUSION

In our proposed designs, we have combined all marginal cost factors (Gate cost, Delay, Garbage and Quantum cost) to generate optimized architecture of Reversible Fault Tolerant adder circuits which gather better performance than existing all fault tolerant designs. This paper has covered the designs of minimum cost fault tolerant Carry Skip Adder (RFT-CSA) and Carry Look-ahead Adder Circuits. Both designs have used the proposed structure of fault tolerant Full Adder (RFT-FA or SNFA) circuit has minimum quantum cost 11. Several number of theorems have been proposed to make the designs of RFT-CSA and RFT-CLA more generalized for n-bit fault tolerant adder circuitry. Finally, we have attached the evolutionary report of performance of proposed designs.

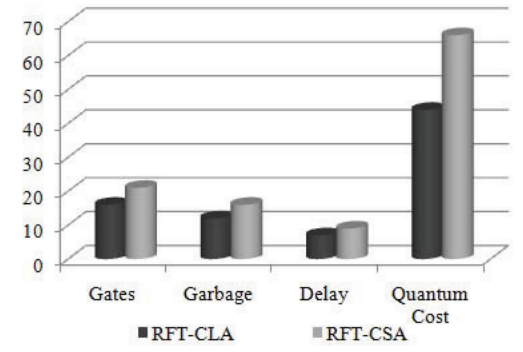


Fig. 13. Comparison between Proposed design of 4-bit Reversible Fault Tolerant Carry Skip Adder and Carry Look-ahead Adder

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