MINVDD Testing for Weak CMOS ICs

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Abstract

A weak chip is one that contains flaws – defects that do not interfere with correct circuit operation at normal conditions but may cause intermittent or early-life failures. ***MINVDD testing*** *can detect weak CMOS chips. The minvdd of a chip is the minimum supply voltage value at which a chip can function correctly. It can be used to differentiate between good chips and weak chips. In the first part of this paper, we will study several types of flaws to demonstrate the effectiveness of MINVDD testing. Experimental results show that MINVDD testing is as effective as VLV testing for screening out burn-in rejects.*

In the second part of this paper, we propose test conditions for low voltage testing, including test voltage, test timing and test sets. Experimental results are presented to validate our proposal.

1. Introduction

Flaws are defects that do not cause chip malfunctions at normal operating conditions. Chips that contain flaws are *weak*. Weak chips escape manufacturing test but might fail early in the field. To avoid early life failures, it is necessary to screen out weak chips before shipping them to the customers.

The common techniques for detecting flaws include burn-in, IDDQ testing [Levi 81], high voltage stress [Barrette 96], and low voltage testing. Burn-in is effective for failure mechanisms that have either a large voltage acceleration factor or a large temperature activation energy [Hnatek 95]. However, burn-in is very expensive in terms of hardware cost and burn-in time. IDDQ testing might not be practical for deep sub-micron technology due to the increasing background currents. High voltage stress is effective for oxide defects, such as gate oxide shorts, but is not effective for defects on interconnects [Chang 96b].

Research has shown that flaws can be accelerated in a low voltage environment [Hao 93][Chang 96][Renovell 96][Li 00]. Very-Low-Voltage (VLV) testing was proposed for detecting weak CMOS ICs [Hao 93]. The test is applied at a voltage that is much lower than the nominal operating voltage. Based on the difference of the electrical behavior at different voltages, it has been shown that VLV testing is effective for flaws that are undetectable at normal voltages [Chang 98].

In the first part of this paper, we study another low voltage testing technique – MINVDD testing. The minvdd of a chip is the minimum supply voltage at which the chip can produce correct logic states at the outputs. In MINVDD testing, the minvdd of a chip is used to decide if it is good or weak. MINVDD testing was mentioned in [Ager 82], however, his application was on bipolar circuits. Here we study the effectiveness of MINVDD testing on CMOS integrated circuits. First, simulation results are presented to validate our study. Secondly, experimental results from chips manufactured in 0.7um CMOS technologies are presented. We also include the preliminary results from a 0.18um test chip experiment.

In the second part of this paper, we address the various aspects of low voltage testing: test voltage selection, test speed characterization, and effectiveness of test patterns. The test voltage should be set as low as possible to improve the flaw coverage. We propose to set the test voltage around the minvdd of the chip. Low voltage testing can be applied at-speed or at slow speed. At-speed test has a better chance of catching delay flaws, but requires repeated characterizations to account for process variations across different lots. On the other hand, slow-speed test might miss delay flaws that can be captured using an at-speed test. For at-speed test, the applied test set should have very high transition fault coverage. For slow-speed test, a test set of high stuck-at fault coverage can do a good job.

This paper is organized as follows. Section 2 describes MINVDD testing for a CMOS circuit. Section 3 studies the issue of characterizations at low voltages. Based on the study in Sec.3, we propose test conditions for low voltage testing in section 4. Section 5 concludes the paper.

2. MINVDD Testing

2.1 minvdd for good chips

The operation of a CMOS circuit is supply voltage-dependent. At a higher voltage, a circuit switches faster. On the other hand, a circuit switches slower at a lower voltage. If the voltage is low enough the circuit may not switch at all. *The minvdd is the voltage below which the circuit stops switching.*

Figure 1 shows the measured voltage-delay relationship for a Murphy chip [Ma 95]. The Murphy chips were built in a 0.7um CMOS technology. The nominal supply voltage is 5V. As shown in Fig.1, the chip delay increases as the voltage decreases. At voltages below 1.24V, the chip's outputs never switch to the correct logic states. Therefore, the minvdd of the chip is 1.24V according to the definition.

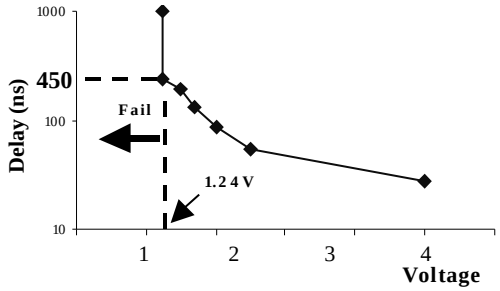

Figure 1. Voltage-delay relationship for a Murphy chip

2.2 minvdd for weak chips

In this section, we study the minvdd for weak chips that contain various types of flaws, including metal shorts, gate-oxide shorts, threshold voltage shifts, and tunneling opens. Metal shorts are unplanned metal connections between two nodes. Gate oxide shorts are unexpected connections between the terminals of a transistor. They are caused by random defects such as pin-holes in the oxide, or by process drifts that result in thinner oxide. Threshold voltage shifts can be caused by process variations or hot electron effects, the former can cause global threshold voltage shifts and the latter can cause either global or local threshold voltage shifts. Tunneling opens are caused by imperfections during fabrication such as incomplete etching or residue. All HSPICE simulations in this section were done with 0.18μm technology. The nominal operating voltage of this technology is 1.8V.

Metal shorts

A metal short is modeled by a resistor connected between two nodes. Figure 2 shows a metal short between 2 inverter chains. The gray line that connects node 'a' and 'b' is a metal short with resistance R_S. Suppose a logic "0" is applied at IN1 and a logic "1" is applied at IN2. Due to the metal short, a current path exists between node 'a' and node 'b'. The current path consists of the PMOS in inverter X1, the metal short, and the NMOS in inverter X3. As the result, the voltage levels at node a and b will not be VDD and GND, respectively, but some intermediate values between VDD and GND.

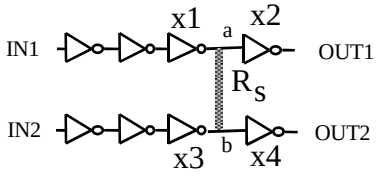

Figure 2: A metal short

Suppose the equivalent resistance[1] of the PMOS P1 is R_{P1} and the resistance of the NMOS N3 is R_{N3}. A voltage divider is formed by R_{P1}, R_s, and R_{N3}. The voltage level at node a, *V(a)*, can be expressed as

$$V(a) = \frac{R_s + R_{N3}}{R_{P1} + R_s + R_{N3}} \times VDD$$

As the supply voltage decreases, *V(a)* decreases because both R_{P1} and R_{N3} increase. Inverter X2 is weakly-driven because *V(a)* is further away from VDD, the ideal voltage level if there are no shorts. Therefore, the delay from IN1 to OUT1 increases due to the longer delay of inverter X2. As a result, the metal shorts cause timing failures due to the excess delay. If the supply voltage is low enough such that *V(a)* is below the logic threshold of inverter X2, inverter X2 will produce a logic "1" at OUT1, instead of the correct logic "0". The circuit starts to fail functionally at this voltage. This voltage is thus the minvdd for the circuits based on the definition in Sec.2.

Table 1 lists the simulated minvdd values for metal shorts with various short resistances. The short resistance, Rs, is varied from 1KΩ to 10KΩ. For a good circuit, the minvdd is 0.45V. For shorts with resistance less than 3 KΩ, the circuit fails at nominal voltage. We use N/A to denote their minvdd because the circuit cannot work at all for any voltage below the nominal voltage, 1.8V. For shorts with resistances between 3KΩ and 10KΩ, the minvdd decreases as the resistance increases but still is significantly higher than 0.45V.

Table 1: minvdd for circuits with metal shorts

Rs	1k	3k	5k	7k	10k	∞
minvdd	NA	NA	1.3V	1.0V	0.8V	0.45V

Gate Oxide shorts

An NMOS gate oxide short can be modeled by a resistor connected between the gate and the drain or source [Hao 91]. We will only discuss the case of gate-to-source short in this section. However, the results can be extended to the case of gate-to-drain shorts and gate-oxide shorts in PMOS as well [Hao 91].

Suppose there is a NMOS gate-to-source short inside inverter X4 in Fig.2. The short will create a path via the PMOS in inverter X3 and the gate-to-source short in the NMOS of X4. Therefore, the voltage level at the input of X4 is no longer GND, the ideal value, but a value higher than GND. Inverter X4 is thus weakly-driven and has excess delay. This effect will be accelerated as the supply voltage decreases. If the supply voltage is low enough, the circuit starts to fail functionally.

Tables 2 show the HSPICE simulation results. For a good circuit, the minvdd is 0.45V. For shorts with resistance less than 3 KΩ, the circuit fails at nominal voltage. As the short resistance increases from 4 KΩ and 10 KΩ, the minvdd values decreases from 1.6V to 0.8V, but is still significantly higher than 0.45V.

Table 2: minvdd for circuits with G-S shorts

Rs	1k	3k	5k	7k	10k	∞
minvdd	NA	NA	1.5V	1.2V	1.1V	0.45V

[1] The equivalent resistance of a transistor is the voltage between drain and source divided by the current.

Threshold Voltage Shifts

If a transistor has a larger threshold voltage than expected, its transconductance is smaller. As a result, the transistor has lower drive capability and causes an excessive delay during a transition. Here we will estimate the impact on minvdd when threshold voltage shifts exists.

The minvdd of a circuit is the minimum supply voltage at which the circuit can still function correctly. Another way to define the minvdd is that *it is the supply voltage below which the propagation delay becomes infinite.* If the propagation delay is infifinite, it means the circuit will not switch at all. Equation (1) is an expression for the propagation delay for a CMOS gate [Chandrakasan 92].[2] According to eq(1), the propagation delay of a circuit will become ∞ at VDD=V_t due to the $(VDD-V_t)^2$ term in the denominator. Therefore, the minvdd of a good circuit should be slightly above Vt.

$$T_d = \frac{C_L \times VDD}{\mu C_{ox}(W/L)(VDD-V_t)^2} = K\frac{VDD}{(VDD-V_t)^2} \quad (1)$$

When there is a threshold voltage shifts ΔV, the delay for the gate with threshold voltage shift can be expressed by the following equation:

$$T_d = \frac{C_L \times VDD}{\mu C_{ox}(W/L)(VDD-V_t-\Delta V)^2} = K\frac{VDD}{(VDD-V_t-\Delta V)^2} \quad (2)$$

The propagation delay is ∞ at VDD=V_t+ΔV. Therefore, the minvdd is increased by the same amount of shifts of the threshold voltage. The larger the threshold voltage shifts, the larger the minvdd.

Tunneling Opens

A tunneling open is a thin layer of oxide that resides mostly in vias and contacts. The current can flow through the thin layer of oxides, however, the magnitude of the current decrease exponentially with the voltage. As a result, a circuit with tunneling opens behaves like a good chip at nominal voltage, but is much slower than a good chip at low voltages [Li 00]. Figure 3 shows the voltage-delay relationship of a good chip and a chip that has a tunneling open. As voltage decreases, the delay of a circuit with a tunneling open increases much faster than that of a good chip. However, the minvdd for a chip with a tunneling open is the same as that for a good chip because tunneling opens only cause timing failures.

Based on the above discussions, flaws can be classified into two types[3]:

Type I: A chip containing type-I flaws has a higher minvdd than a good chip. Gate-oxide shorts, metal shorts, and threshold voltage shifts are type-I flaws.

Type II: A chip containing type-II flaws has similar minvdd value as a good chip. However, it operates at a slower speed than a good chip at minvdd. Tunneling open are type-II flaws.

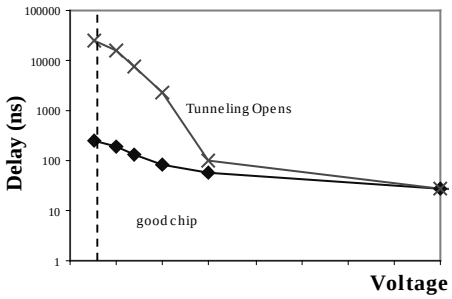

Figure 3: Voltage-delay relationships for tunneling opens

2.3 MINVDD Testing Flow

MINVDD testing uses the minvdd of a chip to decide if the chip is weak. First the minvdd of good chips from different manufacturing lots are characterized to find the minvdd distribution for good chips. A test speed *slower* than the speed of good chips at their minvdd is then selected. The test speed selection will be described in detail in the next paragraph. For all other chips, each is tested by starting at a very low VDD at which the chip fails the test, and raising the VDD up until the chip passes the test. The VDD value at which the chip starts to pass the test is recorded as the minvdd of the chip. After recording the minvdd for all the chips. CUTs with abnormal minvdd are identified as "outliers".

The test speed should be selected such that the resulting minvdd equals the true minvdd for good chips. For example, in Fig.1, the true minvdd for a good Murphy chip can only be obtained when the test speed is slower than 450nS. If the test speed is chosen as 100nS, the measured voltage will be the voltage for the chip to work at that speed, 1.9V, instead of the real minvdd, 1.24V.

2.4 Murphy Experimental Results

We performed MINVDD testing on 320 Murphy CUTs, including the 9 VLV-only CUTs, 195 good CUTs, and 116 defective CUTs [McCluskey 00]. Table 3 lists the characterized minvdd and the corresponding speed for all 5 CUT designs from 4 different manufactured lots. The test speed is set to 600nS, which is 33% larger than the speed of the slowest good CUT at its minvdd (6sq, 450nS). The search for minvdd starts at 1V with 0.02V increment.

Table 4 and 5 list the experimental results. All the 116 defective CUTs failed MINVDD test because they all showed significantly high minvdd values. For the 9 VLV-only CUTs, their minvdd values range from 2.2V to 4V, which is away from the minvdd range of good CUTs, 1.20V-1.26V. They were identified as outliers and were declared as MINVDD failures also.

[2] EQ(1) is only a first-order approximation of the circuit delay. It is also not accurate for predicting the delay at nominal voltage due to the transistor velocity saturations [Plummer 00]. However, a transistor's velocity saturation disappears at low voltage environment. Consequently, eq(1) can still be used for predicting the circuit delay at low voltages.

[3] Other flaws can also be classified based on the above criterions. For example, resistive interconnect is a type-II flaw because it only cause timing failures but not functional failures at low voltages. Due to the limit of paper, we will not discuss the impact on minvdd by other flaws.

Table 3: Characterized minvdd & speed for Murphy CUTs

	CUT	6sq	m12	rob	sim	std
Minvdd (V)	*max*	1.26	1.26	1.26	1.26	1.26
	min	1.20	1.20	1.20	1.20	1.20
Speed (ns)	*max*	450	302	196	198	188
	min	392	258	170	168	156

Table 4: MINVDD Testing results

	Good	Defective	VLV-only
Pass	191	0	0
Fail	0	116	9

Table 5: MINVDD testing results for 9 VLV-only CUTs

CUT	minvdd	Results
good	1.20-1.26	Pass
1	4	***Fail***
2	3.5	***Fail***
3	2.4	***Fail***
4	2.4	***Fail***
5	2.4	***Fail***
6	2.3	***Fail***
7	2.3	***Fail***
8	2.2	***Fail***
9	2.2	***Fail***

2.5 Preliminary 0.18um Experimental Results

We have been collecting data using an ASIC device to evaluate the effectiveness of several reliability screening techniques, including MINVDD testing. In this section, we briefly describe the experiment and present some preliminary testing results. The ASIC chip is built in 0.18um technology and the nominal supply voltage is 2.5V. The chip has been designed with full scan capability. MINVDD testing was applied at a slow speed (1MHz). The *minvdd* is measured for six different groups of test patterns. A chip is classified as a minvdd-only chip if the following conditions are true: (1) The chip passed stuck-fault and delay tests and has normal IDDQ values. (2) The chip is a minvdd outlier for any of the six test sets. A minvdd outlier is one whose minvdd is at least 0.2V from the minvdd distribution of good chips.

To date, we have found a significant number (>50) of minvdd outlier devices. Our plan is to understand the behavior of these devices and perform root cause analysis of a sample of these parts at some point in the future.

2.6 Summary

In this section, we studied the minvdd values for weak chips that contain various kinds of flaws to demonstrate the effectiveness of MINVDD testing. We also showed results from both 0.7um and 0.18um test experiment. Both results showed that MINVDD testing can screen out weak chips.

However, the test flow for MINVDD testing might not be practical for inclusion in production testing due to the lengthy search of the minvdd. It is preferred to set one voltage and one test timing to perform pass/fail testing during production testing in order to save test time. To find the test voltage and test speed requires thorough characterizations. In the next section, we will address issues of characterizations in low voltage regime. We will provide the guidelines for performing low voltage testing in Sec.4.

3. Characterization Issues

Both VLV testing and MINVDD testing expose flaws by operating the weak chip at a much lower than normal voltage. Both tests requires thorough characterizations in order to select the appropriate test voltage and test speed. In this section, we will discuss some issues about characterizations in low voltage environment.

3.1 Timing Characterizations

Table 6 listed the characterized speed for good Murphy CUTs at 3 different voltages: 5V, 2.5Vand 1.7V. For each CUT design, 200 CUTs from 4 manufactured lots (50 CUTs each lot) are characterized to find their speeds at the corresponding voltages. Each entry is the averaged speed of CUTs from the same lot. The data in Table 6 show that the CUT speed varied more significantly at lower voltage than at nominal voltage. At 5V, the CUT speeds from different lots are close for all the five CUT designs. At 1.7V, 15%-20% variations can be observed for all five CUT designs. As a result, it will be difficult to pick up a single speed to test all CUTs in low voltage regime due to the sensitivity of CUT speed to process variations.

Table 6: Average CUT speed(ns) at different voltages

		CUT				
		6sq	m12	rob	sim	std
5V	Lot 1	**26**	**24**	**14**	**14**	**12**
	Lot 2	28	26	14	14	12
	Lot 3	28	26	14	14	12
	Lot 4	**28**	**26**	**14**	**14**	**12**
2.5 V	Lot 1	**76**	**68**	**34**	**32**	**28**
	Lot 2	78	70	36	34	28
	Lot 3	80	72	36	34	30
	Lot 4	**84**	**76**	**38**	**36**	**30**
1.7 V	Lot 1	**126**	**106**	**52**	**48**	**40**
	Lot 2	132	114	54	50	44
	Lot 3	136	118	56	52	44
	Lot 4	**146**	**126**	**60**	**56**	**46**

3.2 Voltage Characterizations

We also characterized the voltages vs. CUT speeds for all 5 CUT designs at 5 different speeds: 100ns, 200ns, 400ns, 500ns, and 600ns. The results are presented in Table 7. For each CUT, the supply voltage for it to work at the corresponding speed is recorded. For each CUT design, Table 7 lists the min/max of all the records at the corresponding speeds. For example, for CUT 6sq, the supply voltage for the CUT from 4 different lots to work at 100nS ranges from 1.83V to 2.01V. If the speed is 500ns, the supply voltage ranges from 1.20V to 1.26V, which is the range of minvdd values for the CUT design.

The results in Table 7 suggest that the minvdd value of a good chip might not be sensitive to the design. Different designs could have similar minvdd values. The intuitive explanation is that the minvdd for a static CMOS circuit is between 1 and 2 times the threshold voltage of a transistor (consider an inverter). This limit depends mostly on the technology, not on the design.

Table 7: Supply voltages at different speeds

		CUT				
speed	Minvdd	6sq	m12	rob	sim	std
100 ns	Min	1.83	1.77	1.41	1.41	1.41
	Max	2.01	1.86	1.50	1.50	1.47
200 ns	Min	1.44	1.41	1.29	1.26	1.26
	Max	1.56	1.53	1.35	1.35	1.35
400 ns	Min	1.26	1.20	**1.20**	**1.20**	**1.20**
	Max	1.32	1.29	**1.26**	**1.26**	**1.26**
500 ns	Min	**1.20**	**1.20**	**1.20**	**1.20**	**1.20**
	Max	**1.26**	**1.26**	**1.26**	**1.26**	**1.26**
600 ns	Min	**1.20**	**1.20**	**1.20**	**1.20**	**1.20**
	Max	**1.26**	**1.26**	**1.26**	**1.26**	**1.26**

3.3 Summary

In this section, we present experimental characterization results in low voltage regime. For a given voltage, it is difficult to find a single chip speed for low voltage testing because the chip speed is more sensitive to process variations. For a given speed, it is possible to find a single voltage to test chips manufactured in different conditions, if the speed is slow enough. The resulting voltage is actually the minvdd for the chip as defined in Sec.2.

4. How to Perform Low Voltage Testing

For MINVDD testing, a slow test speed is specified and the minvdd value of the chip-under-test is measured via searching. As a result, it is not efficient due to the lengthy time it requires to search for minvdd. For VLV testing, a predetermined test voltage is specified and the test speed is derived from characterizations. As discussed in the previous section, it is very difficult to determine a single test speed for chips from various manufacturing conditions because the chip speed is more sensitive to process variations in the low voltage regime.

In this section, we propose the test conditions for performing low-voltage testing, including test voltage, test speed, and test sets to apply. Our discussions are based on the assumptions that low voltage testing should be applied with a single test voltage and a single test speed.

4.1 Test Voltage

Flaws that are more observable at lower voltages include metal shorts, gate-oxide shorts, threshold voltage shifts, tunneling opens, and specific interconnect defects. [Hao 93][Chang 96][Li 00]. For all the flaws listed above, the lower the supply voltages the higher the chance they are observable. Therefore, for a single design, the test voltage to be used in low voltage testing should be as low as possible to achieve the highest coverage of flaws. The lowest voltage a chip can work at is the minvdd for the chip.

As shown in the previous section, the minvdd values for different designs in the same technology are very close to one another. For the 5 Murphy CUT designs, their minvdd values are between 1.20V and 1.26V. To save the cost associated with characterizations for different designs, it also leads to the choice of minvdd as the test voltage.

In summary, the test voltage should be set to the minvdd of the chip-under-test to achieve the maximum flaw coverage and reduce the costs associated with the design-to-design characterizations.

4.2 Test Timing

After setting the test voltage to minvdd of the chip, low voltage testing can be applied at slow speed or characterized speed. For type-I flaws, their detectability does not depend on the test speed because they cause hard failures at minvdd. Type-II flaws, however, cause only timing failures at minvdd. Therefore, at-speed testing has the best chance to capture them. At-speed test is therefore more *effective* than slow speed test.

On the other hand, at-speed test requires lot-to-lot characterizations to determine the test speed because of the sensitivity of chip speed to process variations at low voltages. From the perspective of efficiency, slow-test is more efficient than at-speed test.

In summary, at-speed test can catch more flaws that cause timing problems than slow speed test. Slow-speed test is more efficient because it does not require lot-to-lot characterizations. The choice between the two schemes depends on the defect populations and test cost.

4.3 Test Sets

Flaws can cause either hard failures or timing failures at minvdd. If a flaw causes hard failures, a test set with high single stuck-at fault coverage can be applied to catch it. If a flaw causes timing failures, a test set with high transition fault coverage will have the best chance to catch it [McCluskey 00]. In the Murphy experiment, test sets that detect each stuck-at fault multiple times, n-detect, are the most effective. They all have very high transition fault coverage. As a result, they were able to catch timing failures even though they were generated with stuck-at fault models.

In summary, a test set with high stuck-at fault coverage and transition fault coverage has the best chance to catch flaws.

4.4 Experimental Results

Table 8 lists the number of Murphy CUTs that escaped low voltage testing at three different test conditions. The minvdd values for the CUTs are between 1.20V and 1.26V. We used 1.3V as the test voltage according to the discussion in Sec. 4.1. The test speeds for at-speed test at both 1.3V and 1.7V are derived from characterizations, while the slow speed at 1.3V is 3 times

slower than the characterized speed at 1.3V. The total number of CUTs tested is 125, including 116 defective CUTs and 9 VLV-only CUTs.

Table 8: Low voltage testing escapes

Fault Mode	Cover age %	1.7V at-speed	1.3V at-speed	1.3V slow speed
SSF	500	3	1	1
	300	3	2	2
	100	3	2	3
	95	10	7	8
	90	16	8	10
	80	21	9	12
Transition	100	5	3	4

For stuck-at test sets, the number of escapes decreases as the fault coverage increases. The best stuck-at test set is the 5-detect test. Comparing the number of escapes, testing at 1.3V is more effective than testing at 1.7V. It is more effective to test at-speed, however, the difference is 1-2 CUTs in our experiment. For test sets with high SSF coverage, test sets with higher transition fault coverage detect more defective CUTs.

5. Conclusions

MINVDD testing uses the minimum voltage at which a circuit can operate correctly to differentiate between good and weak chips. The minvdd of a weak chip is much higher than that of a good chip. MINVDD testing is effective for detecting type-I flaws such as metal shorts, gate oxide shorts and threshold voltage shifts, and type-II flaws such as tunneling opens. Simulation results show a significant minvdd difference between good chips and weak ships containing these flaws. The test chip experimental results also suggest that MINVDD testing is an effective reliability screening technique. For the nine weak chips already identified in the Murphy experiment, MINVDD testing detects all of them.

Both MINVDD testing and VLV testing are special cases of low voltage testing. We propose the test conditions for implementing low voltage testing. The test voltage should be set to the minvdd values of the chip-under-test. At-speed test has a better chance of catching delay flaws, but requires repeated characterizations to account for process variations. On the other hand, slow-speed test might miss delay flaws that can be captured using an at-speed test. For at-speed test, the applied test set should have very high transition fault coverage. For slow-speed test, a test set of high stuck-at fault coverage can do a good job.

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